Quad Voltage Monitor and Sequencer

Preliminary Technical Data

ADM1185

FEATURES

Powered from 2.7V to 5.5V on the VCC pin

Monitors Four Supplies via 0.8% Accurate Comparators

Four inputs can be programmed for voltage levels with resistor dividers

Three Open-Drain Enable Outputs

Open-Drain Power Good Output

10-pin MSOP Package

APPLICATIONS

Monitor and Alarm Functions

Power Supply Sequencing

Telecommunication and Datacommunication Equipment

PC/Servers

GENERAL DESCRIPTION

The ADM1185 is an integrated four channel voltage monitoring device. A 2.7V to 5.5V power supply is required on the VCC pin to power the device.

Four precision comparators monitor four voltage rails. All comparators have a 0.6V reference with a worst-case accuracy of 0.8%. Resistor networks external to the VIN1-VIN4 pins set the trip points.

There are four open-drain outputs on the device. A digital core interprets the comparator outputs and asserts the outputs as appropriate.

FUNCTIONAL BLOCK DIAGRAM

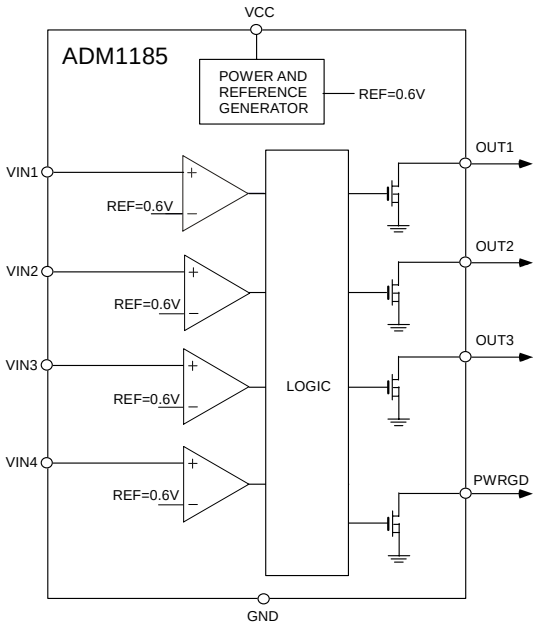

Figure 1.

APPLICATIONS DIAGRAM

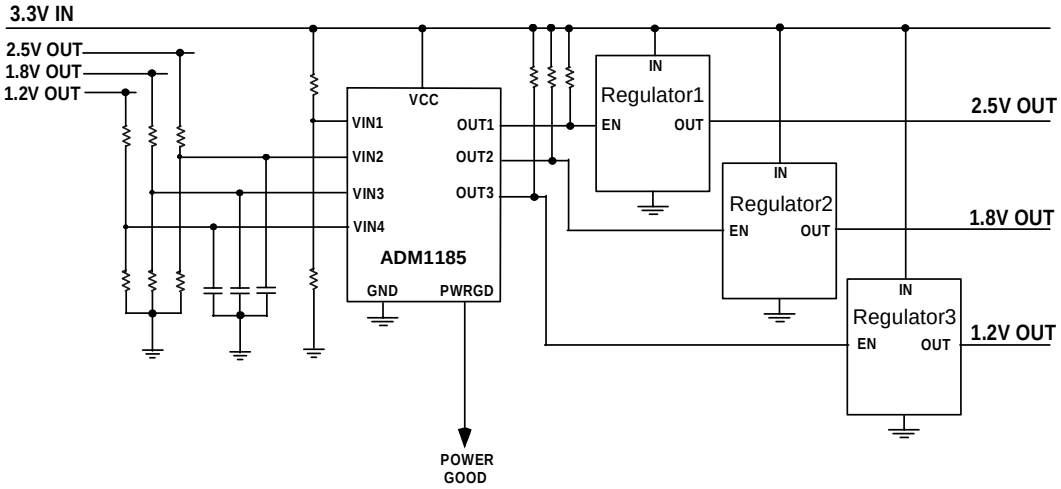

Figure 2.

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ADM1185—SPECIFICATIONS

V_{VCC} = 2.7V to 5.5V, T_A = -40°C to +85°C

Table 1.

Parameter	Min	Typ	Max	Units	Conditions
VCC Pin					
Operating Voltage Range, V_{VCC}	2.7		5.5	V	
Supply Current, I_{VCC}		30	100	µA	
VIN1-VIN4 Pins					
Input Current, $I_{VINLEAK}$	-100		100	nA	V_{VINx} = 0.7V
Input Rising Threshold, V_{THR}	0.5952	0.6000	0.6048	V	
Input Rising Hysteresis, V_{HYST} (=V_{THR}-V_{THF})		9		mV	
OUT1-OUT3, PWRGD Pins					
Output low voltage, V_{OUTL}			0.4	V	V_{VCC} = 2.7 V, I_{SINK} = 2mA
			0.4	V	V_{VCC} = 1 V, I_{SINK} =100µA
Leakage Current, I_{ALERT}	-1		1	µA	
V_{VCC} that guarantees outputs valid	1			V	All outputs will be guaranteed to be either low or giving a valid output level from V_{VCC} = 1V.
VIN1 to OUT1 Delay	100	190	280	ms	V_{VIN1} Rising
VIN4 to PWRGD Delay	100	190	280	ms	V_{VIN4} Rising, condition only valid at certain operational states, refer to state diagram
High-to-Low Propagation Delay		30		µs	V_{VCC} =3.3V, see TPC1
Low-to-High Propagation Delay		30		µs	V_{VCC} =3.3V, see TPC1

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{CC} Pin	−0.3 V to +6 V
VIN1-VIN4 Pin	−0.3 V to +6 V
OUT1-OUT3, PWRGD Pins	−0.3 V to +6 V
Power Dissipation	TBD
Storage Temperature	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature Range (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability. Ambient temperature = 25°C, unless otherwise noted.

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

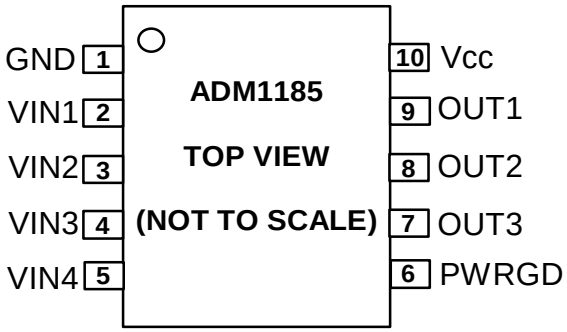


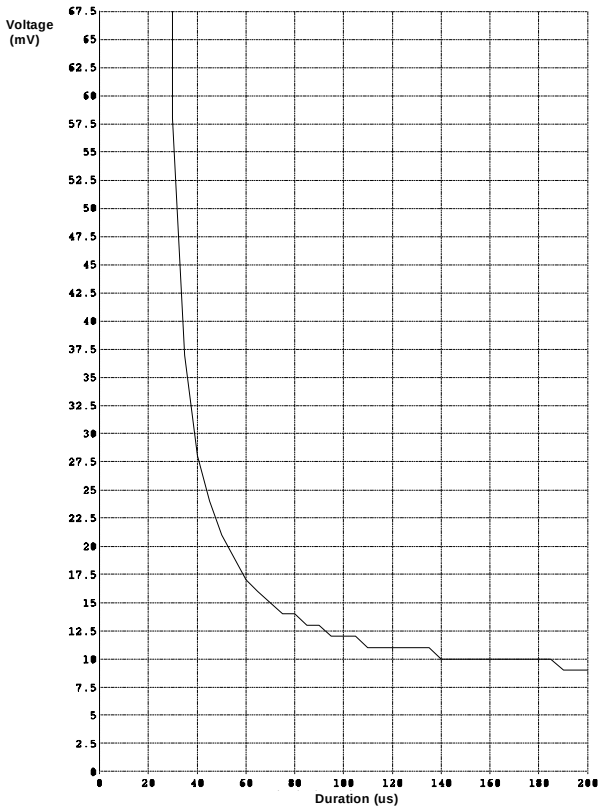
Figure 3. Pin Configurations

PIN FUNCTIONAL DESCRIPTIONS

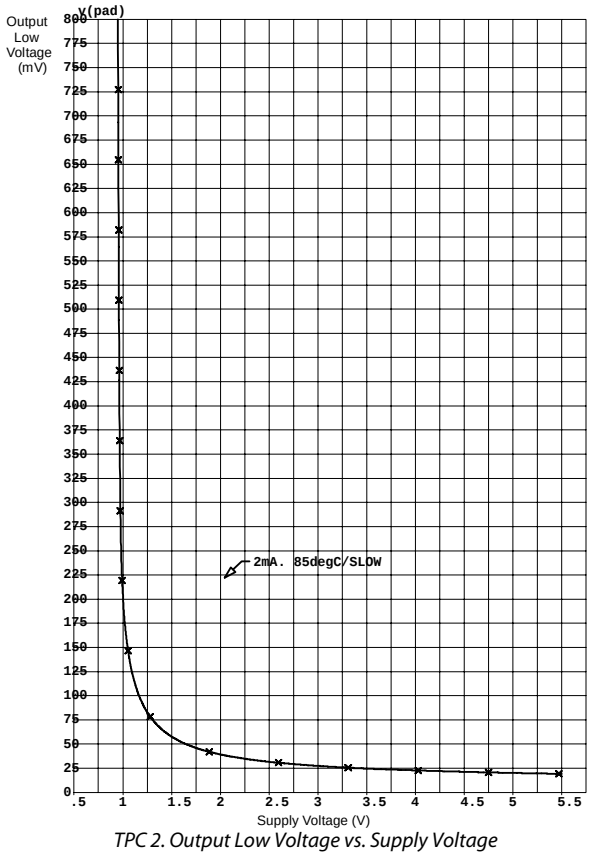
Table 3.

Pin No.	Name	Description
1	GND	Chip Ground Pin.
2	VIN1	Non-inverting input of comparator 1. The voltage on this pin is compared with a 0.6V reference. Can be used to monitor a voltage rail via a resistor divider.
3	VIN2	Non-inverting input of comparator 2. The voltage on this pin is compared with a 0.6V reference. Can be used to monitor a voltage rail via a resistor divider.
4	VIN3	Non-inverting input of comparator 3. The voltage on this pin is compared with a 0.6V reference. Can be used to monitor a voltage rail via a resistor divider.
5	VIN4	Non-inverting input of comparator 4. The voltage on this pin is compared with a 0.6V reference. Can be used to monitor a voltage rail via a resistor divider.
6	PWRGD	Open-drain output. During a power-up sequence (before PWRGD asserts) this output will assert high when the voltage on VIN4 is greater than 0.6V. A time delay of 190ms (typical) is included before assertion of this pin. After power-up (after PWRGD asserts) this output will be driven low if any of the voltages on the VIN1-VIN4 pins falls below 0.6V.
7	OUT3	Open-drain output. During a power-up sequence (before PWRGD asserts) this output will assert high when the voltage on VIN3 is greater than 0.6V. After power-up (after PWRGD asserts) this output will be driven low if the voltage on VIN1 falls below 0.6V.
8	OUT2	Open-drain output. During a power-up sequence (before PWRGD asserts) this output will assert high when the voltage on VIN2 is greater than 0.6V. After power-up (after PWRGD asserts) this output will be driven low if the voltage on VIN1 falls below 0.6V.
9	OUT1	Open-drain output. During a power-up sequence (before PWRGD asserts) this output will assert high when the voltage on VIN1 is greater than 0.6V. A time delay of 190ms (typical) is included before assertion of this pin. After power-up (after PWRGD asserts) this output will be driven low if the voltage on VIN1 falls below 0.6V.
10	VCC	Positive supply input pin. The operating supply voltage range is 2.7 V to 5.5 V.

TYPICAL PERFORMANCE CURVES



TPC 1. Maximum transient duration Without Causing an Output Pulse vs. Output Comparator Overdrive



TPC 2. Output Low Voltage vs. Supply Voltage

Functional Description

The operation of the ADM1185 is explained in this section in the context of the device in a voltage monitoring and sequencing application (figure 4, above). In this application, the ADM1185 will monitor four separate voltage rails, turn on three regulators in a predefined sequence and generate a power good signal to turn on a controller when all power supplies are up and stable.

POWER ON SEQUENCING AND MONITORING

The main supply (in this case 3.3V) powers up the device via the VCC pin as the voltage rises. A supply voltage of 2.7V to 5.5V is needed to power the device.

The VIN1 pin is monitoring the main 3.3V supply. An external resistor divider will scale this voltage down for monitoring at the VIN1 pin. The resistor ratio is chosen so that the VIN1 voltage is 0.6V when the main voltage rises to the preferred level at start-up (some voltage below the nominal 3.3V level). In this case, R1 is 4.6K and R2 is 1.2K so that a voltage level of 2.9V will correspond to 0.6V on the non-inverting input of the first comparator.

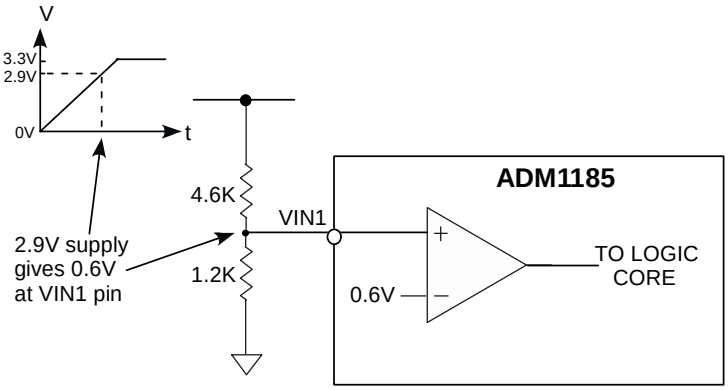


Figure 4.Setting the undervoltage threshold with an external resistor divider

OUT1 is an open drain active high output. In this application, OUT1 is connected to the enable pin of a regulator. Before the voltage on VIN1 has reached 0.6V this output is switched to ground, disabling regulator 1. (Note that all outputs are driven to ground as long as there is 1V on the VCC pin of the ADM1185). When the main system voltage reaches 2.9V VIN1 will detect 0.6V and this will cause OUT1 to assert after a 190ms delay. When this occurs the open drain output will switch high and the external pull-up resistor will pull the voltage on the regulator 1 enable pin above its turn-on threshold, turning on the output of regulator 1.

The assertion of OUT1 will turn on Regulator1. The 2.5V output of this regulator will begin to rise. This will be detected by input VIN2 (with a similar resistor divider scheme as shows in figure 5). When VIN2 sees the 2.5V rail rise above its UV point it will assert output OUT2, turning on Regulator2. A capacitor can be placed on the VIN2 pin to slow the rise of the voltage on this pin- this effectively sets a time delay between the 2.5V rail powering up and the next Regulator being enabled.

The same scheme is implemented with the other input and output pins. Every rail that is turned on via an output pin OUT(n) is monitored via input pin VIN(n+1).

The final comparator inside the VIN4 pin detects the final supply turning on, which is 1.2V in this case. All of the output pins (OUT1-OUT3) are logically ANDed together to generate a system power good signal (PWRGD). There is an internal 190ms delay associated with the assertion of the PWRGD output.

Table 4 below is a truth table that steps through the power on sequence of the outputs. Any associated internal time delays are also shown.

VOLTAGE MONITORING AFTER POWER ON

Once PWRGD is asserted the logical core latches into a different mode of operation. During the initial power up phase each output is directly dependant on an input (i.e. VIN3 asserting causes OUT3 to assert). When power up is complete this function is redundant.

Once in the PWRGD state the following behavior can be observed:

- If the main 3.3V supply that is monitored via VIN1 faults in the power good state then the PWRGD output is deasserted to warn the downstream controller and all of the outputs OUT1-OUT3 are immediately turned off, disabling all locally generated supplies.
- If a supply monitored by VIN2-VIN4 fails the PWRGD output is deasserted to warn the controller but the other outputs are not deasserted.

Table 5 and table 6 are truth tables that highlight the behavior of the ADM1185 under various fault situations during normal operation (i.e. in the mode of operation after PWRGD has asserted).

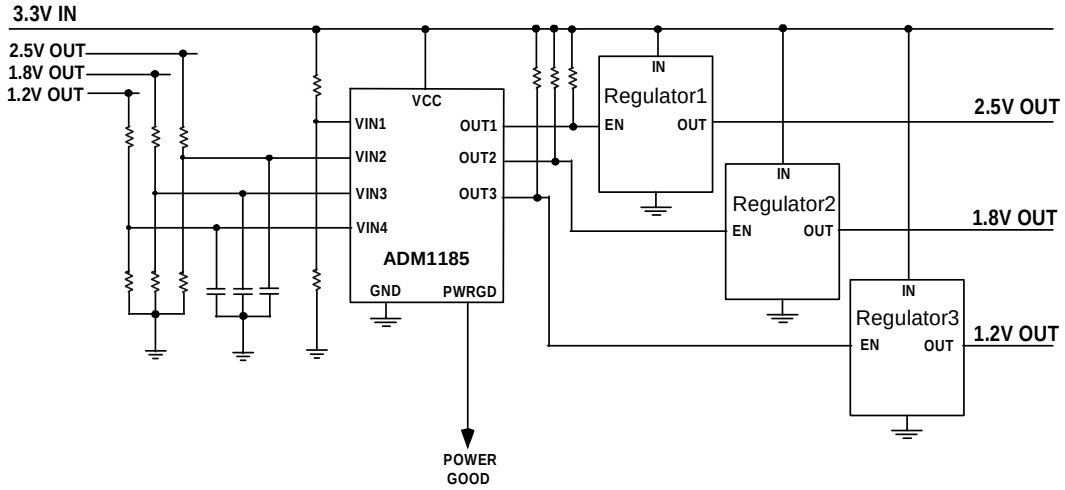


Figure 5. Applications Diagram showing ADM1185 in a voltage monitoring and sequencing application

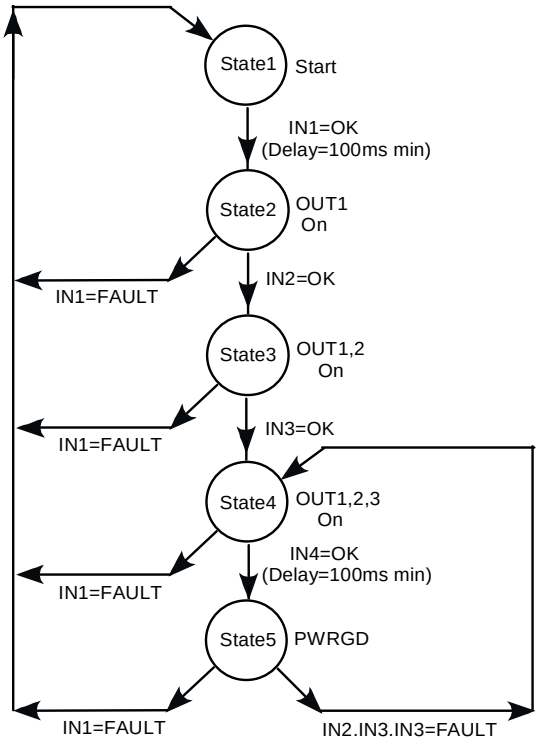
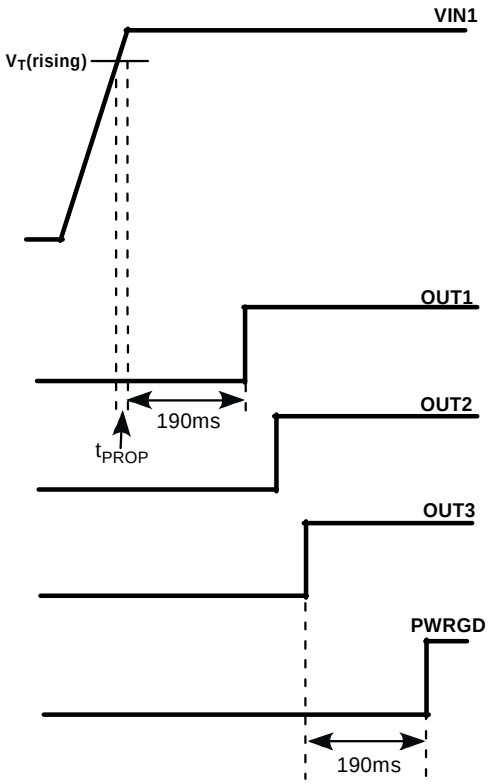


Figure 6. Flow Diagram highlighting the different modes of operation o the logical core

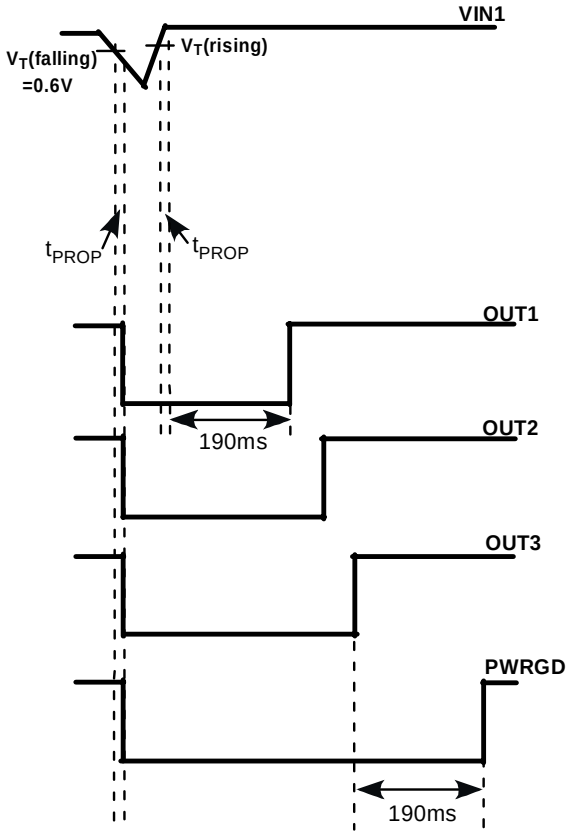
State	State Name	OUT1	OUT2	OUT3	OUT4	Next Event	Next State
1	Reset*	0	0	0	0	IN1 High for 190ms	Out1 On
2	Out1 On	1	0	0	0	IN1 and IN2 High for 30us	Out1,2 On
3	Out1,2 On	1	1	0	0	IN1 and IN3 High for 30us	Out1,2,3 On
4	Out1,2,3 On	1	1	1	0	All High for 190ms	PowerGood
5	PowerGood	1	1	1	1	IN2 or IN3 or IN4 Low for 30us	Out1,2,3 On
						IN1 Low for 30 us	Start

Table 4. Truth table



NOTE* The rising threshold on the VIN1-VIN4 pins will be slightly higher than 0.6V as there is some hysteresis on this pin.

Figure 6. Power-up Waveforms



NOTE* The rising threshold on the VIN1-VIN4 pins will be slightly higher than 0.6V as there is some hysteresis on this pin.

Figure 7. Waveforms showing reaction to a temporary low glitch on the main supply

CASCADING MULTIPLE DEVICES

Multiple ADM1185 devices can be cascaded in situations where a large number of supplies must be monitored and/or sequenced. There are numerous configurations for interconnecting devices. The most suitable configuration will depend on the application. Figures 8, 9 and 10 show some methods for cascading multiple ADM1185 devices.

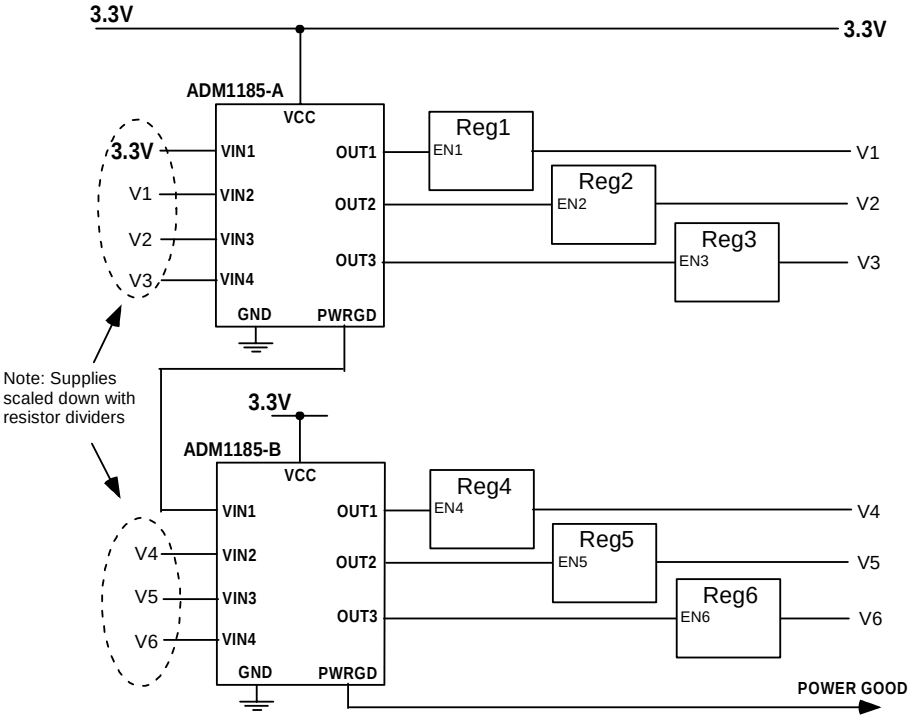


Figure 8. Cascading multiple ADM1185 devices, option 1

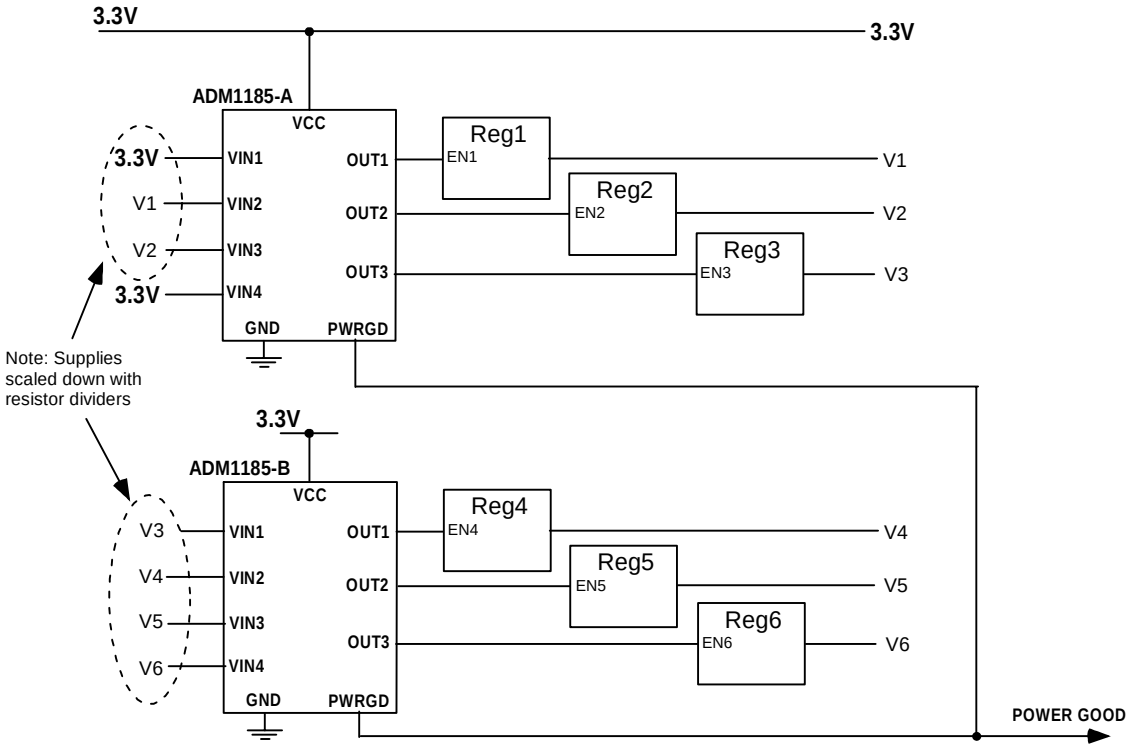


Figure 9. Cascading multiple ADM1185 devices, option 2

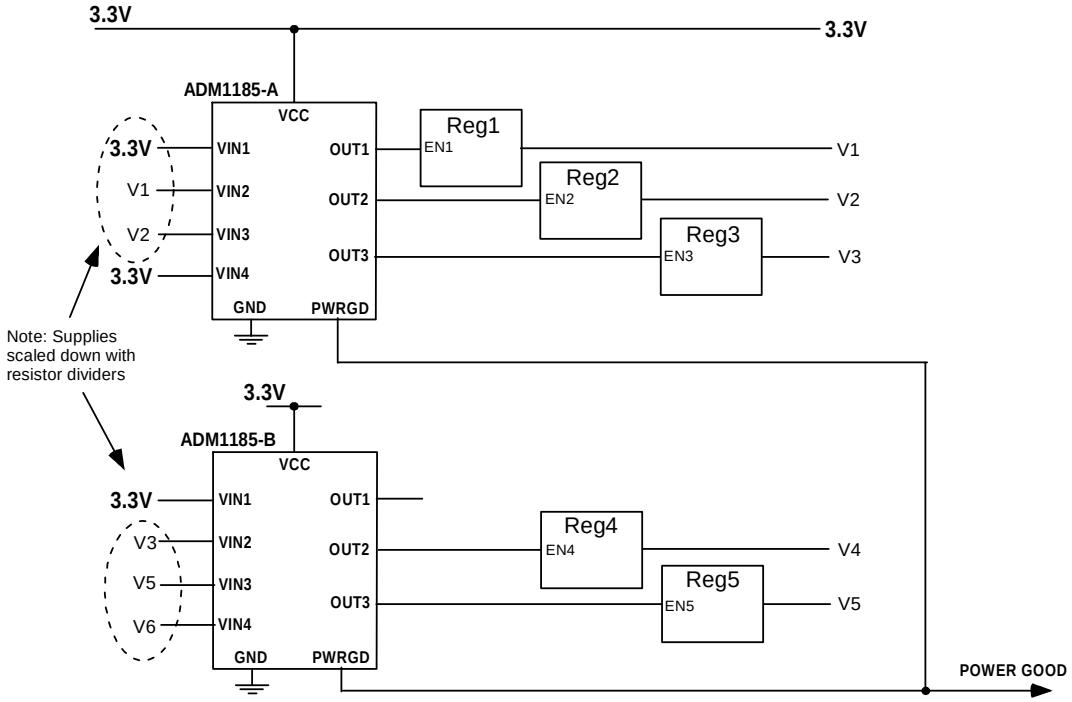


Figure 10. Cascading multiple ADM1185 devices, option 3

OUTLINE DIMENSIONS

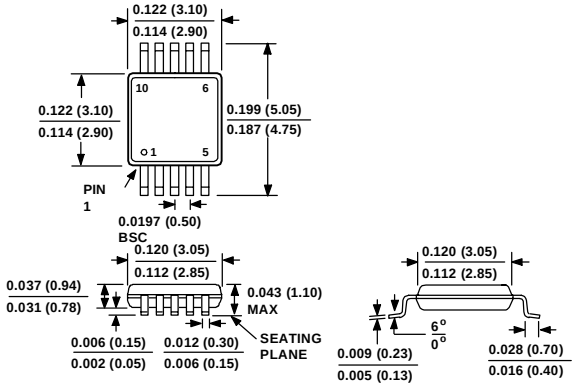


Figure 9. 10-Lead MSOP Package
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Outline
ADM1185ARMZ[1]	-40°C to +85°C	MSOP-10	RM-10

Z=PB-free part

PR06196-0-6/06(PrK)