High Speed Isolated RS-485 Transceiver with Integrated Transformer Driver

Preliminary Technical Data

ADM2485

FEATURES

- Half-duplex isolated RS-485 transceiver
- Integrated oscillator driver for external transformer
- PROFIBUS compliant
- Complies with ANSI TIA/EIA RS-485-A-1998 and ISO 8482:1987(E)
- 16 Mbps data rate
- 5 V or 3 V operation (V_{DD1})
- High common-mode transient immunity: >25 kV/µs
- Isolated DE OUT status output
- Thermal shutdown protection
- Safety and regulatory approvals:
  - UL recognition—2500 V_{RMS} for 1 minute per UL 1577 (pending)
  - CSA component acceptance notice #5A
  - VDE certificate of conformity
    - DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01
    - DIN EN 60950 (VDE 0805):2001-12; EN 60950: 2000
    - V_{IORM} = 560 V peak
- Operating temperature range: -40° to 85°C
- Wide body 16-lead SOIC package

APPLICATIONS

- Isolated RS-485/RS-422 interfaces
- PROFIBUS networks
- Industrial field networks
- Multipoint data transmission systems

GENERAL DESCRIPTION

The ADM2485 differential bus transceiver is an integrated, galvanically isolated component designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and complies with ANSI TIA/EIA RS-485-A-1998 and ISO 8482:1987(E).

The device employs Analog Devices' *i*Coupler technology to combine a 3-channel isolator, a 3-state differential line driver, and a differential input receiver into a single package. An on-chip oscillator outputs a pair of square waveforms which drive an external transformer to provide isolated power with an external transformer. The logic side of the device can be powered with either a 5 V or a 3 V supply while the bus side is powered with an isolated 5 V supply.

The ADM2485 driver has an active high enable. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output port that imposes minimal loading on the bus when the driver is disabled or when V_{DD1} or V_{DD2} = 0 V. Also provided is an active high receiver disable that causes the receive output to enter a high impedance state.

The device has current-limiting and thermal shutdown features to protect against output short circuits and situations where bus contention might cause excessive power dissipation. The part is fully specified over the industrial temperature range and is available in a 16-lead wide-body SOIC package.

FUNCTIONAL BLOCK DIAGRAM

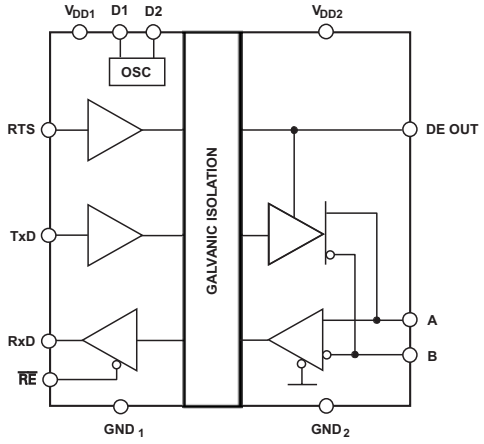

Figure 1

Rev.PrI

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

SPECIFICATIONS

$2.7 \le V_{DD1} \le 5.5$ V, 4.75 V $\le V_{DD2} \le 5.25$ V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Differential Outputs					
Differential Output Voltage, V_{OD}			5	V	R = ∞, Figure 3
	2.1		5	V	R = 50 Ω (RS-422), Figure 3
	2.1		5	V	R = 27 Ω (RS-485), Figure 3
	2.1		5	V	V_{TST} = −7 V to 12 V, $V_{DD1} \ge 4.75$, Figure 4
Δ $\|V_{OD}\|$ for Complementary Output States			0.2	V	R = 27 Ω or 50 Ω, Figure 3
Common-Mode Output Voltage, V_{OC}			3	V	R = 27 Ω or 50 Ω, Figure 3
Δ $\|V_{OC}\|$ for Complementary Output States			0.2	V	R = 27 Ω or 50 Ω, Figure 3
Output Short-Circuit Current, V_{OUT} = High	60		200	mA	-7 V $\le V_{OUT} \le +12$ V
Output Short-Circuit Current, V_{OUT} = Low	60		200	mA	-7 V $\le V_{OUT} \le +12$ V
Bus Enable Output					
Output High Voltage	$V_{DD2}-0.1$			V	I_{ODE} = 20 μA
	$V_{DD2}-0.3$	$V_{DD2}-0.1$		V	I_{ODE} = 1.6 mA
	$V_{DD2}-0.4$	$V_{DD2}-0.2$		V	I_{ODE} = 4 mA
Output Low Voltage			0.1	V	I_{ODE} = −20 μA
		0.1	0.3	V	I_{ODE} = −1.6 mA
		0.2	0.4	V	I_{ODE} = −4 mA
Logic Inputs					
Input High Voltage	0.7 V_{DD1}			V	TxD, RTS, $\overline{RE}$
Input Low Voltage			0.25 V_{DD1}	V	TxD, RTS, $\overline{RE}$
CMOS Logic Input Current (TxD, RTS, $\overline{RE}$)	−10	0.01	10	μA	TxD, RTS, $\overline{RE}$ = V_{DD1} or 0 V
RECEIVER					
Differential Inputs					
Differential Input Threshold Voltage, V_{TH}	−200		200	mV	-7 V $\le V_{CM} \le +12$V
Input Hysteresis		70		mV	-7 V $\le V_{CM} \le +12$V
Input Resistance (A, B)	20	30		kΩ	-7 V $\le V_{CM} \le +12$V
Input Current (A, B)			0.6	mA	V_{IN} = +12 V
			−0.35	mA	V_{IN} = −7 V
RxD Logic Output:					
Output High Voltage	$V_{DD1}-0.1$			V	I_{OUT} = 20 μA, V_A-V_B=0.2 V
	$V_{DD1}-0.4$	$V_{DD1}-0.2$		V	I_{OUT} = 4 mA, V_A-V_B=0.2 V
Output Low Voltage			0.1	V	I_{OUT} = −20 μA, V_A-V_B=-0.2 V
		0.2	0.4	V	I_{OUT} = −4 mA, V_A-V_B=-0.2 V
Output Short Circuit Current	7		85	mA	V_{OUT} = GND or V_{CC}
Three-State Output Leakage Current			±1	μA	0.4 V $\le V_{OUT} \le$ 2.4 V
Transformer Driver					
Oscillator Frequency		500		kHz	
Switch On resistance		0.5	1.5	Ω	
Start-Up Voltage		2.2	2.5	V	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY CURRENT					
Logic Side			1.3	mA	RTS = 0 V, V_{DD1} = 5.5 V
		1.0		mA	2 Mbps, V_{DD1} = 5.5 V, Figure 5
		4.0		mA	16 Mbps, V_{DD1} = 5.5 V, Figure 5
			0.8	mA	RTS = 0 V, V_{DD1} = 3 V
			1.1	mA	2 Mbps, V_{DD1} = 3 V, Figure 5
		2.1		mA	16 Mbps, V_{DD1} = 3 V, Figure 5
Bus Side			3.0	mA	RTS = 0 V
		43.0		mA	2 Mbps, RTS = V_{DD1}, Figure 5
		58.0		mA	16 Mbps, RTS = V_{DD1}, Figure 5
COMMON-MODE TRANSIENT IMMUNITY[1]	25			kV/µs	V_{CM} = 1 kV, Transient Magnitude = 800 V
HIGH FREQUENCY COMMON-MODE NOISE IMMUNITY		100		mV	V_{HF} = +5V, −2 V < V_{TEST2} < 7 V, 1 < f_{TEST} < 50 MHz, Figure 6

[1] CM is the maximum common-mode voltage slew rate that can be sustained while maintaining specification-compliant operation. V_{CM} is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common-mode is slewed. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

TIMING SPECIFICATIONS

$2.7 \le V_{DD1} \le 5.5$ V, 4.75 V $\le V_{DD2} \le 5.25$ V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER					
Maximum Data Rate	16			Mbps	
Propagation Delay t_{PLH}, t_{PHL}	25	45	55	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF; See Figure 7.
RTS-to-DE Propagation Delay	20	35	55	ns	See Figure 8.
Pulse-Width Distortion, t_{PWD}			5	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF; See Figure 7 and Figure 12.
Switching Skew, t_{SKEW}		2	5	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF; See Figure 7 and Figure 12.
Rise/Fall Time t_R, t_F		5	15	ns	R_{LDIFF} = 54 Ω, C_{L1} = C_{L2} = 100 pF; See Figure 7 and Figure 12.
Enable Time		43	53	ns	See Figure 9 and Figure 14.
Disable Time		43	55	ns	See Figure 9 and Figure 14.
Enable Skew, $\lvert t_{AZH}-t_{BZL}\rvert$, $\lvert t_{AZL}-t_{BZH}\rvert$		1	3	ns	See Figure 9 and Figure 14.
Disable Skew, $\lvert t_{AHZ}-t_{BLZ}\rvert$, $\lvert t_{ALZ}-t_{BHZ}\rvert$		2	5	ns	See Figure 9 and Figure 14.
RECEIVER					
Propagation Delay t_{PLH}, t_{PHL}	25	45	55	ns	C_L = 15 pF; See Figure 10 and Figure 13.
Differential Skew t_{SKEW}			5	ns	C_L = 15 pF; See Figure 10 and Figure 13.
Enable Time		3	13	ns	R_L = 1 kΩ, C_L = 15 pF; See Figure 11 and Figure 15.
Disable Time		3	13	ns	R_L = 1 kΩ, C_L = 15 pF; See Figure 11 and Figure 15.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. All voltages are relative to their respective ground.

Table 3.

Parameter	Rating
V_{DD1}	−0.5 V to +6 V
V_{DD2}	−0.5 V to +6 V
Digital Input Voltage (RTS, $\overline{RE}$, TxD)	−0.5 V to V_{DD1} + 0.5 V
Digital Output Voltage	
RxD	−0.5 V to V_{DD1} + 0.5 V
DE OUT	−0.5 V to V_{DD2} + 0.5 V
Driver Output/Receiver Input Voltage	−9 V to +14 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +150°C
Average Output Current per Pin	−35 mA to +35 mA
θ_{JA} Thermal Impedance	73°C/W
Lead Temperature	
Soldering (10 sec)	300°C
Vapour Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ADM2485E CHARACTERISTICS

PACKAGE CHARACTERISTICS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input-Output)[1]	C_{I-O}		3		pF	f = 1 MHz
Input Capacitance[2]	C_I		4		pF	
Input IC Junction-to-Case Thermal Resistance	θ_{JCI}		33		°C/W	Thermocouple located at center of package underside
Output IC Junction-to-Case Thermal Resistance	θ_{JCO}		28		°C/W	

[1] Device considered a two-terminal device: Pins 1, 2, 3, 4, 5, 6, 7, and 8 shorted together, and Pins 9, 10, 11, 12, 13, 14, 15, and 16 shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADM2485 is to be approved by the following organizations:

Table 3.

Organization	Approval Type	Notes
UL	To be recognized under 1577 component recognition program.	In accordance with UL1577, each ADM2485 is proof-tested by applying an insulation test voltage ≥3000 V rms for 1 second (current leakage detection limit = 5 μA).
CSA	To be approved under CSA Component Acceptance Notice #5A.	
VDE	To be certified according to DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01	In accordance with VDE 0884, each ADM2485 is proof-tested by applying an insulation test voltage ≥1050 V_{PEAK} for 1 second (partial discharge detection limit = 5 pC).

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration.
Minimum External Air Gap (Clearance)	L(I01)	5.15 min	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(I02)	5.5 min	mm	Measured from input terminals to output terminals, shortest distance along body.
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1.
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89,).

VDE 0884 INSULATION CHARACTERISTICS

This isolator is suitable for basic electrical isolation only within the safety limit data. Maintenance of the safety data must be ensured by means of protective circuits.

An asterisk (*) on packages denotes VDE 0884 approval for 560 V peak working voltage.

Table 5.

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110 for rated mains voltage			
≤150 V rms		I to IV	
≤300 V rms		I to III	
≤400 V rms		I to II	
Climatic classification		40/85/21	
Pollution degree (DIN VDE 0110, Table 1)		2	
Maximum working insulation voltage	V_{IORM}	560	V_{PEAK}
Input to output test voltage, Method b1	V_{PR}	1050	V_{PEAK}
$V_{IORM} \times 1.875 = V_{PR}$, 100% production tested, t_m = 1 sec, partial discharge < 5 pC			
Input to output test voltage, Method a			
(After environmental tests, Subgroup 1)			
$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC		896	V_{PEAK}
(After input and/or safety test, Subgroup 2/3)			
$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC	V_{PR}	672	V_{PEAK}
Highest allowable overvoltage			
(Transient overvoltage, t_{TR} = 10 sec)	V_{TR}	4000	V_{PEAK}
Safety-limiting values (maximum value allowed in the event of a failure. See thermal derating curve)			
Case temperature	T_S	150	°C
Input current	$I_{S, INPUT}$	265	mA
Output current	$I_{S, OUTPUT}$	335	mA
Insulation resistance at Ts, V_{IO} = 500 V	Rs	$>10^9$	Ω

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

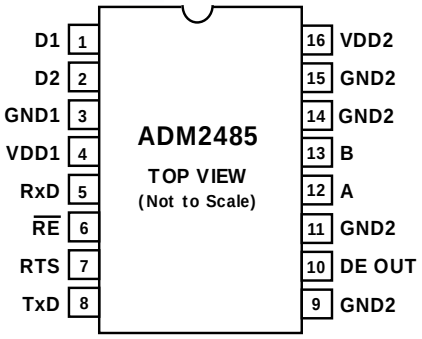

Figure 2. Pin Configuration

Table 4.

Pin	Mnemonic	Function
1	D1	Transformer driver terminal 1.
2	D2	Transformer driver terminal 2.
3	GND_1	Ground, Logic Side.
4	V_{DD1}	Power Supply Logic Side, 3V or 5V. Decoupling capacitor to GND_1 required, capacitor value should be between 0.01 µF and 0.1 µF.
5	RxD	Receiver Output data. This output is high when (A – B) > 200 mV, and low when (A – B) < -200 mV. The output is tri-stated when the receiver is disabled, i.e. when $\overline{RE}$ is driven high.
6	$\overline{RE}$	Receiver Enable input. This is an active-low input. Driving this input low enables the receiver, while driving it high disables the receiver.
7	RTS	Driver enable input. Driving this input high enables the driver, while driving it low disables the driver.
8	TxD	Driver input. Data to be transmitted by the driver is applied to this input.
10	DE OUT	Driver Enable status output
12	A	Noninverting Driver Output/Receiver Input. When the driver is disabled or V_{DD1} or V_{DD2} is powered down, pin A is put in a high impedance state to avoid overloading the bus.
13	B	Inverting Driver Output/Receiver Input. When the driver is disabled or V_{DD1} or V_{DD2} is powered down, pin B is put in a high impedance state to avoid overloading the bus.
9,11,14,15	GND_2	Ground, Bus Side.
16	V_{DD2}	Power Supply Bus Side, Isolated 5V supply. Decoupling capacitor to GND_2 required, capacitor value should be between 0.01 µF and 0.1 µF.

TEST CIRCUITS

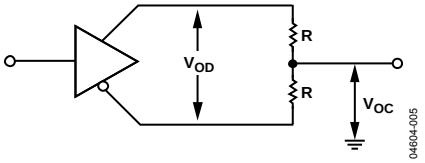

Figure 3. Driver Voltage Measurement

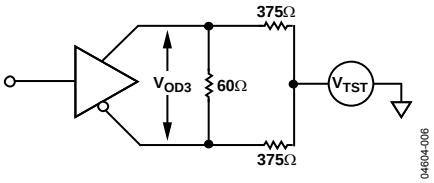

Figure 4. Driver Voltage Measurement

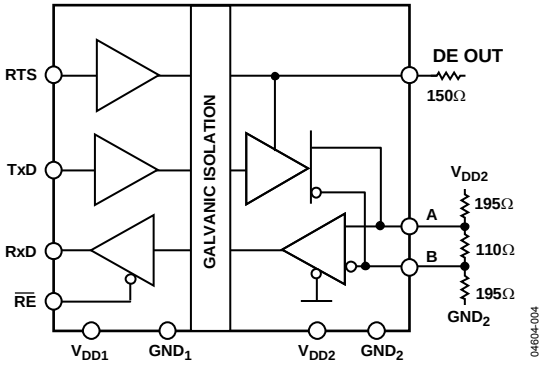

Figure 5. Supply-Current Measurement Test Circuit

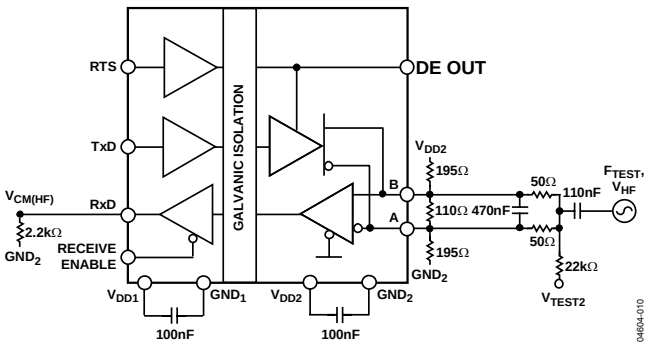

Figure 6. High Frequency Common-Mode Noise Test Circuit

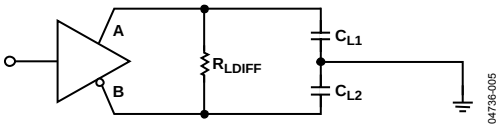

Figure 7. Driver Propagation Delay

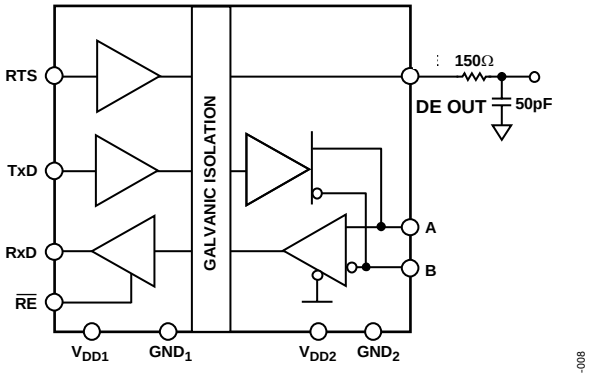

Figure 8. RTS to DE OUT Propagation Delay

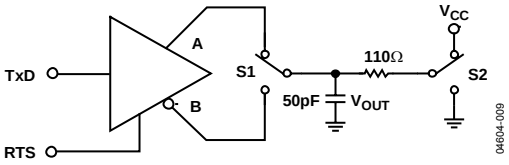

Figure 9. Driver Enable/Disable

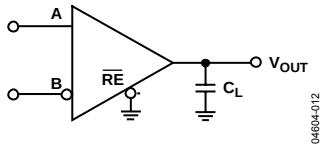

Figure 10. Receiver Propagation Delay

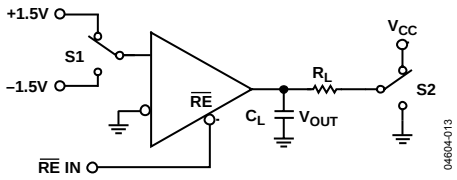

Figure 11. Receiver Enable/Disable

SWITCHING CHARACTERISTICS

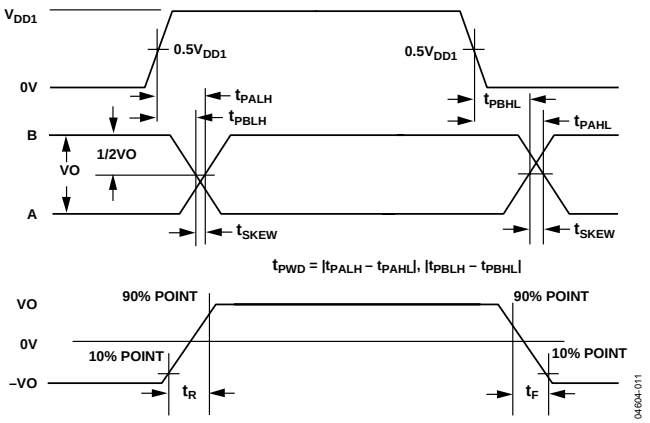

Figure 12. Driver Propagation Delay, Rise/Fall Timing

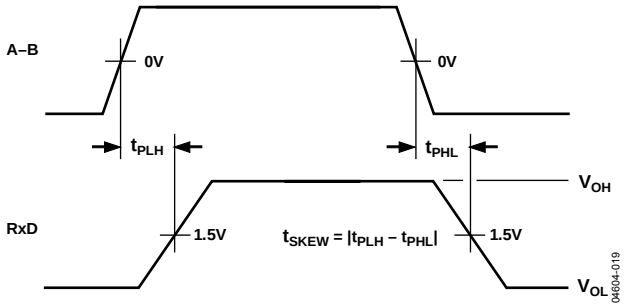

Figure 13. Receiver Propagation Delay

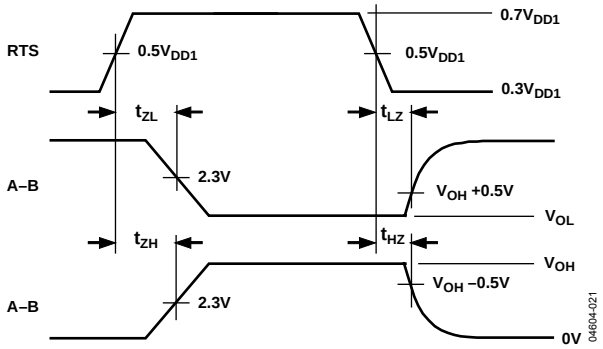

Figure 14. Driver Enable/Disable Timing

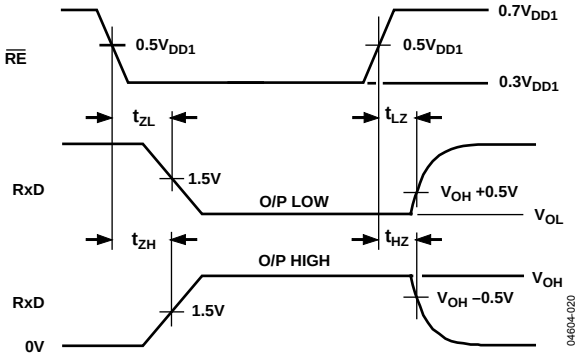

Figure 15. Receiver Enable/Disable Timing

CIRCUIT DESCRIPTION

ELECTRICAL ISOLATION

In the ADM2485, electrical isolation is implemented on the logic side of the interface. Therefore, the part has two main sections: a digital isolation section and a transceiver section (see Figure 16). Driver input and data enable, applied to the TxD and RTS pins, respectively, and referenced to logic ground (GND_1), are coupled across an isolation barrier to appear at the transceiver section referenced to isolated ground (GND_2). Similarly, the receiver output, referenced to isolated ground in the transceiver section, is coupled across the isolation barrier to appear at the RxD pin referenced to logic ground.

*i*Coupler Technology

The digital signals are transmitted across the isolation barrier using *i*Coupler technology. This technique uses chip scale transformer windings to couple the digital signals magnetically from one side of the barrier to the other. Digital inputs are encoded into waveforms that are capable of exciting the primary transformer winding. At the secondary winding, the induced waveforms are then decoded into the binary value that was originally transmitted.

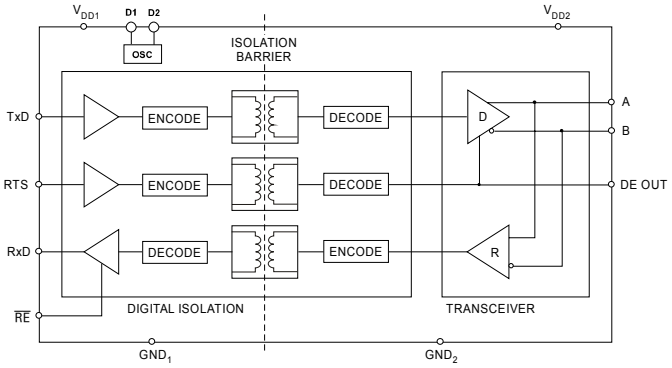

Figure 16. ADM2485 Digital Isolation and Transceiver Sections

TRUTH TABLES

The truth tables in this section use these abbreviations:

Letter	Description
H	High level
I	Indeterminate
L	Low level
X	Irrelevant
Z	High impedance (off)
NC	Disconnected

Table 6. Transmitting

Supply Status		Inputs		Output		
V_{DD1}	V_{DD2}	RTS	TxD	A	B	DE OUT
On	On	H	H	H	L	H
On	On	H	L	L	H	H
On	On	L	X	Z	Z	L
On	Off	X	X	Z	Z	L
Off	On	X	X	Z	Z	L
Off	Off	X	X	Z	Z	L

Table 7. Receiving

Supply Status		Inputs		Output
V_{DD1}	V_{DD2}	A–B (V)	$\overline{RE}$	RxD
On	On	>0.2	L or NC	H
On	On	<–0.2	L or NC	L
On	On	–0.2 < A – B < 0.2	L or NC	I
On	On	Inputs open	L or NC	H
On	On	X	H	Z
On	Off	X	L or NC	H
Off	On	X	L or NC	H
Off	Off	X	L or NC	L

THERMAL SHUTDOWN

The ADM2485 contains thermal shutdown circuitry that protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. This circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are re-enabled at a temperature of 140°C.

RECEIVER FAIL-SAFE INPUTS

The receiver input includes a fail-safe feature that guarantees a logic high RxD output when the A and B inputs are floating or open-circuited.

MAGNETIC FIELD IMMUNITY

Because *i*Couplers use a coreless technology, no magnetic components are present, and the problem of magnetic saturation of the core material does not exist. Therefore, *i*Couplers have essentially infinite dc field immunity. The analysis below defines the conditions under which this may occur. The ADM2485's 3 V operating condition is examined because it represents the most susceptible mode of operation.

The limitation on the iCoupler's ac magnetic field immunity is set by the condition in which the induced error voltage in the receiving coil (the bottom coil in this case) is made sufficiently large, either to falsely set or reset the decoder. The voltage induced across the bottom coil is given by

$$V = \left(\frac{-d\beta}{dt}\right)\sum \pi r_n^2 \; ; \; n = 1, 2, \ldots, N$$

where, if the pulses at the transformer output are greater than 1.0 V in amplitude:
β = magnetic flux density (gauss)
N = number of turns in receiving coil
r_n = radius of nth turn in receiving coil (cm)

The decoder has a sensing threshold of about 0.5 V; therefore, there is a 0.5 V margin in which induced voltages can be tolerated.

Given the geometry of the receiving coil and an imposed requirement that the induced voltage is, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 17.

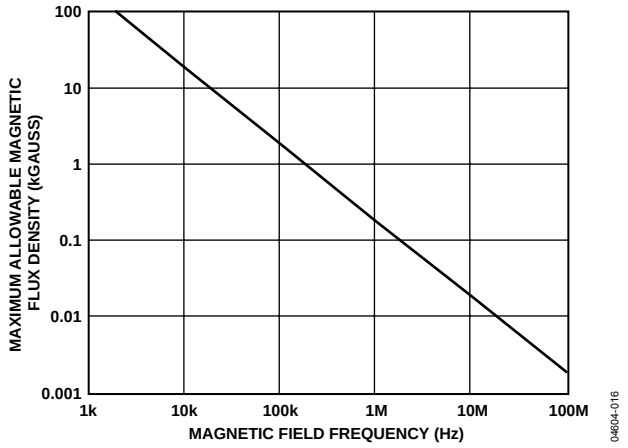

Figure 17. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kGauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse and is the worst-case polarity, it reduces the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

Figure 18 shows the magnetic flux density values in terms of more familiar quantities such as maximum allowable current flow at given distances away from the ADM2485 transformers.

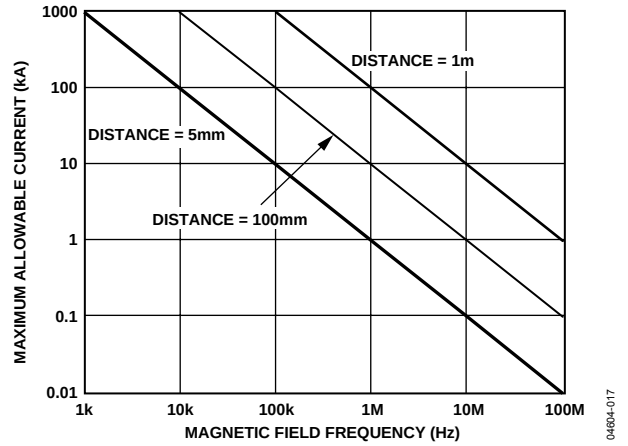

Figure 18. Maximum Allowable Current for Various Current-to-ADM2485 Spacings

At combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

APPLICATIONS INFORMATION

PC BOARD LAYOUT

The ADM2485 isolated RS-485 transceiver requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure).

Bypass capacitors are most conveniently connected between Pin 3 and Pin 4 for V_{DD1} and between Pin 15 and Pin 16 for V_{DD2}. The capacitor value should be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm.

Bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 should also be considered unless the ground pair on each package side is connected close to the package.

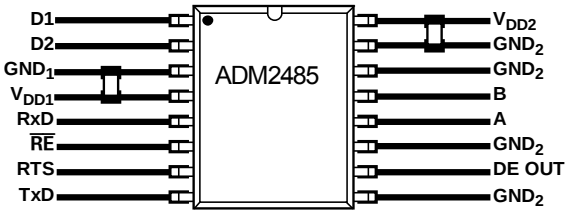

Figure 19. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, care should be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed such that any coupling that does occur equally affects all pins on a given component side.

Failure to ensure this could cause voltage differentials between pins exceeding the device's absolute maximum ratings, thereby leading to latch-up or permanent damage.

APPLICATIONS DIAGRAM

The ADM2485 integrates a transformer driver which when used with an external transformer and LDO generates an isolated 5V power supply, to be supplied between the V_{DD2} and the GND_2 pins.

Pins D1 and D2 of the ADM2485 drive a center-tapped transformer T1, A pair of Schottky diodes and a smoothing capacitor are used to create a rectified signal from the secondary winding. The ADP667 linear voltage regulator provides a regulated 5V power supply to the ADM2485's bus-side circuitry (V_{DD2}), as shown in Figure 20.

When the ADM2485 is powered by 3V on the logic side a 1CT:2.2CT transformer T1 is required to step up the 3V to 6V, so that therefore is enough headroom for the ADP667 LDO to output a regulated 5V output.

If ADM2485 is powered by 5V on the logic side a 1CT:1.5CT transformer T1 is required so that therefore is enough headroom for the ADP667 LDO to output a regulated 5V output.

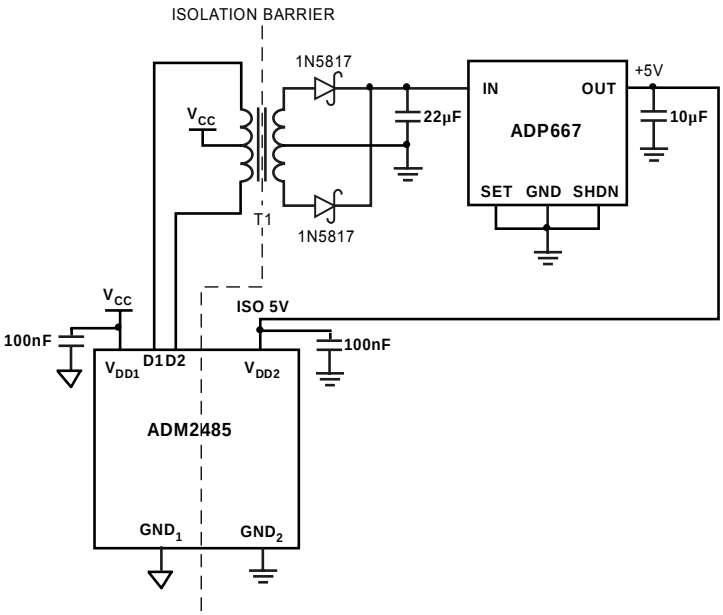

Figure 20. Applications Diagram

OUTLINE DIMENSIONS

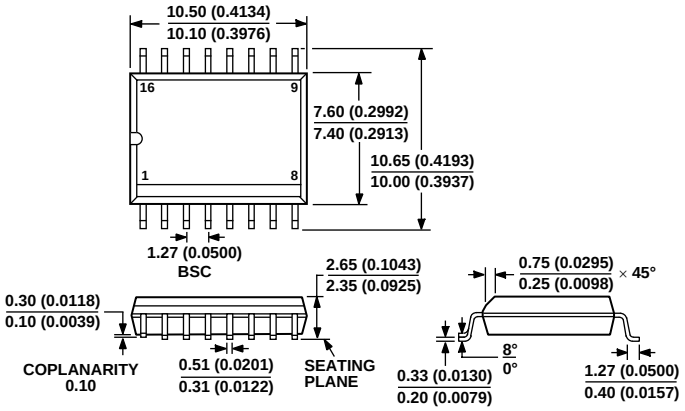

Figure 21. 16-Lead Wide-Body Small Outline Package [SOIC]

(RW-16)

Dimensions shown in millimeters

ORDERING GUIDE

Model	Data Rate (Mbps)	Temperature Range	Package Description	Package Option
ADM2485BRWZ[1]	16	–40°C to +85°C	16-Lead Wide Body SOIC	RW-16
ADM2485BRWZ-REEL[1]	16	–40°C to +85°C	16-Lead Wide Body SOIC	RW-16

The addition of an "-RL" suffix designates a 13" (1000 units) tape and reel option.

[1] Z = Pb-free part.

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