

### FEATURES

Enhanced system-level ESD performance per IEC 61000-4-x

High data rate: dc to 100 Mbps (NRZ)

Compatible with 3.3 V and 5.0 V operation/level translation

105°C maximum operating temperature

Low power operation

5 V operation

2.0 mA maximum @ 1 Mbps

5.6 mA maximum @ 25 Mbps

18 mA maximum @ 100 Mbps

3.3 V operation

1.1 mA maximum @ 1 Mbps

4.2 mA maximum @ 25 Mbps

8.3 mA maximum @ 50 Mbps

8-lead SOIC, Pb-free package

High common-mode transient immunity: >25 kV/μs

Safety and regulatory information

UL recognized: 2500 V rms for 1 minute per UL 1577

CSA Component Acceptance Notice #5A

VDE Certificate of Conformity

DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01

DIN EN 60950 (VDE 0805): 2001-12; EN 60950: 2000

$V_{IORM} = 560 V_{PEAK}$

### GENERAL DESCRIPTION

The ADuM3100<sup>1</sup> is a digital isolator based on Analog Devices *iCoupler*<sup>®</sup> technology. Combining high speed CMOS and monolithic transformer technology, this isolation component provides outstanding performance characteristics superior to alternatives, such as optocoupler devices.

Configured as a pin-compatible replacement for existing high speed optocouplers, the ADuM3100 supports data rates as high as 25 Mbps and 100 Mbps.

The ADuM3100 operates with a voltage supply ranging from 3.0 V to 5.5 V, boasts a propagation delay of <18 ns and an edge asymmetry of <2 ns, and is compatible with temperatures up to 105°C. It operates at very low power, less than 2.0 mA of quiescent current (sum of both sides), and a dynamic current of less than 160 μA per Mbps of data rate. Unlike other optocoupler alternatives, the ADuM3100 provides dc correctness with a patented refresh feature that continuously updates the output signal.

#### Rev. A

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### APPLICATIONS

Digital fieldbus isolation

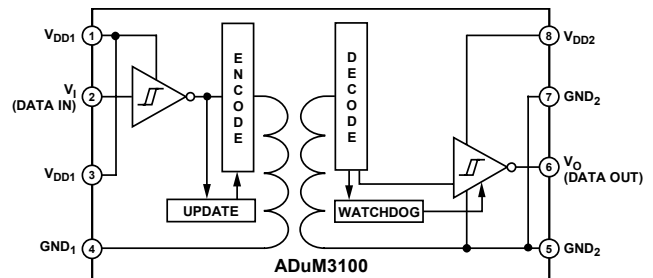
Opto-isolator replacement

Computer-peripheral interface

Microprocessor system interface

General instrumentation and data acquisition

### FUNCTIONAL BLOCK DIAGRAM



NOTES  
1. FOR PRINCIPLES OF OPERATION, SEE METHOD OF OPERATION, DC CORRECTNESS, AND MAGNETIC FIELD IMMUNITY SECTION.

Figure 1.

The ADuM3100 is offered in two grades. The ADuM3100AR and ADuM3100BR can operate up to a maximum temperature of 105°C and support data rates up to 25 Mbps and 100 Mbps, respectively.

In comparison to the ADuM1100 digital isolator, the ADuM3100 contains various circuit and layout changes to provide increased capability relative to system-level IEC 61000-4-x testing (ESD/burst/surge). The precise capability in these tests for either the ADuM1100 or ADuM3100 is strongly determined by the design and layout of the user's board or module. For more information, see [Application Note AN-793, ESD/Latch-Up Considerations with \*iCoupler\* Isolation Products](#).

<sup>1</sup> Protected by U.S. Patents 5,952,849; 6,525,566; 6,922,080; 6,903,578; 6,873,065; and other pending patents.

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## REVISION HISTORY

### 3/06—Rev. 0 to Rev. A

Updated Format.....	Universal
Changes to Product Title, Features, General Description, and Note 1.....	1
Changes to Table 1.....	3
Changes to Table 2.....	4
Changes to Table 3.....	5
Added System-Level ESD Considerations and Enhancements Section.....	13
Added Power Consumption Section.....	15

### 10/05—Revision 0: Initial Version

## ELECTRICAL SPECIFICATIONS, 5 V OPERATION<sup>1</sup>

4.5 V ≤ V<sub>DD1</sub> ≤ 5.5 V, 4.5 V ≤ V<sub>DD2</sub> ≤ 5.5 V. All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T<sub>A</sub> = 25°C, V<sub>DD1</sub> = V<sub>DD2</sub> = 5 V.

**Table 1.**

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>DC SPECIFICATIONS</b>						
Input Supply Current, Quiescent	I <sub>DD1 (Q)</sub>		1.3	1.8	mA	V <sub>I</sub> = 0 V or V <sub>DD1</sub>
Output Supply Current, Quiescent	I <sub>DD2 (Q)</sub>		0.15	0.25	mA	V <sub>I</sub> = 0 V or V <sub>DD1</sub>
Input Supply Current (25 Mbps) (See Figure 4)	I <sub>DD1 (25)</sub>		3.2	4.5	mA	12.5 MHz logic signal freq.
Output Supply Current <sup>2</sup> (25 Mbps) (See Figure 5)	I <sub>DD2 (25)</sub>		0.6	1.1	mA	12.5 MHz logic signal freq.
Input Supply Current (100 Mbps) (See Figure 4)	I <sub>DD1 (100)</sub>		10	15	mA	50 MHz logic signal freq.
Output Supply Current <sup>2</sup> (100 Mbps) (See Figure 5)	I <sub>DD2 (100)</sub>		2.1	2.9	mA	50 MHz logic signal freq., ADuM3100BR only
Input Current	I <sub>I</sub>	-10	+0.01	+10	μA	0 ≤ V <sub>IN</sub> ≤ V <sub>DD1</sub>
Logic High Output Voltage	V <sub>OH</sub>	V <sub>DD2</sub> - 0.1	5.0		V	I <sub>O</sub> = -20 μA, V <sub>I</sub> = V <sub>IH</sub>
		V <sub>DD2</sub> - 0.8	4.6		V	I <sub>O</sub> = -4 mA, V <sub>I</sub> = V <sub>IH</sub>
Logic Low Output Voltage	V <sub>OL</sub>		0.0	0.1	V	I <sub>O</sub> = 20 μA, V <sub>I</sub> = V <sub>IL</sub>
			0.03	0.1	V	I <sub>O</sub> = 400 μA, V <sub>I</sub> = V <sub>IL</sub>
			0.3	0.8	V	I <sub>O</sub> = 4 mA, V <sub>I</sub> = V <sub>IL</sub>
<b>SWITCHING SPECIFICATIONS</b>						
For ADuM3100AR						
Minimum Pulse Width <sup>3</sup>	PW			40	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate <sup>4</sup>		25			Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
For ADuM3100BR						
Minimum Pulse Width <sup>4</sup>	PW		6.7	10	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate <sup>4</sup>		100	150		Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
For All Grades						
Propagation Delay Time to Logic Low Output <sup>5, 6</sup> (See Figure 6)	t <sub>PHL</sub>		10.5	18	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Time to Logic High Output <sup>5, 6</sup> (See Figure 6)	t <sub>PLH</sub>		10.5	18	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Pulse-Width Distortion  t <sub>PLH</sub> - t <sub>PHL</sub>   <sup>6</sup>	PWD		0.5	2	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Change vs. Temperature <sup>7</sup>			3		ps/°C	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew (Equal Temperature) <sup>6, 8</sup>	t <sub>PSK1</sub>			8	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew (Equal Temperature, Supplies) <sup>6, 8</sup>	t <sub>PSK2</sub>			6	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Output Rise/Fall Time	t <sub>r</sub> , t <sub>f</sub>		3		ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic Low/High Output <sup>9</sup>	C <sub>ML</sub>  ,  C <sub>MH</sub>	25	35		kV/μs	V <sub>I</sub> = 0 or V <sub>DD1</sub> , V <sub>CM</sub> = 1000 V
Input Dynamic Supply Current <sup>10</sup>	I <sub>DDI (D)</sub>		0.09		mA/Mbps	
Output Dynamic Supply Current <sup>10</sup>	I <sub>DDO (D)</sub>		0.02		mA/Mbps	

See notes on Page 6.

## ELECTRICAL SPECIFICATIONS, 3.3 V OPERATION<sup>1</sup>

3.0 V ≤ V<sub>DD1</sub> ≤ 3.6 V, 3.0 V ≤ V<sub>DD2</sub> ≤ 3.6 V. All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T<sub>A</sub> = 25°C, V<sub>DD1</sub> = V<sub>DD2</sub> = 3.3 V.

**Table 2.**

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>DC SPECIFICATIONS</b>						
Input Supply Current, Quiescent	I <sub>DD1 (Q)</sub>		0.7	0.9	mA	V <sub>I</sub> = 0 V or V <sub>DD1</sub>
Output Supply Current, Quiescent	I <sub>DD2 (Q)</sub>		0.1	0.2	mA	V <sub>I</sub> = 0 V or V <sub>DD1</sub>
Input Supply Current (25 Mbps) (See Figure 4)	I <sub>DD1 (25)</sub>		2.6	3.4	mA	12.5 MHz logic signal freq.
Output Supply Current <sup>2</sup> (25 Mbps) (See Figure 5)	I <sub>DD2 (25)</sub>		0.4	0.8	mA	12.5 MHz logic signal freq.
Input Supply Current (50 Mbps) (See Figure 4)	I <sub>DD1 (50)</sub>		4.6	6.6	mA	25 MHz logic signal freq., ADuM3100BR only
Output Supply Current <sup>2</sup> (50 Mbps) (See Figure 5)	I <sub>DD2 (50)</sub>		0.7	1.7	mA	25 MHz logic signal freq., ADuM3100BR only
Input Current	I <sub>I</sub>	-10	+0.01	+10	μA	0 ≤ V <sub>IN</sub> ≤ V <sub>DD1</sub>
Logic High Output Voltage	V <sub>OH</sub>	V <sub>DD2</sub> - 0.1	3.3		V	I <sub>O</sub> = -20 μA, V <sub>I</sub> = V <sub>IH</sub>
		V <sub>DD2</sub> - 0.5	3.0		V	I <sub>O</sub> = -2.5 mA, V <sub>I</sub> = V <sub>IH</sub>
Logic Low Output Voltage	V <sub>OL</sub>		0.0	0.1	V	I <sub>O</sub> = 20 μA, V <sub>I</sub> = V <sub>IL</sub>
			0.04	0.1	V	I <sub>O</sub> = 400 μA, V <sub>I</sub> = V <sub>IL</sub>
			0.3	0.4	V	I <sub>O</sub> = 2.5 mA, V <sub>I</sub> = V <sub>IL</sub>
<b>SWITCHING SPECIFICATIONS</b>						
For ADuM3100AR						
Minimum Pulse Width <sup>3</sup>	PW			40	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate <sup>4</sup>		25			Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
For ADuM3100BR						
Minimum Pulse Width <sup>3</sup>	PW		10	20	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Maximum Data Rate <sup>4</sup>		50	100		Mbps	C <sub>L</sub> = 15 pF, CMOS signal levels
For All Grades						
Propagation Delay Time to Logic Low Output <sup>5,6</sup> (See Figure 7)	t <sub>PHL</sub>		14.5	28	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Time to Logic High Output <sup>5,6</sup> (See Figure 7)	t <sub>PLH</sub>		15.0	28	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Pulse-Width Distortion  t <sub>PLH</sub> - t <sub>PHL</sub>   <sup>6</sup> Change vs. Temperature <sup>7</sup>	PWD		0.5	3	ns ps/°C	C <sub>L</sub> = 15 pF, CMOS signal levels C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew (Equal Temperature) <sup>6,8</sup>	t <sub>PSK1</sub>			15	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew (Equal Temperature, Supplies) <sup>6,8</sup>	t <sub>PSK2</sub>			12	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Output Rise/Fall Time	t <sub>R</sub> , t <sub>F</sub>		3		ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic Low/High Output <sup>9</sup>	CM <sub>L</sub>  ,  CM <sub>H</sub>	25	35		kV/μs	V <sub>I</sub> = 0 or V <sub>DD1</sub> , V <sub>CM</sub> = 1000 V, transient magnitude = 800 V
Input Dynamic Supply Current <sup>10</sup>	I <sub>DD1 (D)</sub>		0.08		mA/Mbps	
Output Dynamic Supply Current <sup>10</sup>	I <sub>DDO (D)</sub>		0.01		mA/Mbps	

See notes on Page 6.

## ELECTRICAL SPECIFICATIONS, MIXED 5 V/3 V OR 3 V/5 V OPERATION<sup>1</sup>

5 V/3 V operation:  $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$ ,  $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$ . 3 V/5 V operation:  $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$ ,  $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$ . All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD1} = 3.3\text{ V}$ ,  $V_{DD2} = 5\text{ V}$  or  $V_{DD1} = 5\text{ V}$ ,  $V_{DD2} = 3.3\text{ V}$ .

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>DC SPECIFICATIONS</b>						
Input Supply Current, Quiescent	$I_{DD1(Q)}$		1.3	1.8	mA	
5 V/3 V Operation			0.7	0.9	mA	
3 V/5 V Operation						
Output Supply Current <sup>2</sup> , Quiescent	$I_{DDO(Q)}$		0.1	0.2	mA	
5 V/3 V Operation			0.15	0.25	mA	
3 V/5 V Operation						
Input Supply Current, 25 Mbps	$I_{DD1(25)}$		3.2	4.5	mA	12.5 MHz logic signal freq.
5 V/3 V Operation			2.6	3.4	mA	12.5 MHz logic signal freq.
3 V/5 V Operation						
Output Supply Current <sup>2</sup> , 25 Mbps	$I_{DDO(25)}$		0.4	0.8	mA	12.5 MHz logic signal freq.
5 V/3 V Operation			0.6	1.1	mA	12.5 MHz logic signal freq.
3 V/5 V Operation						
Input Supply Current, 50 Mbps	$I_{DD1(50)}$		5.5	8.0	mA	25 MHz logic signal freq.
5 V/3 V Operation			4.6	6.6	mA	25 MHz logic signal freq.
3 V/5 V Operation						
Output Supply Current <sup>2</sup> , 50 Mbps	$I_{DDO(50)}$		0.7	1.7	mA	25 MHz logic signal freq.
5 V/3 V Operation			1.1	1.6	mA	25 MHz logic signal freq.
3 V/5 V Operation						
Input Currents	$I_{IA}$	-10	+0.01	+10	$\mu\text{A}$	$0 \leq V_{IA}, V_{IB}, V_{IC}, V_{ID} \leq V_{DD1}$ or $V_{DD2}$
Logic High Output Voltage, 5 V/3 V Operation	$V_{OH}$	$V_{DD2} - 0.1$	3.3		V	$I_O = -20\text{ }\mu\text{A}$ , $V_I = V_{IH}$
		$V_{DD2} - 0.5$	3.0		V	$I_O = -2.5\text{ mA}$ , $V_I = V_{IH}$
Logic Low Output Voltage, 5 V/3 V Operation	$V_{OL}$		0.0	0.1	V	$I_O = 20\text{ }\mu\text{A}$ , $V_I = V_{IL}$
			0.04	0.1	V	$I_O = 400\text{ }\mu\text{A}$ , $V_I = V_{IL}$
			0.3	0.4	V	$I_O = 2.5\text{ mA}$ , $V_I = V_{IL}$
Logic High Output Voltage, 3 V/5 V Operation	$V_{OH}$	$V_{DD2} - 0.1$	5.0		V	$I_O = -20\text{ }\mu\text{A}$ , $V_I = V_{IH}$
		$V_{DD2} - 0.8$	4.6		V	$I_O = -4\text{ mA}$ , $V_I = V_{IH}$
Logic Low Output Voltage, 3 V/5 V Operation	$V_{OL}$		0.0	0.1	V	$I_O = 20\text{ }\mu\text{A}$ , $V_I = V_{IL}$
			0.03	0.1	V	$I_O = 400\text{ }\mu\text{A}$ , $V_I = V_{IL}$
			0.3	0.8	V	$I_O = 4\text{ mA}$ , $V_I = V_{IL}$
<b>SWITCHING SPECIFICATIONS</b>						
For ADuM3100AR						
Minimum Pulse Width <sup>3</sup>	PW			40	ns	$C_L = 15\text{ pF}$ , CMOS signal levels
Maximum Data Rate <sup>4</sup>		25			Mbps	$C_L = 15\text{ pF}$ , CMOS signal levels
For ADuM3100BR						
Minimum Pulse Width <sup>3</sup>	PW			20	ns	$C_L = 15\text{ pF}$ , CMOS signal levels
Maximum Data Rate <sup>4</sup>		50			Mbps	$C_L = 15\text{ pF}$ , CMOS signal levels
For All Grades						
Propagation Delay Time to Logic Low/ High Output <sup>5,6</sup>	$t_{PHL}$ , $t_{PLH}$					
5 V/3 V Operation (See Figure 8)			13	21	ns	$C_L = 15\text{ pF}$ , CMOS signal levels
3 V/5 V Operation (See Figure 9)			16	26	ns	$C_L = 15\text{ pF}$ , CMOS signal levels
Pulse-Width Distortion, $ t_{PLH} - t_{PHL} ^6$	PWD					
5 V/3 V Operation			0.5	2	ns	$C_L = 15\text{ pF}$ , CMOS signal levels
3 V/5 V Operation			0.5	3	ns	$C_L = 15\text{ pF}$ , CMOS signal levels

# ADuM3100

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Change vs. Temperature <sup>7</sup>						
5 V/3 V Operation			3		ps/°C	C <sub>L</sub> = 15 pF, CMOS signal levels
3 V/5 V Operation			10		ps/°C	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew (Equal Temperature) <sup>6,8</sup>	t <sub>PSK1</sub>					
5 V/3 V Operation				12	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
3 V/5 V Operation				15	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Propagation Delay Skew (Equal Temperature, Supplies) <sup>6,8</sup>	t <sub>PSK2</sub>					
5 V/3 V Operation				9	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
3 V/5 V Operation				12	ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t <sub>R</sub> , t <sub>F</sub>		3		ns	C <sub>L</sub> = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic Low/High Output <sup>9</sup>	CM <sub>L</sub>  ,  CM <sub>H</sub>	25	35		kV/μs	V <sub>I</sub> = 0 or V <sub>DD1</sub> , V <sub>CM</sub> = 1000 V, transient magnitude = 800 V
Input Dynamic Supply Current per Channel <sup>10</sup>	I <sub>DDI (D)</sub>					
5 V/3 V Operation			0.09		mA/Mbps	
3 V/5 V Operation			0.08		mA/Mbps	
Output Dynamic Supply Current per Channel <sup>10</sup>	I <sub>DDO (D)</sub>					
5 V/3 V Operation			0.01		mA/Mbps	
3 V/5 V Operation			0.02		mA/Mbps	

<sup>1</sup> All voltages are relative to their respective ground.

<sup>2</sup> Output supply current values are with no output load present. See Figure 4 and Figure 5 for information on supply current variation with logic signal frequency. See the Power Consumption section for guidance on calculating the input and output supply currents for a given data rate and output load.

<sup>3</sup> The minimum pulse width is the shortest pulse width at which the specified pulse-width distortion is guaranteed.

<sup>4</sup> The maximum data rate is the fastest data rate at which the specified pulse-width distortion is guaranteed.

<sup>5</sup> t<sub>PHL</sub> is measured from the 50% level of the falling edge of the V<sub>I</sub> signal to the 50% level of the falling edge of the V<sub>O</sub> signal. t<sub>PLH</sub> is measured from the 50% level of the rising edge of the V<sub>I</sub> signal to the 50% level of the rising edge of the V<sub>O</sub> signal.

<sup>6</sup> Because the input thresholds of the ADuM3100 are at voltages other than the 50% level of typical input signals, the measured propagation delay and pulse-width distortion can be affected by slow input rise/fall times. See the System-Level ESD Considerations and Enhancements section and Figure 13 to Figure 17 for information on the impact of given input rise/fall times on these parameters.

<sup>7</sup> Pulse-width distortion change vs. temperature is the absolute value of the change in pulse-width distortion for a 1°C change in operating temperature.

<sup>8</sup> t<sub>PSK1</sub> is the magnitude of the worst-case difference in t<sub>PHL</sub> and/or t<sub>PLH</sub> that is measured between units at the same operating temperature and output load within the recommended operating conditions. t<sub>PSK2</sub> is the magnitude of the worst-case difference in t<sub>PHL</sub> and/or t<sub>PLH</sub> that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

<sup>9</sup> CM<sub>H</sub> is the maximum common-mode voltage slew rate that can be sustained while maintaining V<sub>O</sub> > 0.8 V<sub>DD2</sub>. CM<sub>L</sub> is the maximum common-mode voltage slew rate that can be sustained while maintaining V<sub>O</sub> < 0.8 V. The common-mode voltage slew rates apply to both rising and falling edges. The transient magnitude is the range over which the common-mode is slewed.

<sup>10</sup> Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 4 and Figure 5 for information on supply current variation with logic signal frequency. See the Power Consumption section for guidance on calculating the input and output supply currents for a given data rate and output load.

## PACKAGE CHARACTERISTICS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-to-Output) <sup>1</sup>	R <sub>I-O</sub>		10 <sup>12</sup>		Ω	f = 1 MHz  Thermocouple located at center underside of package
Capacitance (Input-to-Output) <sup>1</sup>	C <sub>I-O</sub>		1		pF	
Input Capacitance <sup>2</sup>	C <sub>I</sub>		4.0		pF	
Input IC Junction-to-Case Thermal Resistance	θ <sub>JCI</sub>		46		°C/W	
Output IC Junction-to-Case Thermal Resistance	θ <sub>JCO</sub>		41		°C/W	
Package Power Dissipation	PPD			240	mW	

<sup>1</sup> Device considered a 2-terminal device: Pin 1, Pin 2, Pin 3, and Pin 4 shorted together, and Pin 5, Pin 6, Pin 7, and Pin 8 shorted together.

<sup>2</sup> Input capacitance is measured at Pin 2 (Vi).

## REGULATORY INFORMATION

The ADuM3100 is approved by the organizations listed in Table 5.

Table 5.

UL	CSA	VDE
Recognized under 1577 Component Recognition Program <sup>1</sup>  File E214100	Approved under CSA Component Acceptance Notice No. 5A, C22.2 No. 1-98, C22.2 No. 14-95, and C22.2 No. 950-95  File 205078	Certified according to DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01 <sup>2</sup> DIN EN 60950 (VDE 0805): 2001-12; EN 60950: 2000 File 2471900-4880-0002

<sup>1</sup>In accordance with UL 1577, each ADuM3100 is proof tested by applying an insulation test voltage  $\geq 3000$  V rms for 1 second (leakage detection current limit,  $I_{I-O} \leq 5 \mu\text{A}$ ).

<sup>2</sup>In accordance with DIN EN 60747-5-2, each ADuM3100 is proof tested by applying an insulation test voltage  $\geq 1050 V_{\text{PEAK}}$  for 1 second (partial discharge detection limit  $\leq 5$  pC). An asterisk (\*) branded on the component designates DIN EN 60747-5-2 approval.

## INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 6.

Parameter	Symbol	Value	Unit	Conditions
Minimum External Air Gap (Clearance)	L(I01)	4.90 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	4.01 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

## DIN EN 60747-5-2 (VDE 0884 PART 2) INSULATION CHARACTERISTICS

Table 7.

Description	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110 For Rated Mains Voltage ≤ 150 V rms For Rated Mains Voltage ≤ 300 V rms For Rated Mains Voltage ≤ 400 V rms		I to IV I to III I to II	
Climatic Classification		40/105/21	
Pollution Degree (DIN VDE 0110, Table 5)		2	
Maximum Working Insulation Voltage	$V_{IORM}$	560	$V_{PEAK}$
Input-to-Output Test Voltage, Method b1 $V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test, $t_M = 1$ sec, Partial Discharge <5 pC	$V_{PR}$	1050	$V_{PEAK}$
Input-to-Output Test Voltage, Method a	$V_{PR}$	672	$V_{PEAK}$
After Environmental Tests Subgroup 1 $V_{IORM} \times 1.6 = V_{PR}$ , $t_M = 10$ sec, Partial Discharge <5 pC	$V_{PR}$	896	$V_{PEAK}$
After Input and/or Output Safety Test Subgroup 2/3 $V_{IORM} \times 1.2 = V_{PR}$ , $t_M = 10$ sec, Partial Discharge <5 pC	$V_{PR}$	672	$V_{PEAK}$
Highest Allowable Overvoltage (Transient Overvoltage, $t_{INI} = 60$ sec)	$V_{TR}$	4000	$V_{PEAK}$
Safety-Limiting Values (Maximum Value Allowed in the Event of a Failure, See Figure 2)			
Case Temperature	$T_S$	150	°C
Input Current	$I_S, INPUT$	160	mA
Output Current	$I_S, OUTPUT$	170	mA
Insulation Resistance at $T_S$ , $V_{IO} = 500$ V	$R_S$	$>10^9$	$\Omega$

This isolator is suitable for basic isolation only within the safety limit data. Maintenance of the safety data is ensured by means of protective circuits. The asterisk (\*) on the package denotes DIN EN 60747-5-2 approval for 560  $V_{PEAK}$  working voltage.

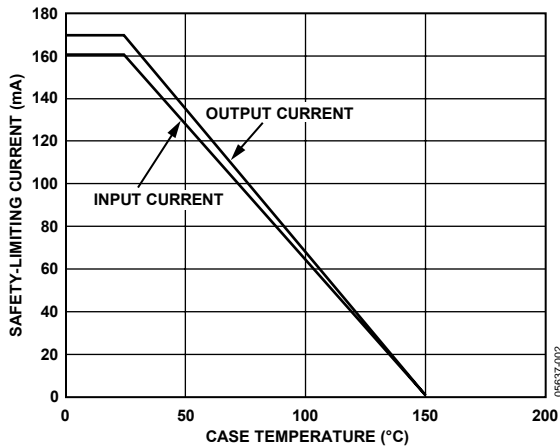


Figure 2. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per DIN EN 60747-5-2

## RECOMMENDED OPERATING CONDITIONS

Table 8.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	$T_A$	-40	+105	°C
Supply Voltages <sup>1</sup>	$V_{DD1}$ , $V_{DD2}$	3.0	5.5	V
Logic High Input Voltage, 5 V Operation (See Figure 10 and Figure 11)	$V_{IH}$	2.0	$V_{DD1}$	V
Logic Low Input Voltage, 5 V Operation <sup>1,2</sup> (See Figure 10 and Figure 11)	$V_{IL}$	0.0	0.8	V
Logic High Input Voltage, 3.3 V Operation <sup>1,2</sup> (See Figure 10 and Figure 11)	$V_{IH}$	1.5	$V_{DD1}$	V
Logic Low Input Voltage, 3.3 V Operation <sup>1,2</sup> (See Figure 10 and Figure 11)	$V_{IL}$	0.0	0.5	V
Input Signal Rise and Fall Times			1.0	ms

<sup>1</sup>All voltages are relative to their respective ground.

<sup>2</sup>Input switching thresholds have 300 mV of hysteresis. See the Method of Operation, DC Correctness, and Magnetic Field Immunity section, Figure 18, and Figure 19 for information on immunity to external magnetic fields.



## ABSOLUTE MAXIMUM RATINGS

Table 9.

Parameter	Min	Max	Unit
Storage Temperature, $T_{ST}$	-55	+150	°C
Ambient Operating Temperature, $T_A$	-40	+125	°C
Supply Voltages <sup>1</sup> , $V_{DD1}$ , $V_{DD2}$	-0.5	+6.5	V
Input Voltage <sup>1</sup> , $V_I$	-0.5	$V_{DD1} + 0.5$	V
Output Voltage <sup>1</sup> , $V_O$	-0.5	$V_{DD2} + 0.5$	V
Average Current, per Pin <sup>2</sup>			
Temperature $\leq 105^\circ\text{C}$	-25	+25	mA
Common-Mode Transients <sup>3</sup>	-100	+100	kV/ $\mu\text{s}$

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Ambient temperature = 25°C, unless otherwise noted.

<sup>1</sup> All voltages are relative to their respective ground.

<sup>2</sup> See Figure 2 for information on maximum allowable current for various temperatures.

<sup>3</sup> Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Rating can cause latch-up or permanent damage.

Table 10. Truth Table (Positive Logic)

$V_I$ Input	$V_{DD1}$ State	$V_{DD2}$ State	$V_O$ Output
H	Powered	Powered	H
L	Powered	Powered	L
X	Unpowered	Powered	H <sup>1</sup>
X	Powered	Unpowered	X <sup>1</sup>

<sup>1</sup>  $V_O$  returns to  $V_I$  state within 1  $\mu\text{s}$  of power restoration.

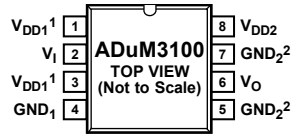
### ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



# ADuM3100

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



<sup>1</sup>PIN 1 AND PIN 3 ARE INTERNALLY CONNECTED. IT IS STRONGLY RECOMMENDED THAT BOTH BE CONNECTED TO  $V_{DD1}$ .  
<sup>2</sup>PIN 5 AND PIN 7 ARE INTERNALLY CONNECTED. IT IS STRONGLY RECOMMENDED THAT BOTH BE CONNECTED TO  $GND_2$ .

09637-003

Figure 3. Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$V_{DD1}$	Input Supply Voltage, 3.0 V to 5.5 V
2	$V_I$	Logic Input
3	$V_{DD1}$	Input Supply Voltage, 3.0 V to 5.5 V
4	$GND_1$	Input Ground
5	$GND_2$	Output Ground
6	$V_O$	Logic Output
7	$GND_2$	Output Ground
8	$V_{DD2}$	Output Supply Voltage, 3.0 V to 5.5 V

TYPICAL PERFORMANCE CHARACTERISTICS

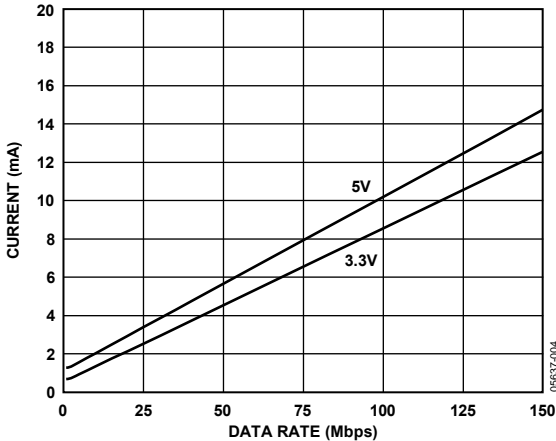


Figure 4. Typical Input Supply Current vs. Logic Signal Frequency for 5 V and 3.3 V Operation

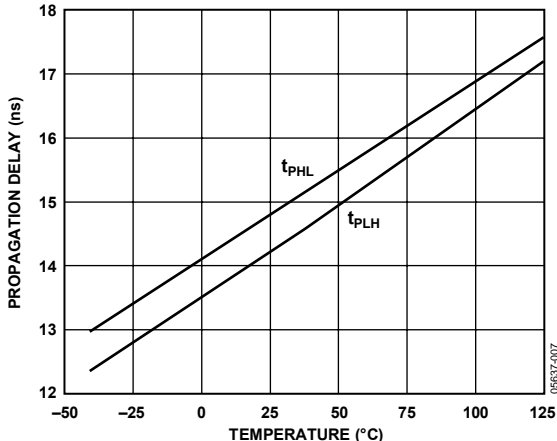


Figure 7. Typical Propagation Delays vs. Temperature, 3.3 V Operation

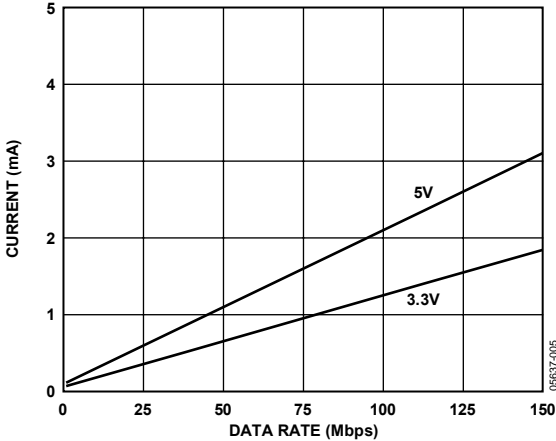


Figure 5. Typical Output Supply Current vs. Logic Signal Frequency for 5 V and 3.3 V Operation

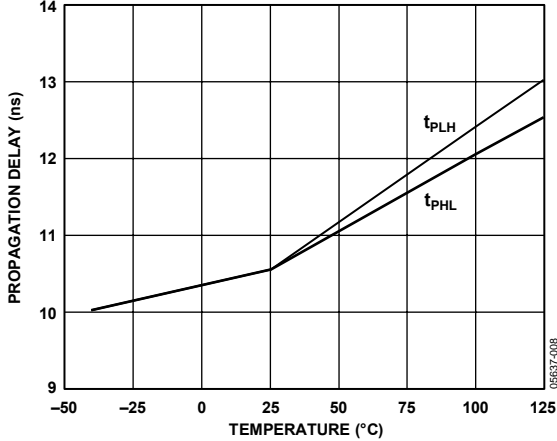


Figure 8. Typical Propagation Delays vs. Temperature, 5 V/3 V Operation

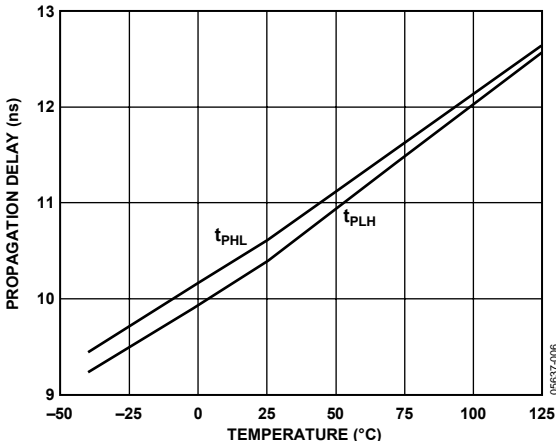


Figure 6. Typical Propagation Delays vs. Temperature, 5 V Operation

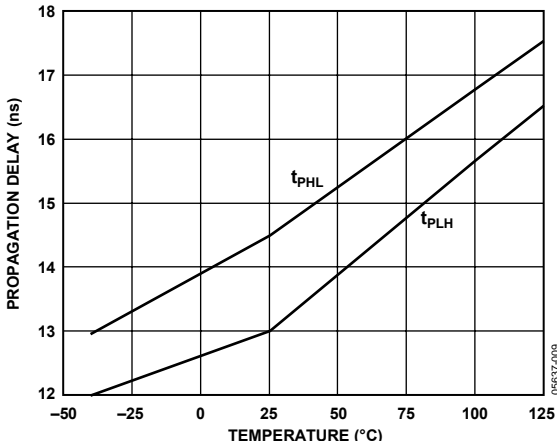


Figure 9. Typical Propagation Delays vs. Temperature, 3 V/5 V Operation

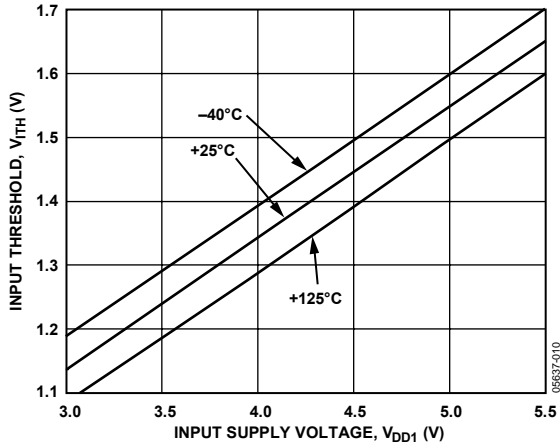


Figure 10. Typical Input Voltage Switching Threshold, Low-to-High Transition

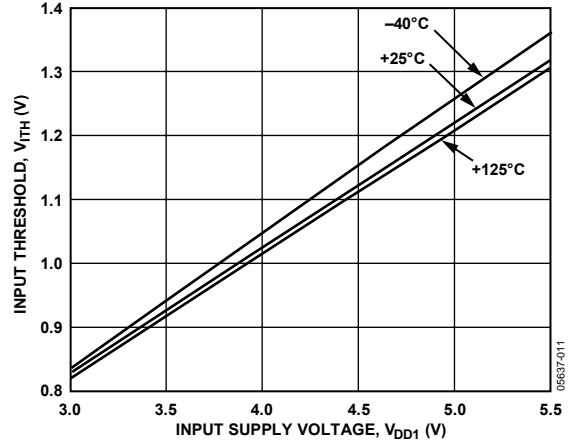


Figure 11. Typical Input Voltage Switching Threshold, High-to-Low Transition

## APPLICATIONS

### PC BOARD LAYOUT

The ADuM3100 digital isolator requires no external interface circuitry for the logic interfaces. A bypass capacitor is recommended at the input and output supply pins. The input bypass capacitor can conveniently connect between Pin 3 and Pin 4 (see Figure 12). Alternatively, the bypass capacitor can be located between Pin 1 and Pin 4. The output bypass capacitor can be connected between Pin 7 and Pin 8 or Pin 5 and Pin 8. The capacitor value should be between 0.01  $\mu\text{F}$  and 0.1  $\mu\text{F}$ . The total lead length between both ends of the capacitor and the power supply pins should not exceed 20 mm.

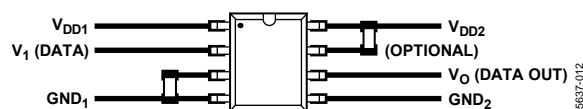


Figure 12. Recommended Printed Circuit Board Layout

### SYSTEM-LEVEL ESD CONSIDERATIONS AND ENHANCEMENTS

System-level ESD reliability (for example, per IEC 61000-4-x) is highly dependent on system design which varies widely by application. The ADuM3100 incorporates many enhancements to make ESD reliability less dependent on system design. The enhancements include:

- ESD protection cells added to all input/output interfaces.
- Key metal trace resistances reduced using wider geometry and paralleling of lines with vias.
- The SCR effect inherent in CMOS devices minimized by use of guarding and isolation technique between PMOS and NMOS devices.
- Areas of high electric field concentration eliminated using 45° corners on metal traces.
- Supply pin overvoltage prevented with larger ESD clamps between each supply pin and its respective ground.

While the ADuM3100 improves system-level ESD reliability, it is no substitute for a robust system-level design. See [Application Note AN-793, ESD/Latch-Up Considerations with iCoupler Isolation Products](#) for detailed recommendations on board layout and system-level design.

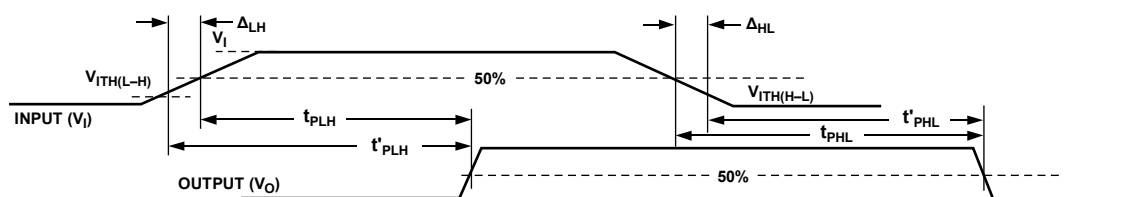


Figure 14. Impact of Input Rise/Fall Time on Propagation Delay

### PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay time describes the length of time it takes for a logic signal to propagate through a component. Propagation delay time to logic low output and propagation delay time to logic high output refer to the duration between an input signal transition and the respective output signal transition (see Figure 13).

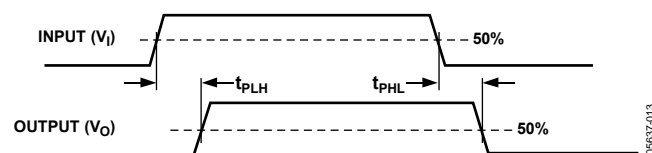


Figure 13. Propagation Delay Parameters

Pulse-width distortion is the maximum difference between  $t_{PLH}$  and  $t_{PHL}$  and provides an indication of how accurately the input signal timing is preserved in the component output signal. Propagation delay skew is the difference between the minimum and maximum propagation delay values among multiple ADuM3100 components operated at the same operating temperature and having the same output load.

Depending on the input signal rise/fall time, the measured propagation delay based on the input 50% level can vary from the true propagation delay of the component (as measured from its input switching threshold). This is due to the fact that the input threshold, as is the case with commonly used optocouplers, is at a different voltage level than the 50% point of typical input signals. This propagation delay difference is:

$$\Delta_{LH} = t'_{PLH} - t_{PLH} = (t_r/0.8 V_I)(0.5 V_I - V_{ITH(L-H)})$$

$$\Delta_{HL} = t'_{PHL} - t_{PHL} = (t_f/0.8 V_I)(0.5 V_I - V_{ITH(H-L)})$$

where:

$t_{PLH}$ ,  $t_{PHL}$  = propagation delays as measured from the input 50%.

$t'_{PLH}$ ,  $t'_{PHL}$  = propagation delays as measured from the input switching thresholds.

$t_r$ ,  $t_f$  = input 10% to 90% rise/fall time.

$V_I$  = amplitude of input signal (0 to  $V_I$  levels assumed).

$V_{ITH(L-H)}$ ,  $V_{ITH(H-L)}$  = input switching thresholds.

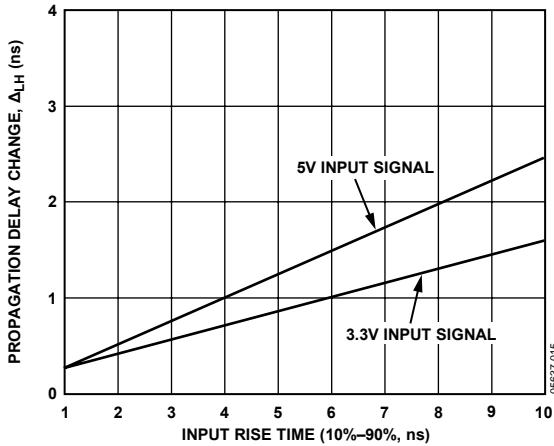


Figure 15. Typical Propagation Delay Change due to Input Rise Time Variation (for  $V_{DD1} = 3.3\text{ V}$  and  $5\text{ V}$ )

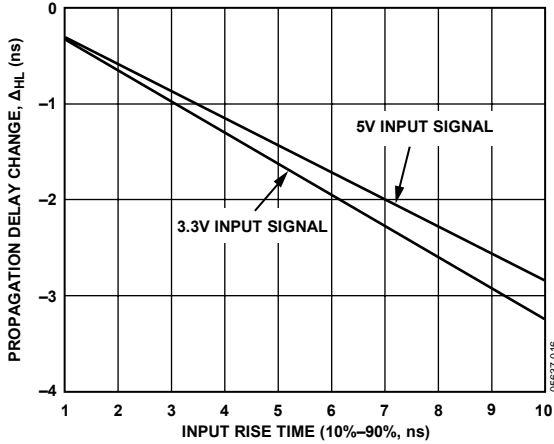


Figure 16. Typical Propagation Delay Change due to Input Fall Time Variation (for  $V_{DD1} = 3.3\text{ V}$  and  $5\text{ V}$ )

The impact of the slower input edge rates can also affect the measured pulse-width distortion as based on the input 50% level. This impact can either increase or decrease the apparent pulse-width distortion depending on the relative magnitudes of  $t_{PHL}$ ,  $t_{PLH}$ , and PWD. The case of interest here is the condition that leads to the largest increase in pulse-width distortion. The change in this case is given by

$$\Delta_{PWD} = PWD' - PWD = \Delta_{LH} - \Delta_{HL} = (t/0.8 V_i)(V - V_{ITH(L-H)} - V_{ITH(H-L)}), (\text{for } t = t_r = t_f)$$

where:

$$PWD = |t_{PLH} - t_{PHL}|$$

$$PWD' = |t'_{PLH} - t'_{PHL}|$$

This adjustment in pulse-width distortion is plotted as a function of input rise/fall time in Figure 17.

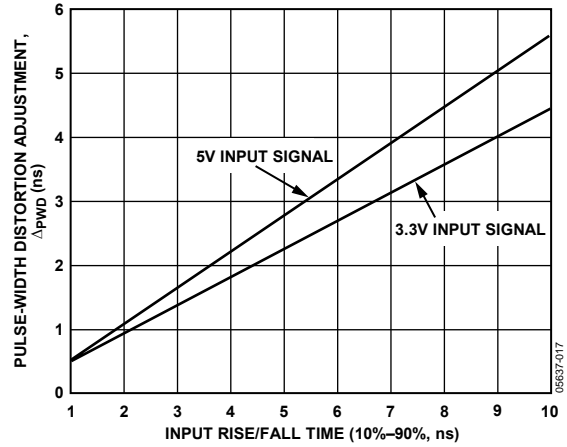


Figure 17. Typical Pulse-Width Distortion Adjustment due to Input Rise/Fall Time Variation (at  $V_{DD1} = 3.3\text{ V}$  and  $5\text{ V}$ )

## METHOD OF OPERATION, DC CORRECTNESS, AND MAGNETIC FIELD IMMUNITY

Referring to Figure 1, the two coils act as a pulse transformer. Positive and negative logic transitions at the isolator input cause narrow (2 ns) pulses to be sent via the transformer to the decoder. The decoder is bistable and therefore either set or reset by the pulses indicating input logic transitions. In the absence of logic transitions at the input for more than 2  $\mu\text{s}$ , a periodic update pulse of the appropriate polarity is sent to ensure dc correctness at the output. If the decoder does not receive any of these update pulses for more than approximately 5  $\mu\text{s}$ , the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a logic high state by the watchdog timer circuit.

The limitation on the ADuM3100 magnetic field immunity is set by the condition in which induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The analysis that follows defines the conditions under which this can occur. The ADuM3100 3.3 V operating condition is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output are greater than 1.0 V in amplitude. The decoder has sensing thresholds at about 0.5 V, therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \sum \pi r_n^2, n = 1, 2, \dots, N$$

where:

$\beta$  = magnetic flux density (gauss).

$N$  = number of turns in receiving coil.

$r_n$  = radius of  $n$ th turn in receiving coil (cm).

Given the geometry of the receiving coil in the ADuM3100 and an imposed requirement that the induced voltage be at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 18.

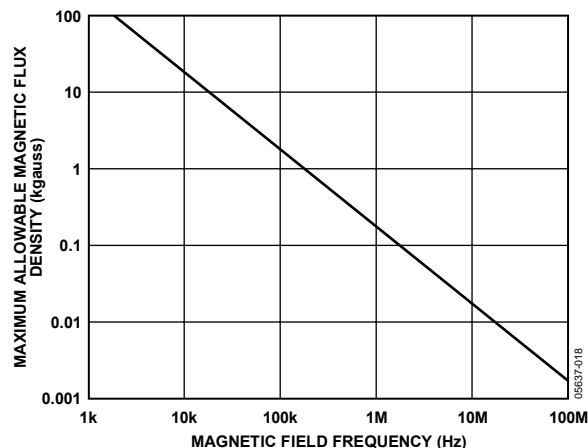


Figure 18. Maximum Allowable External Magnetic Field

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event were to occur during a transmitted pulse (and was of the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM3100 transformers. Figure 19 shows the allowable current magnitudes as a function of frequency for selected distances. As can be seen, the ADuM3100 is extremely immune and can be affected only by extremely large currents operated at high frequency and very close to the component. For the 1 MHz example noted, one would have to place a current of 0.5 kA 5 mm away from the ADuM3100 to affect the component's operation.

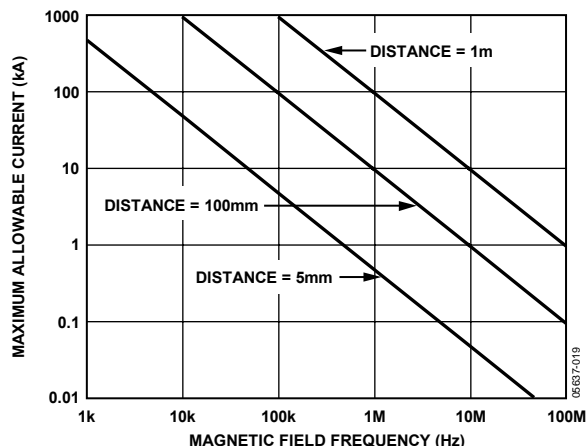


Figure 19. Maximum Allowable Current for Current-to-ADuM3100 Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

## POWER CONSUMPTION

The supply current of the ADuM3100 isolator is a function of the supply voltage, the input data rate, and the output load.

The input supply current is given by

$$I_{DDI} = I_{DDI(Q)} \quad f \leq 0.5f_r$$

$$I_{DDI} = I_{DDI(D)} \times (2f - f_r) + I_{DDI(Q)} \quad f > 0.5f_r$$

The output supply current is given by

$$I_{DDO} = I_{DDO(Q)} \quad f \leq 0.5f_r$$

$$I_{DDO} = (I_{DDO(D)} + (0.5 \times 10^{-3}) \times C_L V_{DDO}) \times (2f - f_r) + I_{DDO(Q)} \quad f > 0.5f_r$$

where:

$I_{DDI(D)}$ ,  $I_{DDO(D)}$  are the input and output dynamic supply currents per channel (mA/Mbps).

$C_L$  is output load capacitance (pF).

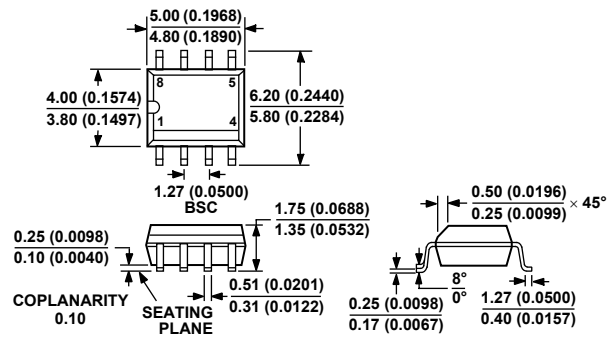
$V_{DDO}$  is the output supply voltage (V).

$f$  is the input logic signal frequency (MHz, half of the input data rate, NRZ signaling).

$f_r$  is the input stage refresh rate (Mbps).

$I_{DDI(Q)}$ ,  $I_{DDO(Q)}$  are the specified input and output quiescent supply currents (mA).

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 20. 8-Lead Standard Small Outline Package [SOIC\_N]  
 Narrow Body (R-8)

Dimensions shown in millimeters and (inches)

## ORDERING GUIDE

Model	Temperature Range	Max Data Rate (Mbps)	Minimum Pulse Width (ns)	Package Description	Package Option
ADuM3100ARZ <sup>1</sup>	-40°C to +105°C	25	40	8-Lead SOIC_N	R-8
ADuM3100ARZ-RL7 <sup>1</sup>	-40°C to +105°C	25	40	8-Lead SOIC_N, 1,000 Piece Reel	R-8
ADuM3100BRZ <sup>1</sup>	-40°C to +105°C	100	10	8-Lead SOIC_N	R-8
ADuM3100BRZ-RL7 <sup>1</sup>	-40°C to +105°C	100	10	8-Lead SOIC_N, 1,000 Piece Reel	R-8

<sup>1</sup> Z = Pb-free part.