

ACT3492 Series

MIL-STD-1553B Remote Terminal, BUS Controller, or Passive Monitor Hybrid with Status Word Control Dual Low Power Monolithic BUS Tranceivers

Features

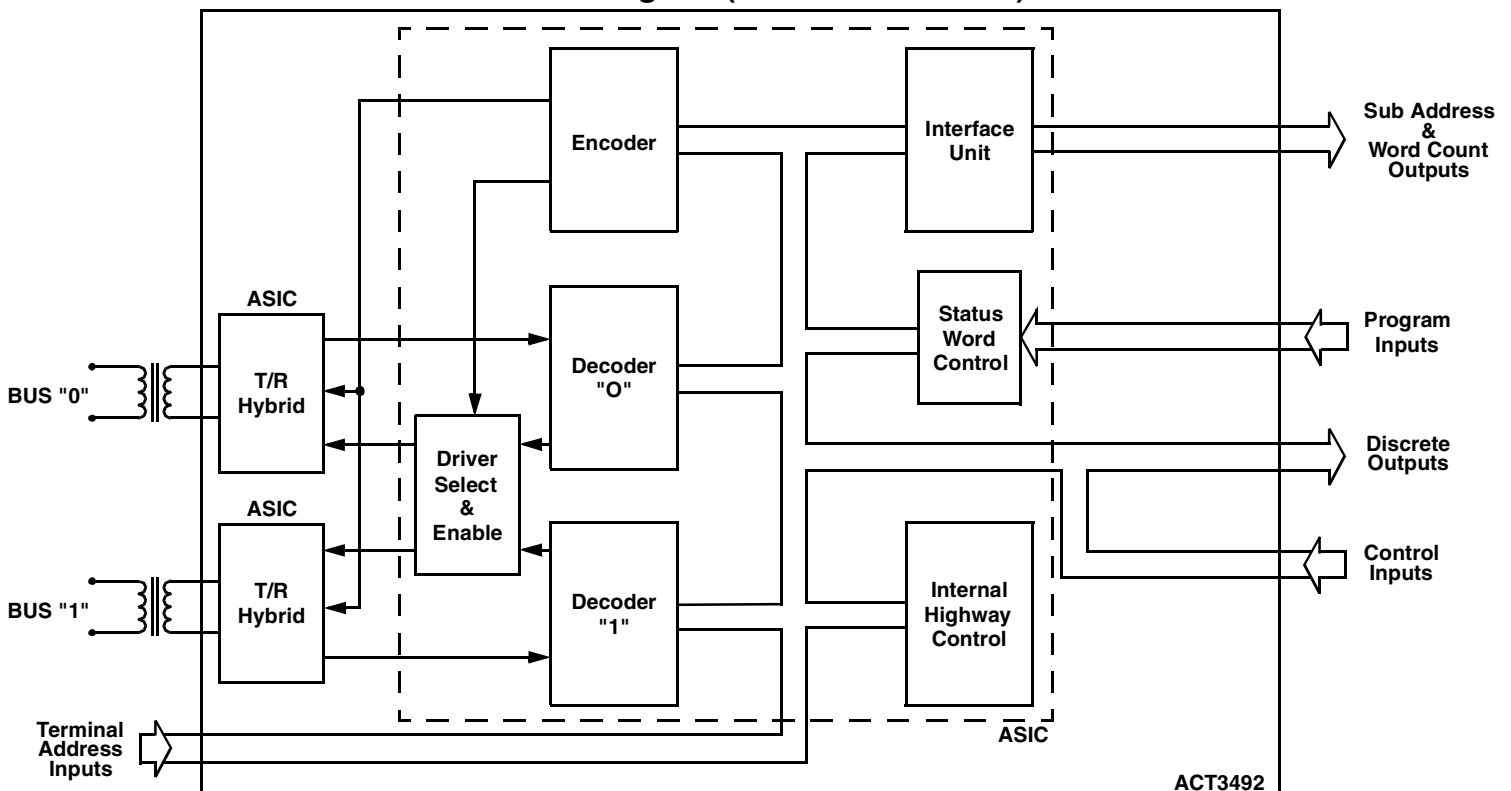
- Dual Low Power Monolithic Bus Tranceivers
- Performs the Complete Dual-Redundant Remote Terminal, Bus Controller Protocol and Passive Monitor Functions of MIL-STD-1553B
- Automated Self-Test Functions
- Allows Setting of the Message Error Bit on Illegal Commands
- Provides programmable control over Terminal Flag and Subsystem Flag Status Bits
- MIL-PRF-38534 Compliant Circuits Available
- 250 mw Typical Power Consumption
- Small Size
- Available in Ceramic Plug-in Package Configuration
- 5V DC Operation
- Full Military (-55°C to +125°C) Temperature Range
- DESC SMD# Pending



General Description

The ACT3492 Series is a monolithic implementation of the MIL-STD-1553B Bus Controller, Remote Terminal and Passive Monitor functions including dual low power Bus tranceivers. All protocol functions of MIL-STD-1553B are incorporated and a number of options are included to improve flexibility. These features include programming of the status word, illegalizing specific commands and an independent loop back self-test which is initiated by the subsystem. This unit is directly compatible with all microprocessor interfaces such as the CT1611 and CT1800 produced by Aeroflex Incorporated.

Block Diagram (With Transformers)



Electrical Performance Characteristics

Absolute Maximum Ratings

Parameter	Min	Max	Units
V _{CC}	-0.3	7.0	V
Input or Output Voltage at any Pin	-0.3	V _{CC} + 0.3V	V
Storage Case Temperature	-65	+150	°C
Load Temperature (Soldering 10 Sec)		+300	°C

Digital Protocol Logic Characteristics (Over Full Temperature Range)

Parameter	Test Conditions	Min	Typ	Max	Unit	Notes
V _{CC} (Logic)		4.5	5.0	5.5	V	
V _{IH}	V _{CC} = 5.0V	2.2			V	
V _{IL}	V _{CC} = 5.0V			0.7	V	
V _{OH} High Level Output Voltage	V _{CC} = 4.5V	2.4			V	1A
V _{OL} Low Level Output Voltage	V _{CC} = 4.5V			0.4	V	1A
I _{IH} High Level Input Current	V _{CC} = 5.5V, V _{IN} = 2.7V	-200 -25		-700 -400	μA μA	2A 3A
I _L Low Level Input Current	V _{CC} = 5.5V, V _{IN} = 0.4V	-400 -25		-900 -400	μA μA	2A 3A
I _{CC} (Logic)	V _{CC} = 5.5V			20	mA	4A

Notes:

1A/ I_{OL} = 3mA maximum, I_{OH} = -2 mA maximum for all outputs and bidirectionals.

2A/ RTAD 0, 1, 2, 3, 4 and RTADPAR only.

3A/ All inputs and bidirectionals other than those in note 2.

4A/ Input clock (running) = 6Mhz, All remaining Inputs are Open and All Outputs and Bidirectionals have no load.

Absolute Maximum Ratings (Analog Transceiver)

Parameter	Min	Max	Units
V _{CC}	-0.3	7.0	V
Receiver Differential Voltage		10 V _{p-p}	V
Receiver Common-Mode Voltage	-5.0	+5.0	V _{dc}
Driver Peak Output Current		800	mA

Analog Transceiver Recommended Operating Conditions

Parameter	Min	Max	Unit	Notes
V _{CC} (Logic)	4.75	5.5	V	
Receiver Differential Voltage (See Point A Figure 4)		4.0	V _{p-p}	
Receiver Common-Mode Voltage (See Figure 4)	-1.75	+5	V _{dc}	
Driver Peak Output Current		700	mA	
Serial Data Rate		1.0	MHz	
Case operating temperature	-55	+125	°C	

Analog Transceiver Characteristics (Over Full Temperature Range)

Parameter	Min	Max	Unit	Notes
Differential Input Level	-8	+8	V _{p-p}	1,3
Input Common-Mode Voltage	-1.75	+5	V	1,3
Threshold Voltage	0.6	1.1	V	4

Analog Transceiver Characteristics (Over Full Temperature Range)

Parameter	Symbol	Test Conditions	Min	Max	Unit	Notes
Differential Output Voltage	V _O	35 ohm load, Point A 70 ohm load, Point C Figure 4	6.0 18	9.0 26	V _{p-p} V _{p-p}	1
Differential Output Noise	V _{ON}	Inhibited Figure 4, Point A		10	mV _{p-p}	3
Terminal Input Impedance	Z _{IN}	Transmitter off 1 Mhz sine wave As measured from the 1553 bus (direct coupled). Figure 4 Point A	2.0		KΩ	1
Differential Offset Voltage	V _{OS}	35 ohm load, Point A 70 ohm load, Point C Figure 4		±90 ±250	mV mV	1, 3, 5 1,5
Rise Time	t _R	35 or 70 ohm load Figure 4, Points A,C	100	300	nSec	1
Fall Time	t _F	35 or 70 ohm load Figure 4, Points A,C	100	300	nSec	1

Analog Transceiver Power Supply Characteristics (Each Channel)

Parameter	Symbol	Test Conditions	Min	Max	Unit	Notes
Supply Current	I _{CC1}	Standby		25	mA	1,2
	I _{CC2}	25% duty cycle		160	mA	1,2
	I _{CC3}	50% duty cycle		290	mA	1,2
	I _{CC4}	100% duty cycle		550	mA	1,2,3

Notes:

- 1/ VCC = 5.0 Volts dc +/-0.1 Volts dc unless otherwise specified.
- 2/ All specifications and limits are for a single channel with no connections made to the other channel.
- 3/ Parameters shall be tested as part of device initial characterization and after design and process changes. Parameter shall be guaranteed to limits specified in above tables for all lots not specifically tested.
- 4/ Threshold determined by first no response to a receive 32 word command.
- 5/ Measured 2.5μSec after the mid-bit zero crossing of the last parity bit of a 660μSec transmission.

REMOTE TERMINAL OPERATION

Receive Data Operation

All valid data words associated with a valid receive data command word for the RT are passed to the subsystem. The RT examines all command words from the bus and will respond to valid (i.e. correct Manchester, parity coding etc.) commands which have the correct RT address (or broadcast address if the RT broadcast option is enabled). When the data words are received, they are decoded and checked by the RT and, if valid, passed to the subsystem on a word by word basis at 20 μ s intervals. This applies to receive data words in both Bus Controller to RT and RT to RT messages. When the RT detects that the message has finished, it checks that the correct number of words have been received and if the message is fully valid, then a Good Block Received signal is sent to the subsystem, which must be used by the subsystem as permission to use the data just received.

The subsystem must therefore have a temporary buffer store up to 32 words long into which these data words can be placed. The Good Block Received signal will allow use of the buffer store data once the message has been validated.

If a block of data is not validated, then Good Block Received will not be generated. This may be caused by any sort of message error or by a new valid command for the RT being received on another bus to which the RT must switch.

Transmit Data Operation

If the RT receives a valid transmit data command addressed to the RT, then the RT will request the data words from the subsystem for transmission on a word by word basis. To allow maximum time for the subsystem to collect each data word, the next word is requested by the RT as soon as the transmission of the current word has commenced.

It is essential that the subsystem should provide all the data words requested by the RT once a transmit sequence has been accepted. Failure to do so will be classed by the RT as a subsystem failure and reported as such to the Bus Controller.

Control of Data Transfers

This section describes the detailed operation of the data transfer mechanism between the RT and subsystems. It covers the operations of the signals \overline{DTRQ} , \overline{DTAK} , IUSTB, H/L, \overline{GBR} , \overline{NBGT} , TX/RX during receive data and transmit data transfers. Figures 29 and 30 show typical interfacing logic.

Figures 5 and 15 shows the operation of the data handshaking signals during a receive command with one data word. When the RT has fully checked the command word, \overline{NBGT} is pulsed low, which can be used by the subsystem as an initialization signal. TX/RX will be set low indicating a receive command. When the first data word has been fully validated, \overline{DTRQ} is set low. The subsystem must then reply within approximately 1.5 μ s by setting \overline{DTAK} low. This indicates to the RT that the subsystem is ready to accept data. The data word is then passed to the subsystem on the internal highway IH08-IH715 in two bytes using IUSTB as a strobe signal and H/L as the byte indicator (high byte first followed by low byte). Data is valid about both edges of IUSTB. Signal timing for this handshaking is shown in Figure 15. Also see Figures 19 and 20.

If the subsystem does not declare itself busy, then it must respond to \overline{DTRQ} going low by setting \overline{DTAK} low within approximately 1.5 μ s. Failure to do so will be classed by the RT as a subsystem failure and reported as such to the Bus Controller.

It should be noted that IUSTB is also used for internal working in the RT. \overline{DTRQ} being low should be used as an enable for clocking data to the subsystem with IUSTB.

Once the receive data block has finished and been checked by the RT, \overline{GBR} is pulsed low if the block is entirely correct and valid. This is used by the subsystem as permission to make use of the data block. If no \overline{GBR} signal is generated, then an error has been detected by the RT and the entire data block is invalid and no data words in it may be used.

If the RT is receiving data in an RT to RT transfer, the data handshaking signals will operate in an identical

fashion but there will be a delay of approx 70 μ s between $\overline{\text{NBGT}}$ going low and $\overline{\text{DTRQ}}$ first going low. Figures 6 and 15 show the operation of the data handshaking signals during transmit command with one data word. As with the receive command discussed previously, $\overline{\text{NBGT}}$ is pulsed low if the command is valid and for the RT. $\text{TX}/\overline{\text{RX}}$ will be set high indicating a transmit data command. While the RT is transmitting its status word, it requests the first data word from the subsystem by setting $\overline{\text{DTRQ}}$ low. The subsystem must then reply within approximately 13.5 μ s by setting $\overline{\text{DTAK}}$ low. By setting $\overline{\text{DTAK}}$ low, the subsystem is indicating that it has the data word ready to pass to the RT. Once $\overline{\text{DTAK}}$ is set low by the subsystem, $\overline{\text{DTRQ}}$ should be used together with $\text{H}/\overline{\text{L}}$ and $\text{TX}/\overline{\text{RX}}$ to enable first the high byte and then the low byte of the data word onto the internal highway IH08-IH715. The RT will latch the data bytes during IUSTB, and will then return $\overline{\text{DTRQ}}$ high. Data for each byte must remain stable until IUSTB has returned low. Signal timing for this handshaking is shown in Figure 15.

Additional Data Information Signals

At the same time as data transfers take place, a number of information signals are made available to the subsystem. These are $\overline{\text{INCMD}}$, the subaddress lines SA0-SA4, the word count lines WC0-WC4 and current word count lines CWC0-CWC4. Use of these signals is optional.

$\overline{\text{INCMD}}$ will go active low while the RT is servicing a valid command for the RT. The subaddress, transmit/receive bit, and word count from the command word are all made available to the subsystem as SA0-SA4, $\text{TX}/\overline{\text{RX}}$ and WC0-WC4 respectively. They may be sampled when $\overline{\text{INCMD}}$ goes low and will remain valid while $\overline{\text{INCMD}}$ is low. See Figure 11.

The subaddress is intended to be used by the subsystem as an address pointer for the data block. Subaddress 0 and 31 are mode commands, and there can be no receive or transmit data blocks associated with these. (Any data word associated with a mode command uses different handshaking operations. If the subsystem does not use all the subaddresses available, then some of the subaddress lines may be ignored.

The $\text{TX}/\overline{\text{RX}}$ signal indicates the direction of data transfer across the RT - subsystem interface. Its use is described in the previous section.

The word count tells the subsystem the number of words to expect to receive or transmit in a message, up to 32 words. A word count of all 0s indicates a count of 32 words.

The current word count is set to 0 at the beginning of a new message and is incremented following each data word transfer across the RT - subsystem interface. (It is clocked on the falling edge of the second IUSTB pulse in each word transfer). It should be noted that there is no need for the subsystem to compare the word count and current word count to validate the number of words in a message. This is done by the RT.

Subsystem Use of Status Bits and Mode Commands

General Description

Use of the status bits and the mode commands is one of the most confusing aspects of MIL-STD-1553B. This is because much of their use is optional, and also because some involve only the RT while others involve both the RT and the subsystem.

The ACT3492 allows full use to be made of all the Status Bits, and also implements all the Mode Commands. External programming of the Terminal Flag and Subsystem Flag Bits plus setting of the Message Error Bit on reception of an illegal command when externally decoded is available. The subsystem is given the opportunity to make use of Status Bits, and is only involved in Mode Commands which have a direct impact on the subsystem.

The mode commands in which the subsystem may be involved are Synchronize, Synchronize with data word, Transmit Vector Word, Reset and Dynamic Bus Control Acceptance. The Status Bits to which the subsystem has access, or control are Service Request, Busy, Dynamic Bus Control Acceptance, Terminal Flag, Subsystem Flag, and Message Error Bit. Operation of each of these Mode Commands and of the Status Bits is described in the following sections.

All other Mode Commands are serviced internally by the RT. The Terminal Flag and Message Error Status Bits and BIT Word contents are controlled by the RT; however the subsystem has the option to set the Message Error Bit and to control the reset conditions for the Terminal Flag and Subsystem Flag Bits in the Status Word, and the Transmitter Timeout, Subsystem Handshake, and Loop Test Fail Bits in the BIT Word.

Synchronize Mode Commands

Once the RT has validated the command word and checked for the correct address, the SYNC line is set low. The signal WC4 will be set low for a Synchronize mode command, and high for a Synchronize with data word mode command (See Figure 9). In a Synchronize with data word mode command, SYNC remains low during the time that the data word is received. Once the data word has been validated, it is passed to the subsystem on the internal highway IH08-IH715 in two bytes using IUSTB as a strobe signal and H/L as the byte indicator (high byte first followed by low byte). SYNC being low should be used on the enable to allow IUSTB to clock synchronize mode data to the subsystem.

If the subsystem does not need to implement either of these mode commands, the SYNC signal can be ignored, since the RT requires no response from the subsystem.

Transmit Vector Word Mode Command

Figures 8 and 17 illustrates the relevant signal timings for an RT receiving a valid Transmit Vector Word mode command. The RT requests data by setting $\overline{\text{VECTEN}}$ low. The subsystem should use H/L to enable first the high byte and then the low byte of the Vector word onto the internal highway IH08-IH715.

It should be noted that the RT expects the Vector word contents to be already prepared in a latch ready for enabling onto the internal highway when $\overline{\text{VECTEN}}$ goes low. If the subsystem has not been designed to handle the Vector word mode command, it will be the fault of the Bus Controller if the RT receives such a command. Since the subsystem is not required to acknowledge the mode command, the RT will not be affected in any way by Vector word circuitry not being implemented in the subsystem. It will however transmit a data word as the Vector word, but this word will have no meaning.

Reset Mode Command

Figure 7 shows the relevant signal timings for an RT receiving a valid reset mode command. Once the command word has been fully validated and serviced, the RESET signal is pulsed low. This signal may be used as a reset function for subsystem interface circuitry.

Dynamic Bus Allocation

This mode command is intended for use with a terminal which has the capability of configuring itself into a bus controller on command from the bus. The line $\overline{\text{DBCREQ}}$ (See Figure 7) cannot go true unless the $\overline{\text{DBCACC}}$ line was true at the time of the valid command, i.e. tied low. For terminals acting only as RTs, the signal $\overline{\text{DBCACC}}$ should be tied high (inactive), and the signal $\overline{\text{DBCREQ}}$ should be ignored and left unconnected.

Use of the Busy Status Bit

The Busy Bit is used by the subsystem to indicate that it is not ready to handle data transfers either to or from the RT.

The RT sets the bit to logic one if the $\overline{\text{BUSY}}$ line from the subsystem is active low at the time of the second falling edge of INCLK after $\overline{\text{INCMD}}$ goes low. This is shown in Figures 14 and 20. Once the Busy bit is set, the RT will stop all receive and transmit data word transfers to and from the subsystem. The data transfers in the Synchronize with data word and Transmit Vector word mode commands are not affected by the Busy bit and will take place even if it has been set.

It should be noted that a minimum of 0.5 μs subaddress decoding time is given to the subsystem before setting of status bits. This allows the subsystem to selectively set the Busy bit if for instance one

subaddress is busy but others are ready. This option will prove useful when an RT is interfacing with multiple subsystems.

Use of the Service Request Status Bit

The Service Request bit is used by the subsystem to indicate to the Bus Controller that an asynchronous service is requested.

The timing of the setting of this bit is the same as the Busy bit and is shown in Figures 14 and 20. Use of $\overline{\text{SERVREQ}}$ has no effect on the RT apart from setting the Service Request bit.

It should be noted that certain mode commands require that the last status word be transmitted by the RT instead of the current one, and therefore a currently set status bit will not be seen by the Bus Controller. Therefore the user is advised to hold $\overline{\text{SERVREQ}}$ low until the requested service takes place.

Use of the Subsystem Status Bit

This status bit is used by the RT to indicate a subsystem fault condition. If the subsystem sets $\overline{\text{SSERR}}$ low at any time, the subsystem fault condition in the RT will be set, and the Subsystem Flag status bit will subsequently be set. The fault condition will also be set if a handshaking failure takes place during a data transfer to or from the subsystem. The fault condition is cleared on power-up or by a Reset mode command.

Dynamic Bus Control Acceptance Status Bit

$\overline{\text{DBCACC}}$, when set true, enables an RT to configure itself into a Bus Controller, if the subsystem has the capability, by allowing $\overline{\text{DBCREQ}}$ to pulse true and BIT TIME 18 to be set in the status response. If Dynamic Bus Control is not required then $\overline{\text{DBCACC}}$ must be tied high. $\overline{\text{DBCACC}}$ tied high inhibits $\overline{\text{DBCREQ}}$ and clears BIT TIME 18 in the status response.

OPTIONAL STATUS WORD CONTROL

Message Error Bit

The ACT3492 monitors all receptions for errors and sets the Message Error Bit as prescribed in MIL-STD-1553B. The subsystem designer may, however, exercise the option of monitoring for illegal commands and forcing the Message Error Bit to be set.

The word count and subaddress lines for the current command are valid when $\overline{\text{INCMD}}$ goes low. The subsystem must then determine whether or not the word count or subaddress is to be considered illegal by the RT. If either of them is considered illegal, the subsystem must produce a positive-going pulse called MEREQ. The positive-going edge of MEREQ must occur within 500 nSec of the falling edge of $\overline{\text{INCMD}}$.

Subsystem Flag and Terminal Flag Bits

The conditions that cause the Subsystem Flag and Terminal Flag Bits in the Status Word to be reset may be controlled by the subsystem using the $\overline{\text{ENABLE}}$, $\overline{\text{BIT DECODE}}$, $\overline{\text{NEXT STATUS}}$, and $\overline{\text{STATUS UPDATE}}$ inputs. If $\overline{\text{ENABLE}}$ is inactive (high), then the Terminal Flag and Subsystem Flag behavior is the same as described below: (i.e. the other three option lines are disabled).

Subsystem Flag Bit

This bit is reset to logic zero by a power up initialization or the servicing of a legal mode command to reset the remote terminal (code 01000).

This bit shall be set in the current status register if the subsystem error line, $\overline{\text{SSERR}}$, from the subsystem ever goes active low. This bit shall also be set if an RT/subsystem handshaking failure occurs. This bit, once set, shall be repeatedly set until the detected error condition is known to be no longer present.

Terminal Flag Bit

This bit is reset to logic zero by a power up initialization or the servicing of a legal mode command to reset the remote terminal (code 01000). This bit can be set to logic one in the current status register in four possible ways:

- a) If the RX detects any message encoding or content error in the terminal's transmission. A loop test failure, LTFAIL, will be signalled which shall cause the Terminal Flag to be set and the transmission aborted.
- b) If a transmitter timeout occurs while the terminal is transmitting.
- c) If a remote terminal self test fails.
- d) If there is a parity error in the hard wired address to the RX chip.

This bit, once set, shall be repeatedly set until the detected error condition is known to be no longer present. The transmission of this bit as a logic one can be inhibited by a legal mode command to inhibit terminal flag bit (code 00110). Similarly, this inhibit can be removed by a mode command to override inhibit terminal flag bit (code 00111), a power up initialization or a legal mode command to reset remote terminal (code 01000).

If $\overline{\text{ENABLE}}$ is held low, then the three options described below are available and are essentially independent. Any, all, or none may be selected. Also, reporting of faults by the subsystem requires that SSERR be latched (not pulsed) low until the fault is cleared.

Resetting SSF and TF on Receipt of Valid Commands

If $\overline{\text{ENABLE}}$ is selected and the other three option lines are held high, then the Status Word Register will be reset on receipt of any valid command with the exception of Transmit Status and Transmit Last Command. Note that in this mode, the TF will never be seen in the Status Word, and the SSF will only be seen if $\overline{\text{SSERR}}$ is latched low. Also note that the SSF will not be seen in response to Transmit Status or Transmit Last Command if the preceding Status Word was clear, regardless of actions taken on the $\overline{\text{SSERR}}$ line after the clear status transmission.

Status Register Update at Fault Occurrence

If $\overline{\text{STATUS UPDATE}}$ is selected (held low), then the TF or SSF will appear in response to a Transmit Status or Transmit Last Command issued as the first command after the fault occurs. Any other command (except as noted in the Preserving the BIT Word section) will reset the TF and SSF. Repeated Transmit Status or Transmit Last Command immediately following the fault will continue to show the TF and/or SSF in the Status Word. Note that this behavior may not meet the "letter-of-the-spec" as described in MIL-STD-1553B, but is considered the "preferred" behavior by some users.

TF and SSF Reporting in the Next Status Word After the Fault

If $\overline{\text{NEXT STATUS}}$ is selected (held low), then the TF or SSF will appear in response to the very next valid command after the fault except for Transmit Status or Transmit Last Command. The flag(s) will be reset on receipt of any valid command following the status transmission with the flag(s) set except for Transmit Status, Transmit Last Command, or as noted in the following section on Preserving the BIT Word.

Preserving the BIT Word

In order to preserve the Transmitter Timeout Flag, Subsystem Handshake Failure, and Loop Test Failure Bits in the BIT Word, it is necessary to select $\overline{\text{BIT DECODE}}$ (hold it low). This will prevent resetting those bits if the Transmit Bit Word Mode Command immediately follows the fault or follows a Transmit Last Command or Transmit Status immediately following the fault. It will also prevent resetting the TF and SSF Bits in the Status Word. Any other valid commands will cause those BIT Word Bits and the Status Word Bits to be reset.

BUS CONTROL OPERATION

To enable its use in a bus controller the ASIC has additional logic within it. This logic can be enabled by pulling the pin labelled RT/ \overline{BC} low. Once the ASIC is in bus control mode, all data transfers must be initiated by the bus control processor correctly commanding the ASIC via the subsystem interface. In bus control mode six inputs are activated which in RT mode are inoperative and four signals with dual functions exercise the second function (the first being for the RT operation).

To use the ACT3492 as a 1553B bus control interface, the bus control processor must be able to carry out four basic bus-related functions. Two inputs, BCOPA and BCOPB allow these four options to be selected. The option is then initiated by sending a negative-going strobe on the $\overline{BCOPSTB}$ input. $\overline{BCOPSTB}$ must only be strobed low when \overline{NDRQ} is high. This is particularly important when two options are required during a single transfer. See Figure 28 and Table 1.

With these options all message types and lengths can be handled. Normal BC/RT exchanges are carried out in option zero. This is selected by setting BCOPA and BCOPB to a zero and strobing $\overline{BCOPSTB}$. On receipt of the strobe, the ACT3492 loads the command word from an external latch using \overline{CWEN} and H/L. The command word is transmitted down the bus. The TX/RX bit is, however, considered as being its inverse and so if a transmit command is sent to a RT (Figure 21), the ACT3492 in BC mode believes it has been given a receive command. As the RT returns the requested number of data words plus its status, the BC carries out a full validation check and passes the data into the subsystem using \overline{DTRQ} , \overline{DTAK} , H/L, IUSTB and CWC as in RT operation. It also supplies \overline{GBR} at the end of a valid transmission. Conversely, a receive command sent down the bus is interpreted by the BC as a transmit command, and so the requisite data words are added to the command word. See Figure 22.

For mode commands, where a single command word is required, option one is selected by strobing $\overline{BCOPSTB}$ when BCOPA is high and BCOPB is low. On receiving the strobe, the command word is loaded from the external latch using \overline{CWEN} and H/L, the correct sync and parity bits are added and the word transmitted (See Figure 23). Mode commands followed by a data word requires option two, selected by strobing $\overline{BCOPSTB}$ while BCOPA is low and BCOPB is high, loads a data word via \overline{DWEN} and H/L, adds sync and parity and transmits them to the bus (See Figure 25). If the mode code transmitted required the RT to return a data word, then selecting option three by strobing $\overline{BCOPSTB}$ when BCOPA and BCOPB are both high will identify that data word and if validated, output it to the subsystem interface using RMDSTB and H/L. This allows data words resulting from mode codes to be identified differently from ordinary data words and routed accordingly (See Figure 24). All received status words are output to the subsystem interface using STATSTB and H/L.

In BC option three, if the signal \overline{PASMON} is active, then all data appearing on the selected bus is output to the subsystem using STATSTB for command and status words or RMDSTB for data words. See Passive Monitor.

RT to RT transfers require the transmission of two command words. A receive command to one RT is contiguously followed by a transmit command to the other RT. This can be achieved by selecting option one followed by option zero for the second command. The strobe ($\overline{BCOPSTB}$) for option zero must be delayed until \overline{NDRQ} has gone low and returned high following the strobe for option one. The RT transmissions are checked and transferred in the subsystem interface to the bus control processor (See Figure 26).

BC must wait for \overline{RTO} to pulse before issuing subsequent messages.

PASSIVE MONITOR

The Monitor Mode may be utilized to analyze or collect all activities which occur on a selected bus. This is initiated by selecting a bus, placing the unit in BC option three and setting \overline{PASMON} low. All data appearing on the selected bus is output to the subsystem using STATSTB for Command and Status Words or RMDSTB for Data Words. See Figure 27.

AUTOMATED SELF-TEST

The ACT3492 has been designed to fully support a wrap-around self-test which ensures a high degree of

fault coverage. The monolithic circuit includes all circuitry required to perform the self-test.

Self-test can be an on-line or off-line function which is initiated by simple subsystem intervention. The \overline{DRVINH} signal selects on-line or off-line testing. The circuit accomplishes the on-line test without accessing the MIL-STD-1553 data bus by providing an internal data path which connects the encoder circuitry directly to the decoder circuitry. The transceiver is inhibited during this on-line test. The off-line test is designed to include the transceiver as well as the protocol device. This mode will generally be useful as an off-line card test where no live bus is in use.

To initiate the self-test a word is placed in the Vector Word Latch, Loop Test Enable (\overline{LTEN}) is held low, and the Loop Test Trigger (\overline{LTTRIG}) signal is pulsed low. The primary bus will be tested with the word that resides in the Vector Word Latch, encoded then looped back, decoded and presented to the subsystem as a normal data transfer would be accomplished. The secondary bus is sequentially tested after the primary bus is completed via Request Bus A (REQBUSA) utilizing the same word residing in the Vector Word Latch. Upon completion of each test, pass/fail signals will be asserted reporting the results of the test. This test implementation verifies MIL-STD-1553 protocol compliance; proper sync character, 16 data bits, Manchester II coding, odd parity, contiguous word checking and a bit by bit comparison of the transmitted data. The self-test circuitry increases the fault coverage by insuring that the internal function blocks; encoder, decoder, and internal control circuitry are operating correctly. An effective data pattern to accomplish this is HEX AA55 since each bit is toggled, (8 bit internal highway) on a high/low byte basis. The total time required to complete the self-test cycle is 89 microseconds. The Loop Test Enable signal must remain in the low state throughout the diagnostic cycle.

Pin Description

Signal	Direction	Pin	Signal Description
RTAD 0-4	INPUT	K6,K5 J5,H5 F4	RT address lines - These should be hardwired by the user. RTAD4 is the most significant bit.
RTADPAR	INPUT	J6	RT address parity line - This must be hardwired by the user to give odd parity.
$\overline{\text{BIT DECODE}}$	INPUT	J4	Bitword Decode - When held low, prevents resetting TXTO Bit, HSFAIL Bit, and LTFAIL Bit in the BIT Word (as well as TF and SSF Bits in the Status Word) upon receipt of a Transmit Bit Word Mode Command.
BCSTEN 1	INPUT	F5	Broadcast command enable Bus 1 - When low the recognition of broadcast command is prevented on Bus 1.
BCSTEN 0	INPUT	G5	Broadcast command enable Bus 0 - When low the recognition of broadcast command is prevented on Bus 0.
6MCK (Clock)	INPUT	E4	6 Megahertz master clock.
IH 08 (LSB) IH 19 IH 210 IH 311 IH 412 IH 513 IH614 IH715 (MSB)	BIDIR	E9 D6 D7 A9 D8 B9 D9 C9	Internal Highway - Bi-directional 8 bit highway on which 16 bit words are passed in two bytes. IH 715 is the most significant bit of each byte, the most significant byte being transferred first. The highway should only be driven by the subsystem when data is to be transferred to the RT.
$\overline{\text{DTRQ}}$	OUTPUT	K10	Data Transfer Request - Goes low to request a data transfer between the ASIC and subsystem. Goes high at the end of the transfer.
$\overline{\text{DTAK}}$	INPUT	F6	Data Transfer Acknowledge - Goes low to indicate that the subsystem is ready for the data transfer.
IUSTB	OUTPUT	G6	Interface Unit Strobe - This is a double pulse strobe used to transfer the two bytes of data
H/ $\overline{\text{L}}$	OUTPUT	J9	High/Low - Indicates which byte of data is on the internal highway. Logic level "0" for least significant byte.
$\overline{\text{GBR}}$	OUTPUT	J7	Good Block Received - Pulses low for 500ns when a block of data has been received by the ASIC and has passed all the validity and error checks.
$\overline{\text{NBGT}}$	OUTPUT	G9	New Bus Grant - Pulses low whenever a new command is accepted by the ASIC.
MEREQ	INPUT	E8	Message Error Request - Positive-going edge will cause Message Error Bit in Status Word to be set.

Pin Description (Cont.)

Signal	Direction	Pin	Signal Description
TX/RX	OUTPUT	H10	Transmit/Receive - The state of this line informs the subsystem whether it is to transmit or receive data. The signal is valid while $\overline{\text{INCMD}}$ is low.
$\overline{\text{INCMD}}$	OUTPUT	K9	In Command - Goes low when the RT is servicing a valid command. The subaddress and word count lines are valid while the signal is low.
WC0-WC4	OUTPUT	B7,C8 A6,B6 A4	Word Count - These five lines specify the requested number of data words to be received or transmitted. Valid when $\overline{\text{INCMD}}$ is low.
SA0-SA4	OUTPUT	J10,K8 H7,K3 H2	Sub Address - These five lines are a label for the data being transferred. Valid when $\overline{\text{INCMD}}$ is low.
CWC0-CWC4	OUTPUT	H4,H8 K4,J8 K1	Current Word Count - These five lines define which data word in the message is currently being transferred.
$\overline{\text{SYNC}}$	OUTPUT	G7	Synchronize - Goes low when a synchronize mode code is being serviced.
$\overline{\text{VECTEN/DWEN}}$	OUTPUT	G8	Vector Word Enable/DataWord Enable - In the RT mode, this signal is provided to enable the contents of the vector word latch (which is situated in the subsystem) onto the ASIC's internal highway. This signal, when in the Bus Controller mode, is used to enable mode code data from the subsystem onto the internal highway.
$\overline{\text{RESET}}$	OUTPUT	C4	Reset - This line pulses low for 500ns on completion of the servicing of a valid and legal mode command to reset remote terminal.
$\overline{\text{SSERR}}$	INPUT	A5	Subsystem Error - By taking this line low, the subsystem can set the Subsystem Flag in the Status Word.
$\overline{\text{BUSY}}$	INPUT	C7	Busy - This signal should be driven low if the subsystem is not ready to perform a data transfer to or from the ASIC.
$\overline{\text{SERVREQ}}$	INPUT	A3	Service Request - This signal should be driven low to request an asynchronous transfer and left low until the transfer has taken place.
INCLK	OUTPUT	G10	Internal Clock (2 MHz) - This is made available for synchronization use by the subsystem if required. However, many of the outputs to the subsystem are asynchronous.
$\overline{\text{EOT}}$	OUTPUT	H9	End of Transmission - Goes low if a valid sync plus two data bits do not appear in time to be contiguous with preceding word.
$\overline{\text{RTADER}}$	OUTPUT	A1	Remote Terminal Address Error - This line goes low if an error is detected in the RT address parity of the selected receiver. Any receiver detecting an error in the RT address will turn itself off.

Pin Description (Cont.)

Signal	Direction	Pin	Signal Description
HSFAIL	OUTPUT	B5	Handshake Failure - This line pulses low if the allowable time for $\overline{\text{DTAK}}$ response has been exceeded during the ASIC/subsystem data transfer handshaking.
LSTCMD/CWEN	OUTPUT	D5	Last Command/Command Word Enable - This line pulses low when servicing a valid and legal mode command to transmit last command. When in RT mode this line must not be used to enable data from the subsystem. This line also pulses low, when in the Bus Control mode, when a command word is required for transmission.
STATEN/ STATSTB	OUTPUT	K7	Status Enable/Status Strobe - This line pulses low to enable the status word onto the internal highway for transmission. When in RT mode this line must not be used to enable data from the subsystem. This line also pulses high, when in the Bus Control mode, to strobe received status words into the subsystem. When $\overline{\text{PASM0N}}$ is true this line pulses high for Command and Status words.
STAT UPDATE	INPUT	E6	Status Update - When held low, causes TF or SSF to appear in Status Word response to Transmit Status or Transmit Last Command issued immediately after fault occurrence
BITEN/ RMDSTB	OUTPUT	C6	Built In Test Enable/Receive Mode Data Strobe - This line pulses low when servicing a valid and legal mode command to transmit the internal BIT word. This signal is for information only and must not be used to enable data from the subsystem. This line also pulses high when in the Bus Control mode when mode data is received to be passed to the subsystem and when data is passed to the subsystem during $\overline{\text{PASM0N}}$.
DWSYNC	OUTPUT	G3	Data Word Sync - This line goes low if a data word sync and two Manchester biphase bits are valid.
ENABLE	INPUT	E7	Enable - When held low, enables Bit Decode, Next Status, and Status Update program lines.
CMSYNC	OUTPUT	G4	Command Word Sync - This line goes low if a command word sync and two Manchester biphase bits are valid.
NDRQ	OUTPUT	D10	No Data Required - This line goes low if the encoder transmit buffer is full i.e. another word is going to be transmitted. This signal is for information only and must not be used to enable data from the subsystem.
NEXT STAT	INPUT	A10	Next Status - When held low, causes TF or SSF to appear in very next Status Word after fault occurrence (except for Transmit Status or Transmit Last Command).
MASTER RESET	INPUT	B8	Master Reset - A logic low on this input (100 nSec minimum) will reset the interface.

Pin Description (Cont.)

Signal	Direction	Pin	Signal Description
$\overline{\text{PASM}}\text{ON}$	INPUT	F8	Passive Monitor - When functioning as a Bus Controller this line acts as a passive monitor select. The active going edge of this line will cause the REQBUS lines to be latched and that bus, now selected will be monitored so long as $\overline{\text{PASM}}\text{ON}$ remains low. All traffic on the bus will be handed, after validation, to the subsystem via STATSTB for status and commands words, and RMDSTB for data words.
$\overline{\text{BCOP}}\text{STB}$	INPUT	F7	Bus Controller Operation Strobe - When functioning as a Bus Controller a low going pulse on this line will initiate the selected bus controller operation on the requested bus, using BCOPA&B and REQBUS A&B.
BCOPA	INPUT	B10	Bus Control Operation A - Least significant bit of the bus controller operation select lines.
BCOPB	INPUT	C10	Bus Control Operation B - Most significant bit of the bus controller operation select lines.
REQBUS A	BIDIR	E5	Request Bus A - This line, when in RT mode, is the least significant bit of the bus request lines which specify the origin of the command, i.e. they are sources. When in BC mode these lines are sinks and specify which bus is to be used for the next command.
REQBUS B	BIDIR	H6	Request Bus B - Most significant bit of the bus request lines. (See above for description.)
RT/ $\overline{\text{BC}}$	INPUT	B4	Remote Terminal/Bus Control - This line when high causes the ASIC to function as a remote terminal. When low the ASIC functions as a bus controller or passive monitor.
$\overline{\text{DBC}}\text{ACC}$	INPUT	B3	Dynamic Bus Control Accept - This line should be permanently tied low if a subsystem is able to accept control of the bus if offered.
$\overline{\text{LTF}}\text{AIL}$	OUTPUT	E2	Loop Test Fail - This line goes low if any error in the transmitted waveform is detected or if any parity error in the hardwired RT address is detected.
$\overline{\text{ERR}}\text{OR}$	OUTPUT	F2	Error - This line latches low if a Manchester or parity error is detected. It is reset by the next $\overline{\text{CMS}}\text{YNC}$ (RT mode) and also by $\overline{\text{RTO}}$ in the BC mode.
$\overline{\text{RTO}}$	OUTPUT	F3	Reply Time Out - This signal will pulse low whenever the reply time for a transmitting terminal has been exceeded. This line is intended for the bus controller use.
$\overline{\text{TX}}\text{TO}$	OUTPUT	C3	Transmitter Time Out - This line latches low if the transmitter time out limits are exceeded.
$\overline{\text{PAR}}\text{ER}$	OUTPUT	D3	Parity Error - This line will pulse low if a parity error is detected by the decoder.

Pin Description (Cont.)

Signal	Direction	Pin	Signal Description
MANER	OUTPUT	E3	Manchester Error - This line will pulse low if a Manchester error is detected by the decoder.
DBCREQ	OUTPUT	C5	Dynamic Bus Control Request - This line will pulse low when the status reply for a mode code Dynamic Bus Control has finished where the accept bit was set.
VALD	OUTPUT	C2	Valid Data - This line will pulse low when a valid data word is received.
DRVINH	INPUT	H3	Driver Inhibit - Selects on-line or off-line testing during automated self test. When high self test is on-line. Must be high when LTEN is high.
LTEN	INPUT	A7	Loop Test Enable - Enables automated self-test when low. Normally high.
LTTRIG	INPUT	A8	Loop Test Trigger - When pulsed low while LTEN is low automated self-test is initiated. LTEN pulse width should be $100\text{ns} \leq \text{PW} \leq 5\mu\text{s}$.
TX/RX A1 TX/RX A2	BIDIR	B2 B1	Bus A Transmit/Receive - HIGH output to the primary side of the coupling transformer that connects to the A Channel of the 1553 Bus.
$\overline{\text{TX/RX A1}}$ $\overline{\text{TX/RX A2}}$	BIDIR	D2 D1	Bus A Transmit/Receive - LOW output to the primary side of the coupling transformer that connects to the A Channel of the 1553 Bus.
TX/RX B1 TX/RX B2	BIDIR	G1 G2	Bus B Transmit/Receive - HIGH output to the primary side of the coupling transformer that connects to the B Channel of the 1553 Bus.
$\overline{\text{TX/RX B1}}$ $\overline{\text{TX/RX B2}}$	BIDIR	J1 J2	Bus B Transmit/Receive - LOW output to the primary side of the coupling transformer that connects to the B Channel of the 1553 Bus.
+5VAA +5VAB	POWER	E1 A2	+5V Input Power Supply connection for the A Channel Transceiver
+5VBA +5VBB	POWER	K2 F1	+5V Input Power Supply connection for the B Channel Transceiver
+5VLogic	POWER	E10	+5V Input Power Supply connection for the Digital Protocol section.
GND A	POWER	C1	Power Supply return for the A Channel Transceiver.
GND B	POWER	H1	Power Supply return for the B Channel Transceiver.
DIGGND 1 DIGGND 2	POWER	F9 F10	Power Supply return for the Digital Protocol section.
CASE			Connected to DIGGND1 and DIGGND2

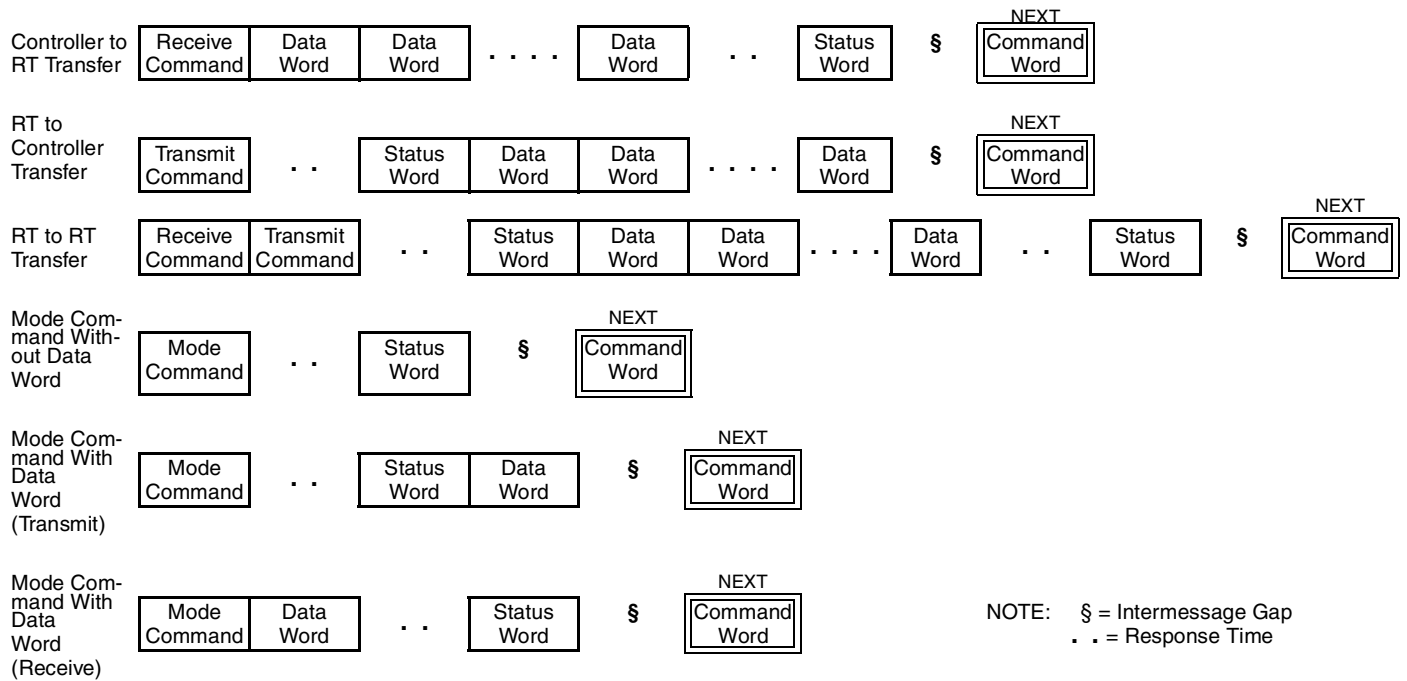
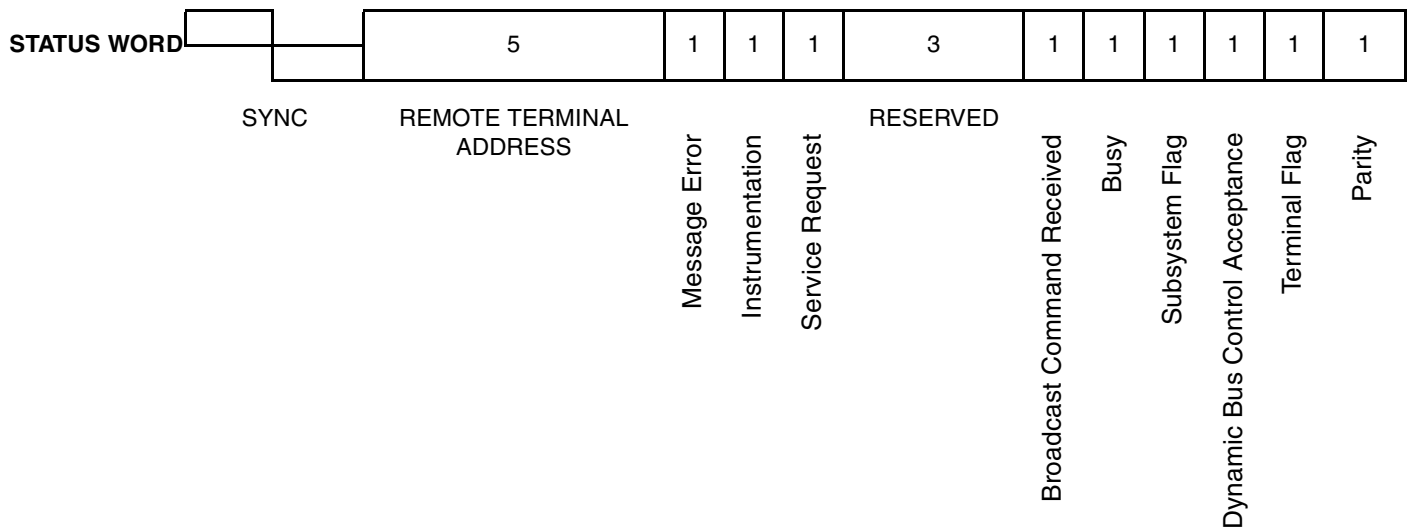
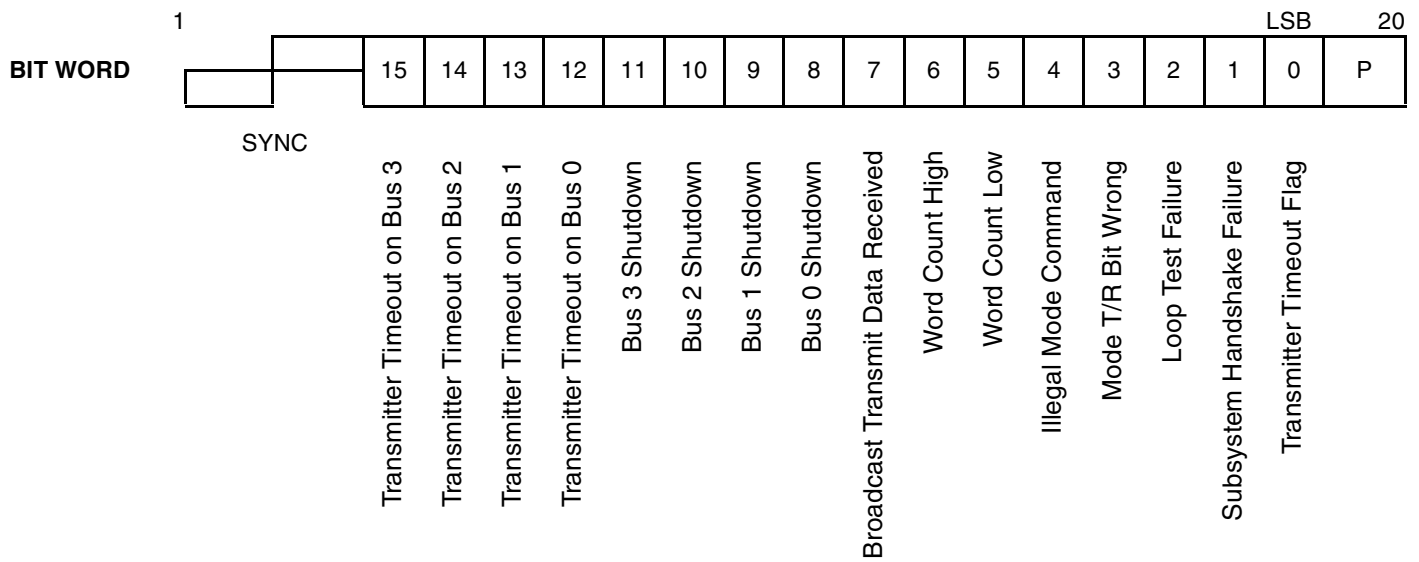
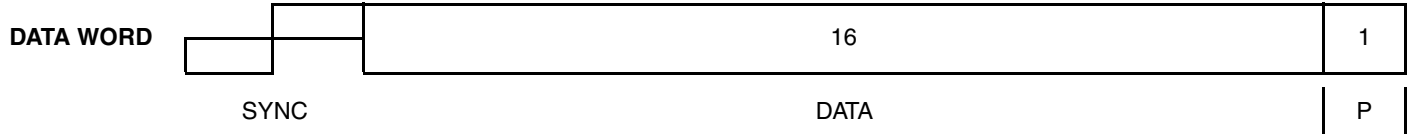
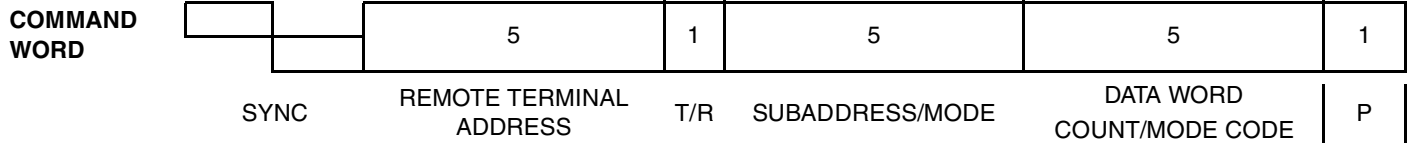
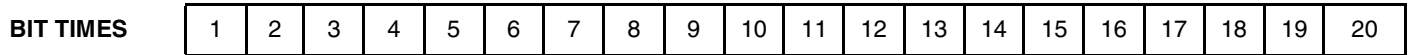


Figure 1 – Typical Message Formats

T/R Bit	Mode Code	Function	Associated Data Word	Broadcast Command Allowed
1	00000	Dynamic Bus Control	No	No
1	00001	Synchronize	No	Yes
1	00010	Transmit Status Word	No	No
1	00011	Initiate Self Test	No	Yes
1	00100	Transmitter Shutdown	No	Yes
1	00101	Override Transmitter Shutdown	No	Yes
1	00110	Inhibit Terminal Flag Bit	No	Yes
1	00111	Override Inhibit Terminal Flag Bit	No	Yes
1	01000	Reset Remote Terminal	No	Yes
1	01001	Reserved	No	TBD
	↓	↓	↓	↓
1	01111	Reserved	No	TBD
1	10000	Transmit Vector Word	Yes	No
0	10001	Synchronize	Yes	Yes
1	10010	Transmit Last Command	Yes	No
1	10011	Transmit BITWord	Yes	No
0	10100	Selected Transmitter Shutdown	Yes	Yes
0	10101	Override Selected Transmitter Shutdown	Yes	Yes
1 or 0	10110	Reserved	Yes	TBD
	↓	↓	↓	↓
1 or 0	11111	Reserved	Yes	TBD

Figure 2 – Assigned Mode Codes



Note: T/R – Transmit/Receive
P – Parity

Figure 3 – Word Formats

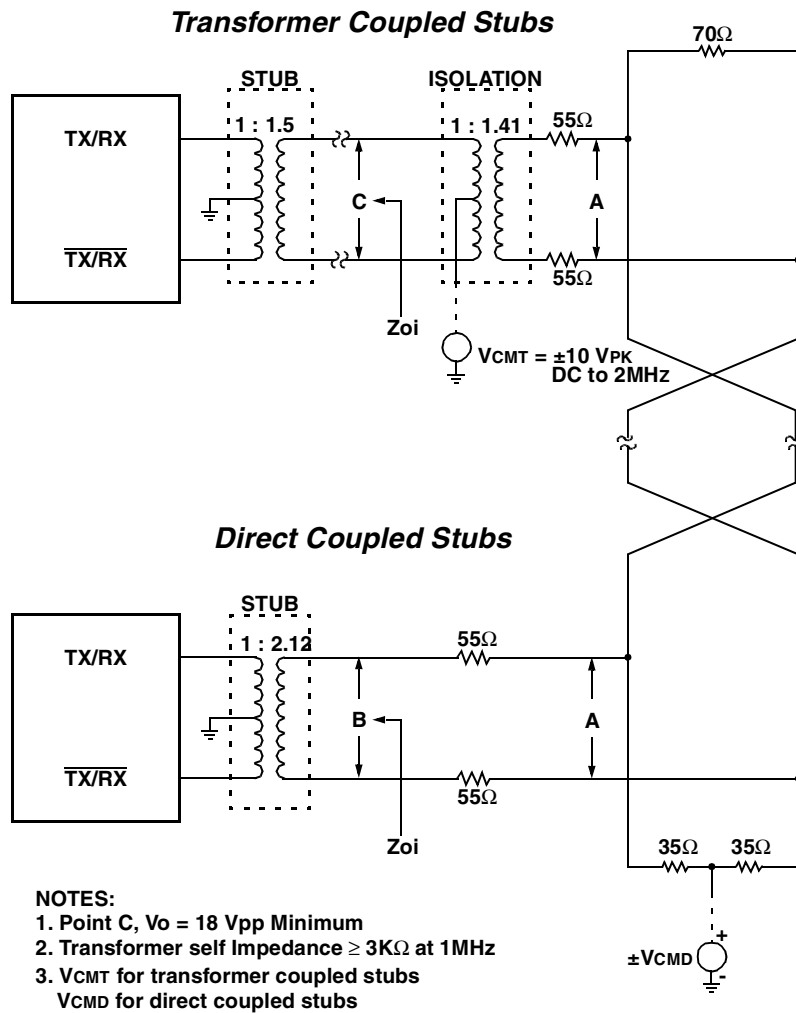


Figure 4 – TRANCEIVER SIGNAL POINTS

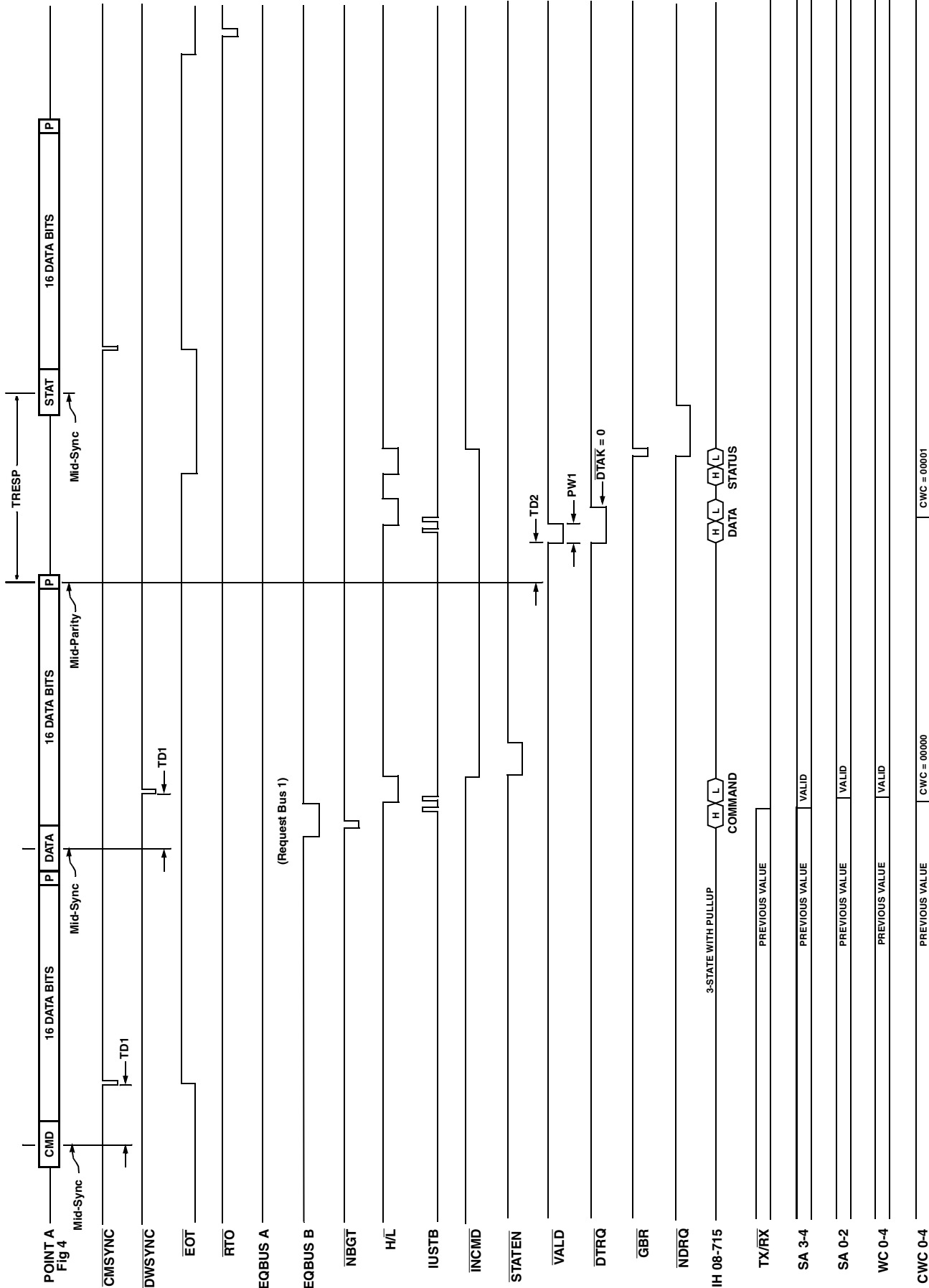


Figure 5 – RT RECEIVE 1 WORD (NON MODE)

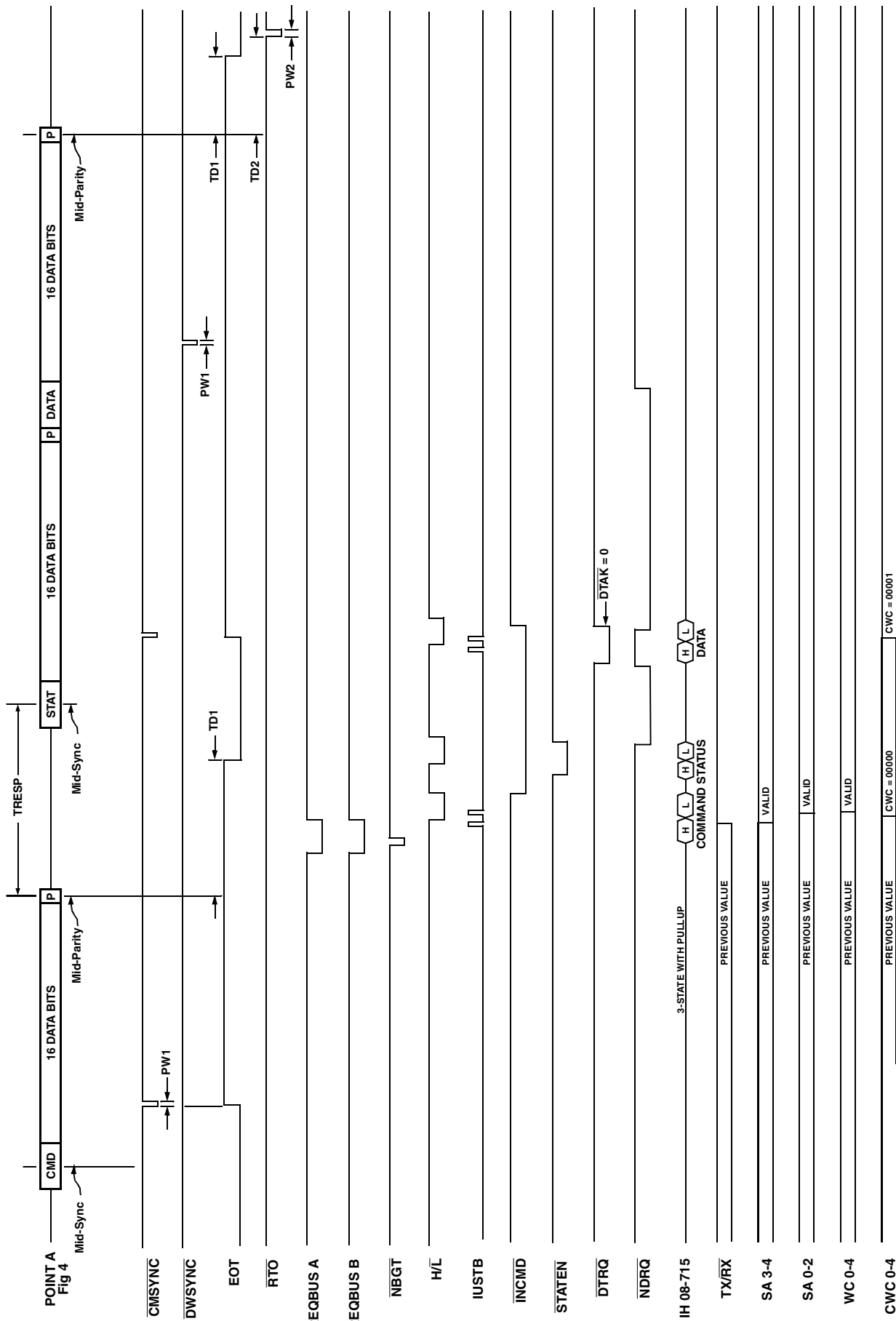


Figure 6 – RT TRANSMIT 1 WORD (NON MODE)

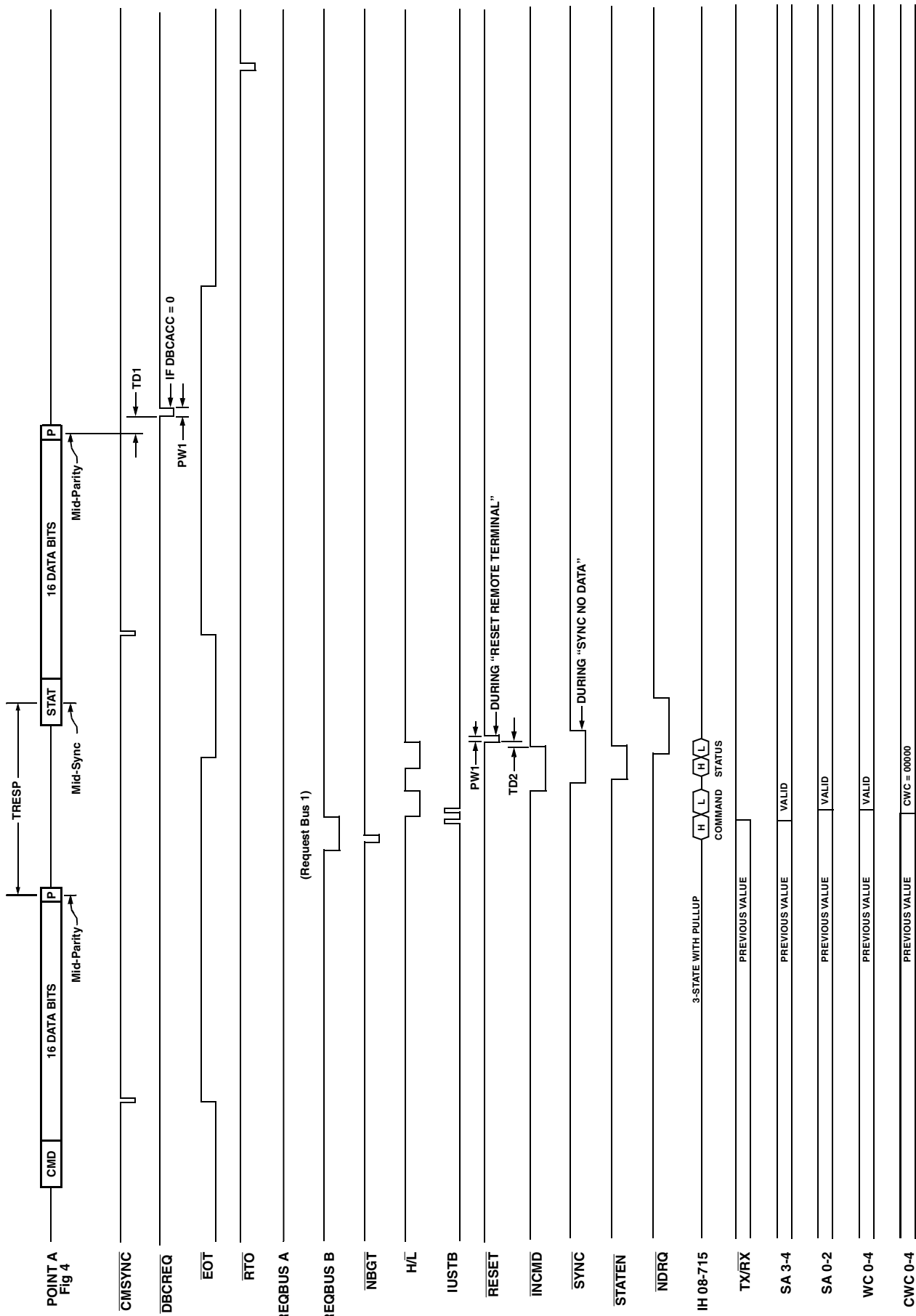


Figure 7 – RT TRANSMIT MODE (NO DATA)

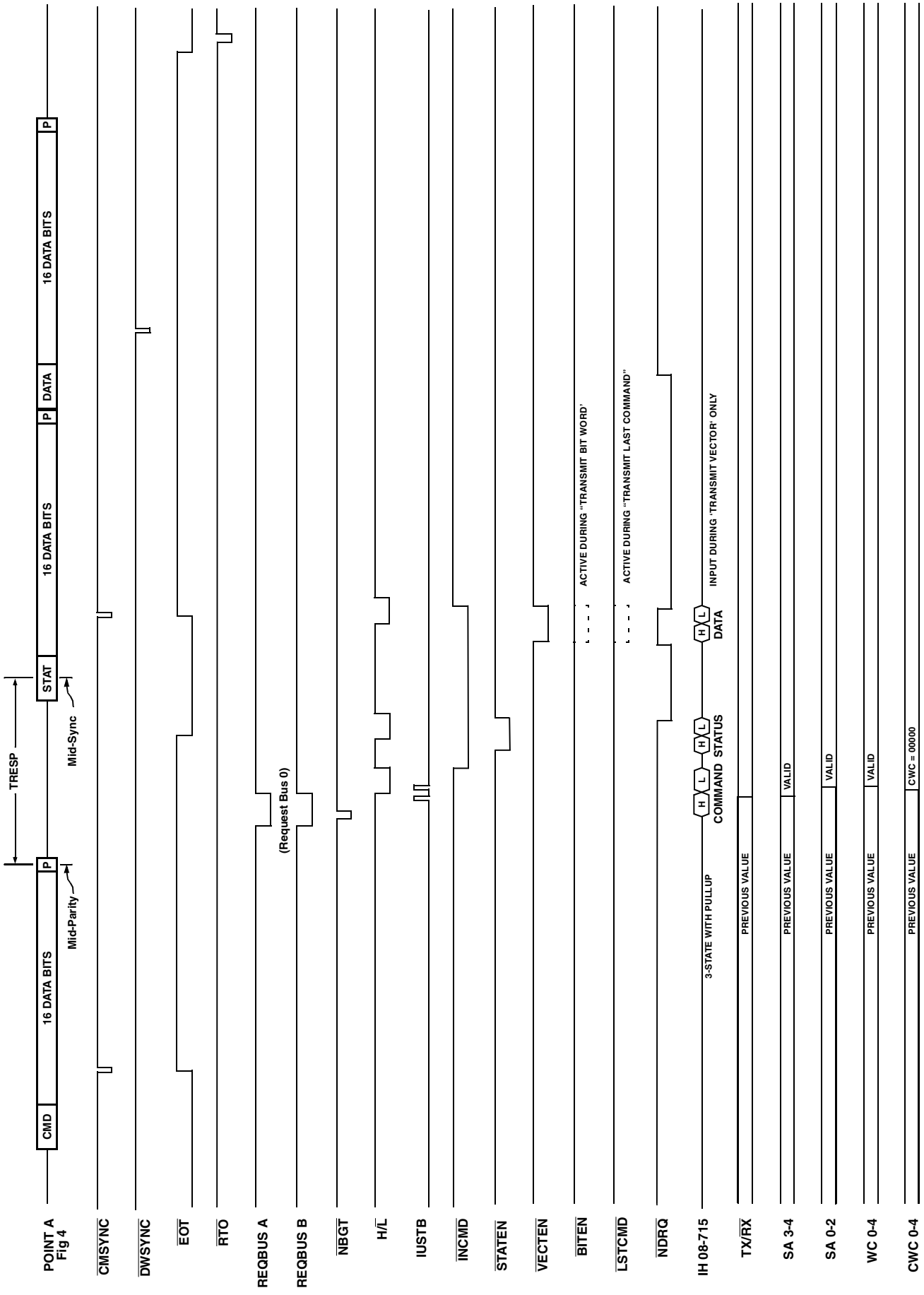


Figure 8 – RT TRANSMIT MODE (WITH DATA)

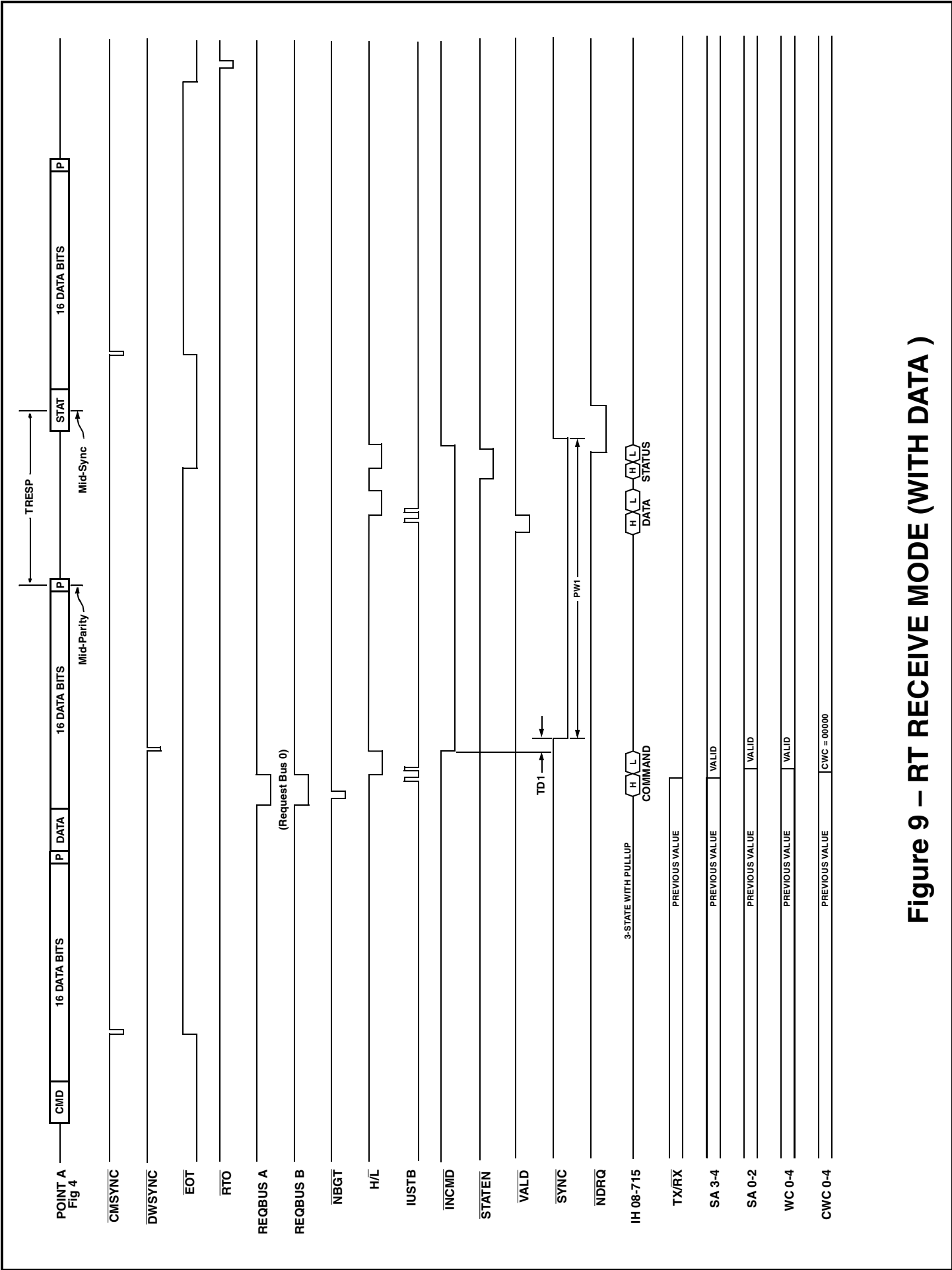


Figure 9 – RT RECEIVE MODE (WITH DATA)

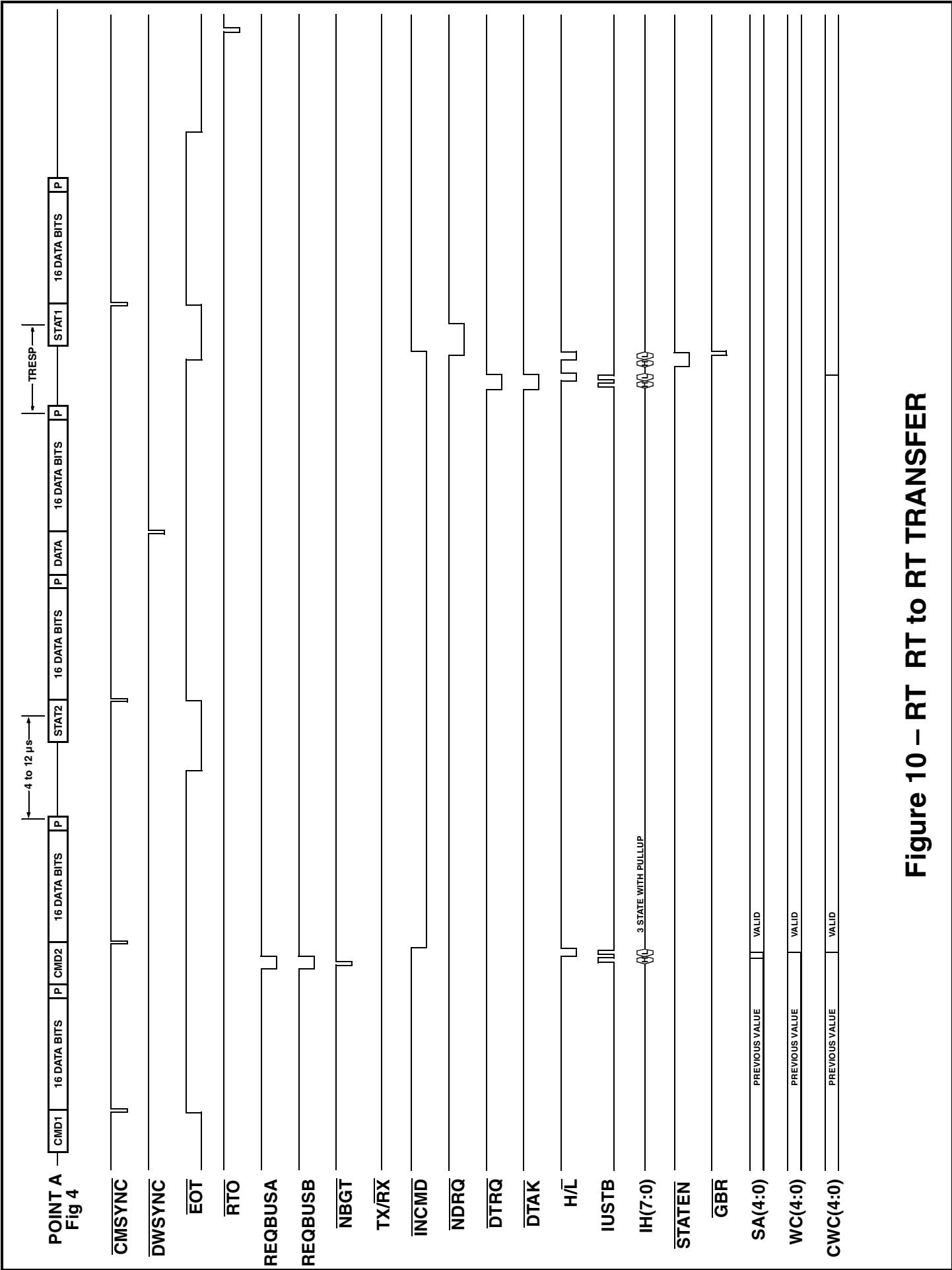


Figure 10 – RT to RT TRANSFER

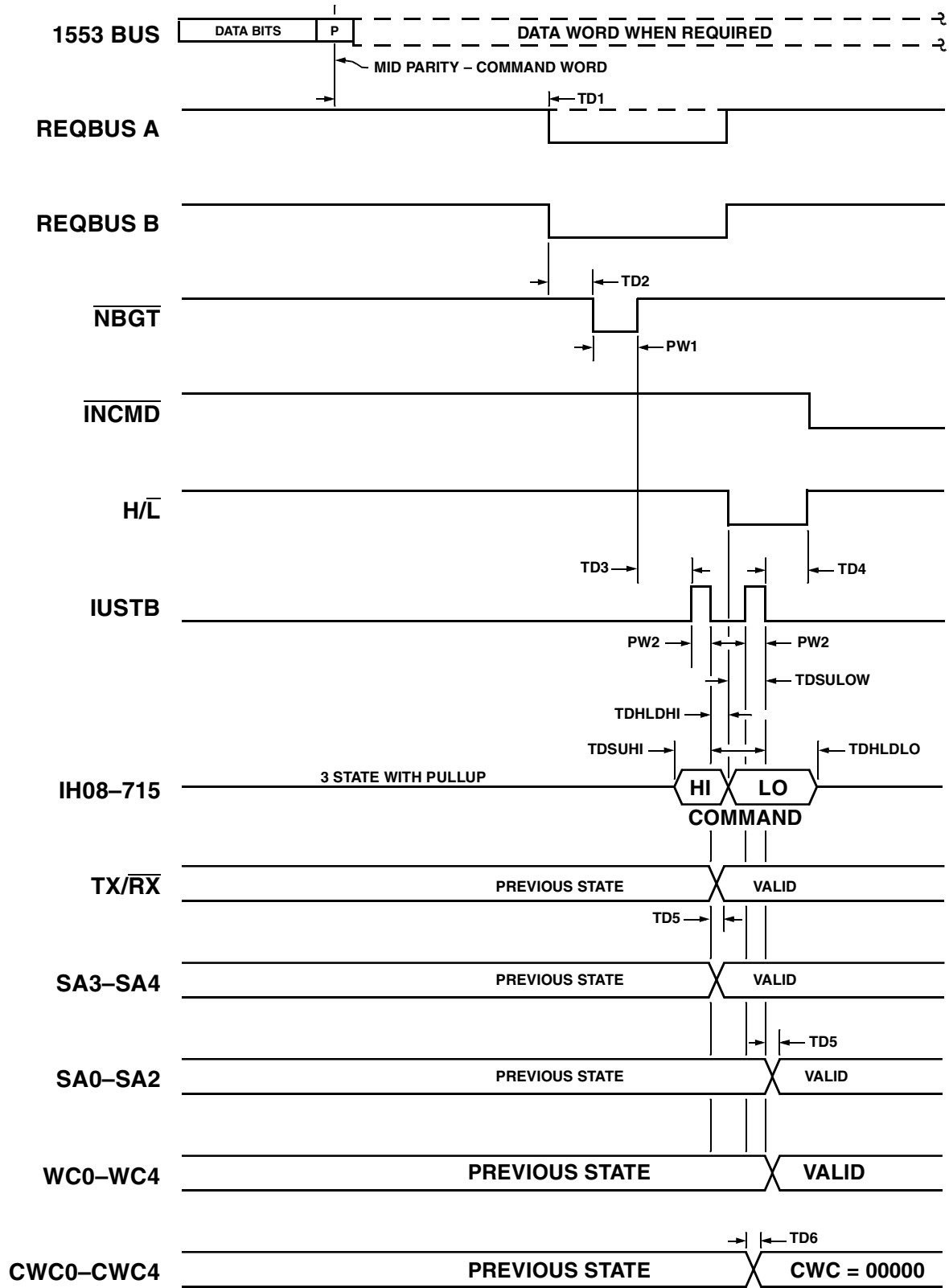


Figure 11 – COMMAND WORD TRANSFER (ALL)

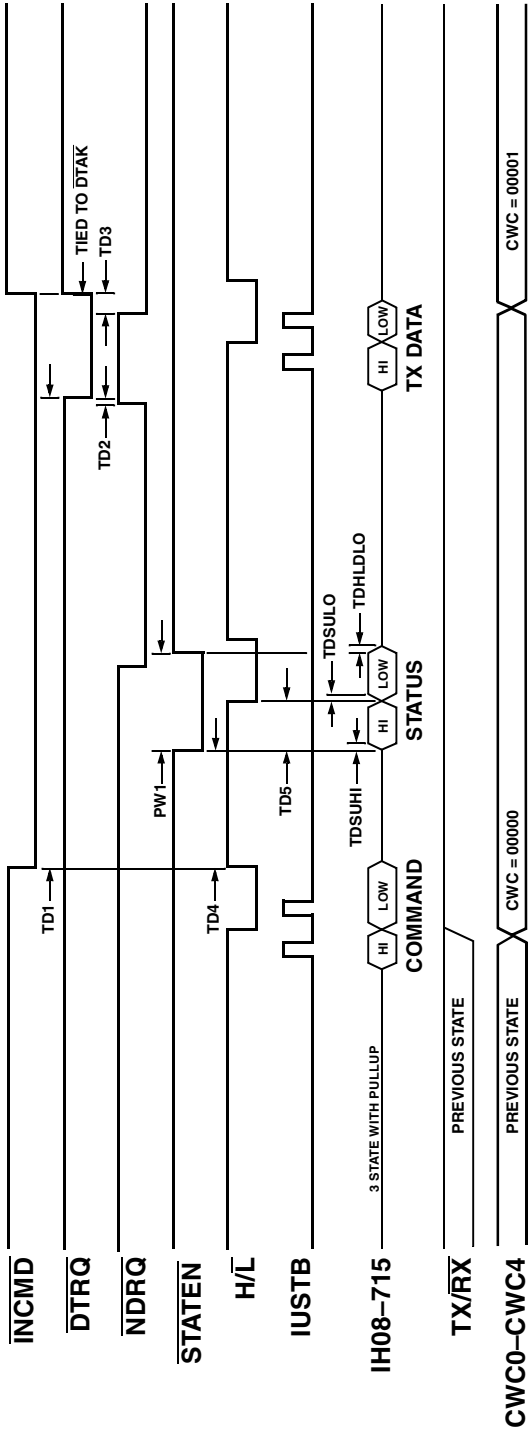


Figure 12 – RT TRANSMIT COMMAND SERVICE (NON-MODE)

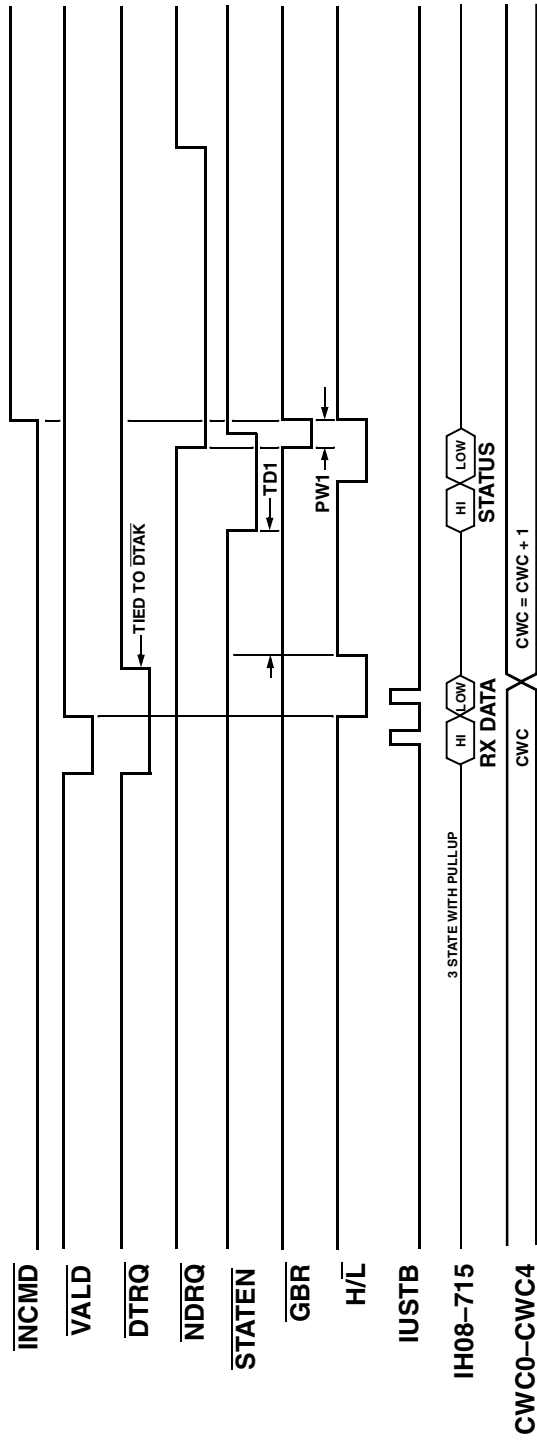


Figure 13 – RT RECEIVE COMMAND SERVICE (NON-MODE)

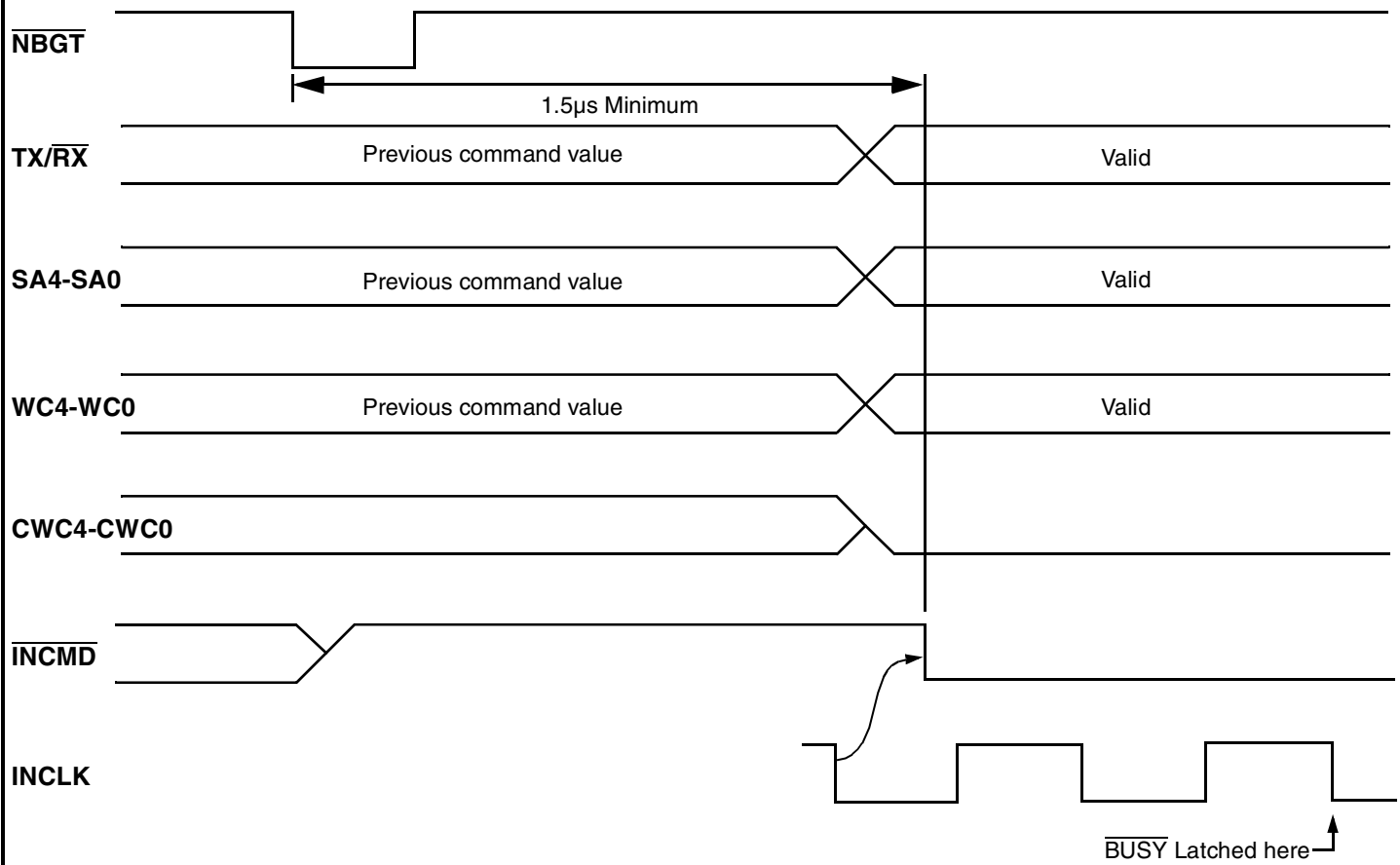


Figure 14 – NEW COMMAND INITIALIZATION

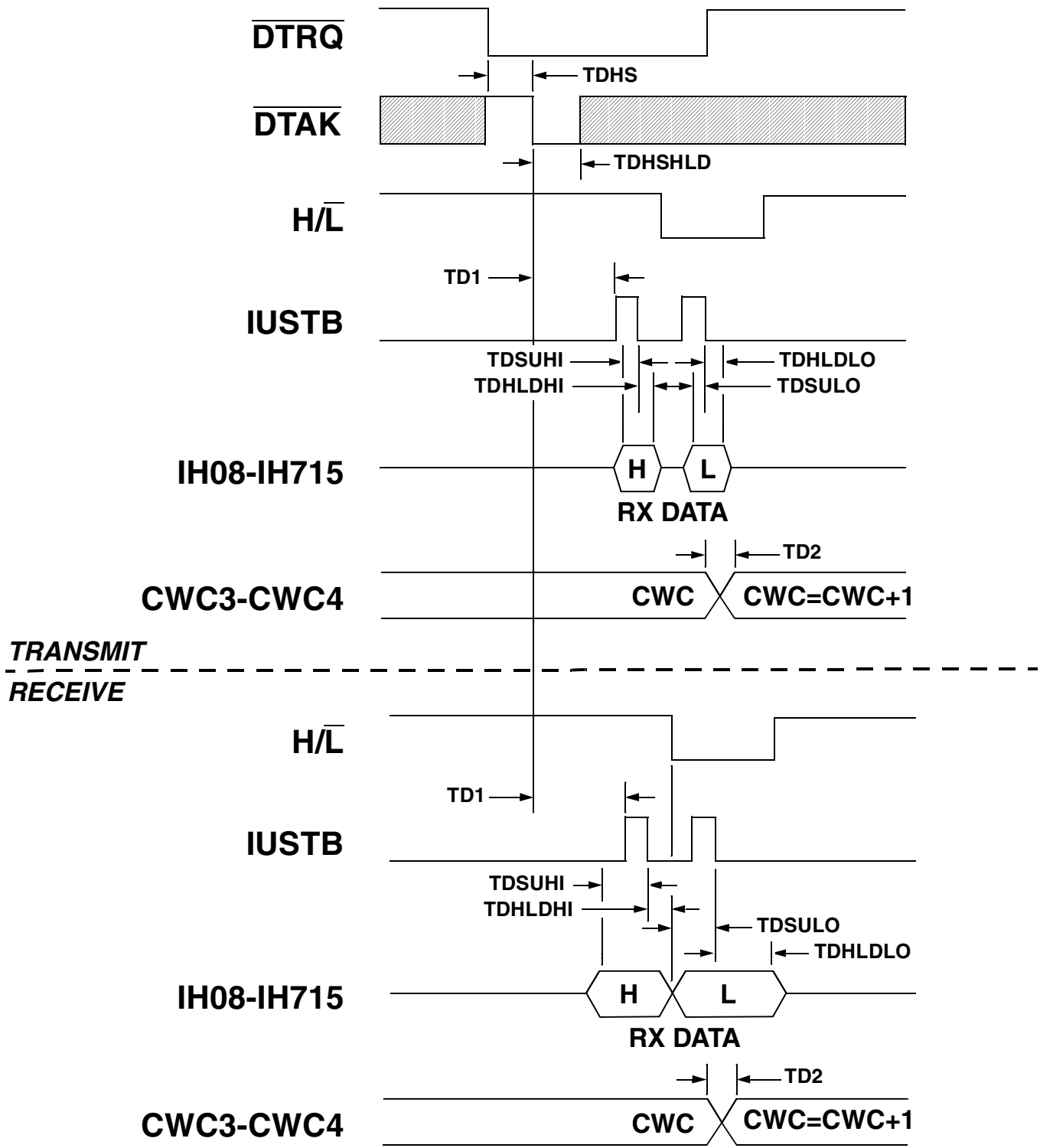


Figure 15 – DATA HANDSHAKE TRANSMIT / RECEIVE

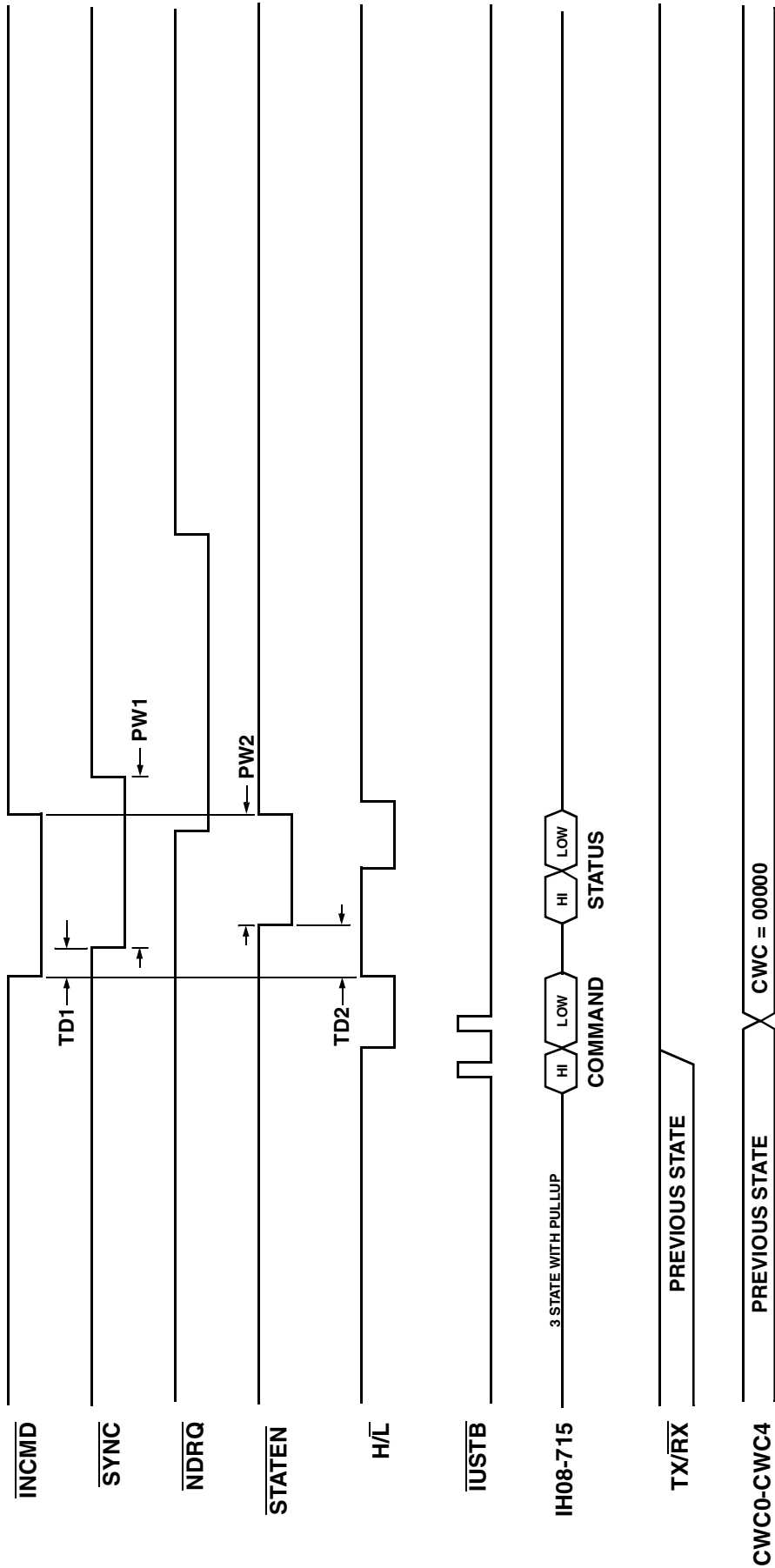


Figure 16 – RT TRANSMIT MODE SERVICE (NO DATA)

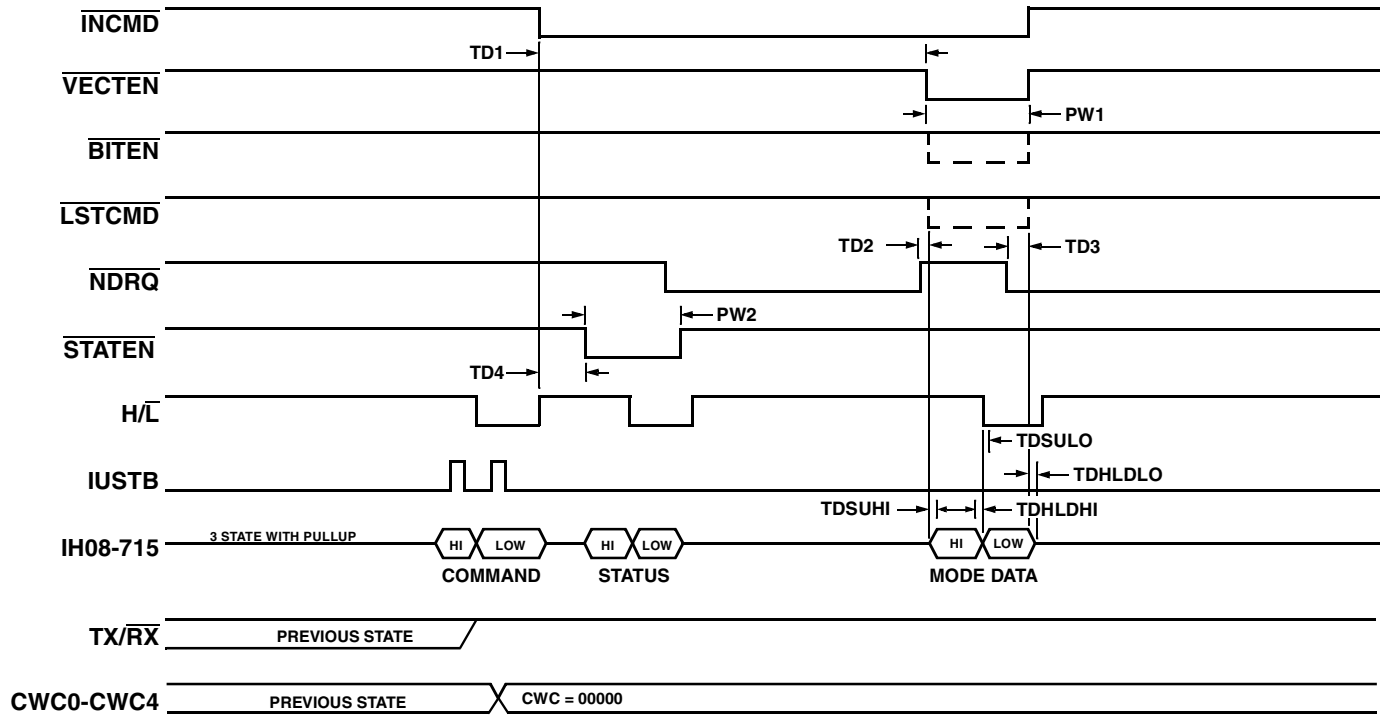


Figure 17 – RT TRANSMIT MODE SERVICE (WITH DATA)

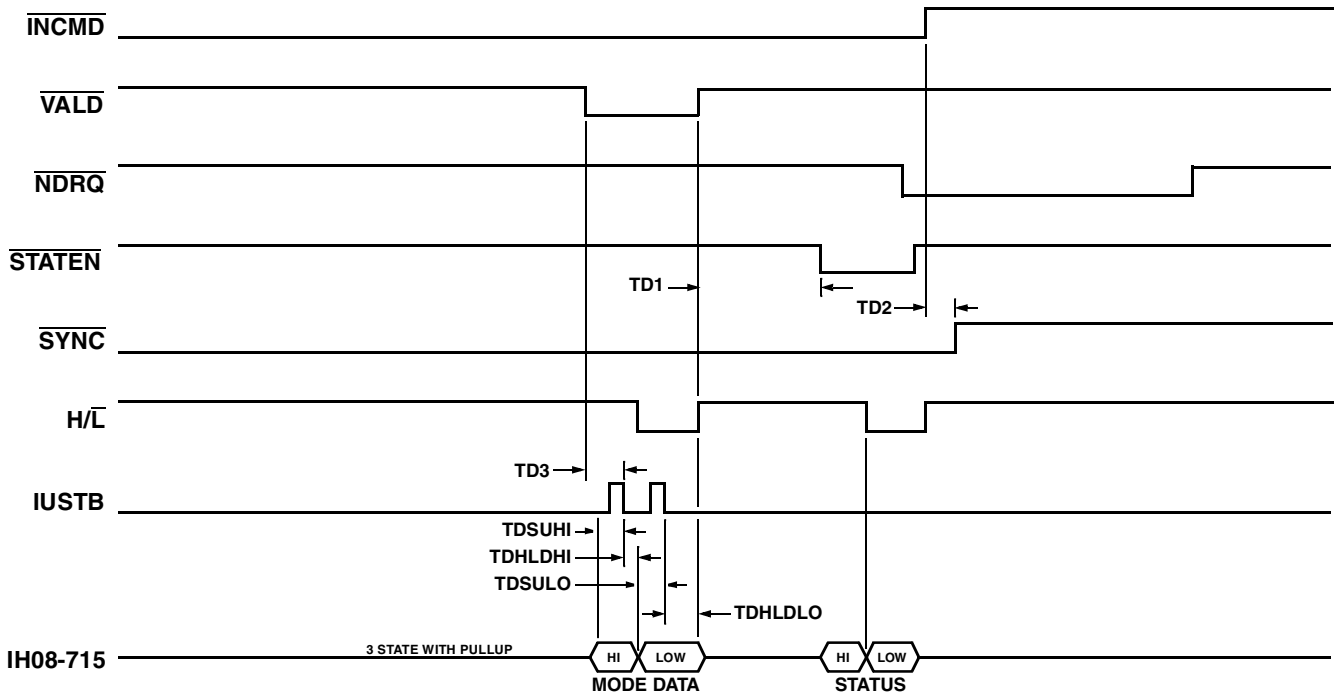


Figure 18 – RT RECEIVE MODE SERVICE (WITH DATA)

PARAMETRICS

Test Conditions:

$V_{CC} = +5V \pm 10\%$, $V_{SS} = 0$, $R_L(\text{PULL-UP}) = 1.6K\Omega$, $R_L(\text{PULL-DOWN}) = 5K\Omega$, $C_L = 20 \text{ pf}$ (Including Test Jig)}

TRANSMIT (NON MODE)

(See Figure 6)

SYMBOL	LIMITS		
	MIN	MAX	UNITS
TRESP	10.5	11.75	μs
PW1	275	550	ns
PW2	475	525	ns
TD1	6.5	7.0	μs
TD2	18.5	19	μs

RECEIVE (NON MODE)

(See Figure 5)

SYMBOL	LIMITS		
	MIN	MAX	UNITS
TRESP	9.0	10	μs
PW1	875	1325	ns
TD1	3.65	3.95	μs
TD2	2.8	3.5	μs

TRANSMIT COMMAND SERVICE (NON MODE)

(See Figure 12)

SYMBOL	LIMITS		
	MIN	MAX	UNITS
PW1	1.4	1.6	μs
TD1	6.7	6.9	μs
TD2	10	75	ns
TD3	225	275	ns
TD4	1.7	1.8	μs
TD5	700	800	ns

RECEIVE COMMAND (NON MODE) SERVICE

(See Figure 13)

SYMBOL	LIMITS		
	MIN	MAX	UNITS
PW1	400	600	ns
TD1	700	800	ns

COMMAND WORD TRANSFER (ALL)
(See Figure 11)

SYMBOL	LIMITS		
	MIN	MAX	UNITS
PW1	475	525	ns
PW2	225	275	ns
TD1	3.0	3.4	μs
TD2	275	350	ns
TD3	50	500	ns
TD4	450	550	ns
TD5	-	75	ns
TD6	50	-	ns
TDSUHI	400	-	ns
TDHLDHI	150	-	ns
TDSULO	400	-	ns
TDHLDLO	150	-	ns

TRANSMIT MODE (WITH DATA)
(See Figure 8)

SYMBOL	LIMITS		
	MIN	MAX	UNITS
TRESP	9.5	10.5	μs

DATA HANDSHAKE (See Figure 15)

SYMBOL	LIMITS		
	MIN	MAX	UNITS
TRANSMIT			
TDHS (TX)	0	13.5	μs
TDHSHLD	750	-	ns
TDSUHI	25	-	ns
TDHLDHI	25	-	ns
TDSULO	25	-	ns
TDHLDLO	25	-	ns
TD1	675	800	ns
TD2	50	-	ns
RECEIVE			
TDHS (RX)	0	1.5	μs
TDHSHLD	750	-	ns
TDSUHI	400	-	ns
TDHLDHI	150	-	ns
TDSULO	400	-	ns
TDHLDLO	150	-	ns
TD1	675	800	ns
TD2	50	-	ns

RECEIVE MODE (WITH DATA) (See Figure 9)

SYMBOL	LIMITS		
	MIN	MAX	UNITS
TRESP	9.0	10	μs
PW1	21.75	23.0	μs
TD1	200	300	ns

**TRANSMIT MODE SERVICE
(WITH DATA) (See Figure 17)**

SYMBOL	LIMITS		
	MIN	MAX	UNITS
PW1	1.4	1.6	μs
PW2	1.4	1.6	μs
TD1	6.2	6.3	μs
TD2	400	600	ns
TD3	10	-	μs
TD4	700	800	ns
TDSUHI	-	100	ns
TDHLDHI	0	-	ns
TDSULO	-	100	ns
TDHLDLO	0	-	ns

**RECEIVE MODE SERVICE
(WITH DATA) (See Figure 18)**

SYMBOL	LIMITS		
	MIN	MAX	UNITS
TD1	725	825	ns
TD2	680	760	ns
TD3	375	825	ns
TDSUHI	400	-	ns
TDHLDHI	150	-	ns
TDSULO	400	-	ns
TDHLDLO	150	-	ns

**TRANSMIT MODE (NO DATA)
(See Figure 7)**

SYMBOL	LIMITS		
	MIN	MAX	UNITS
TRESP	9.5	11	μs
PW1	400	600	ns
TD1	600	1000	ns
TD2	150	275	ns

**TRANSMIT MODE SERVICE
(NO DATA) (See Figure 16)**

SYMBOL	LIMITS		
	MIN	MAX	UNITS
PW1	2.45	2.55	μs
PW2	1.4	1.6	μs
TD1	450	550	ns
TD2	700	800	ns

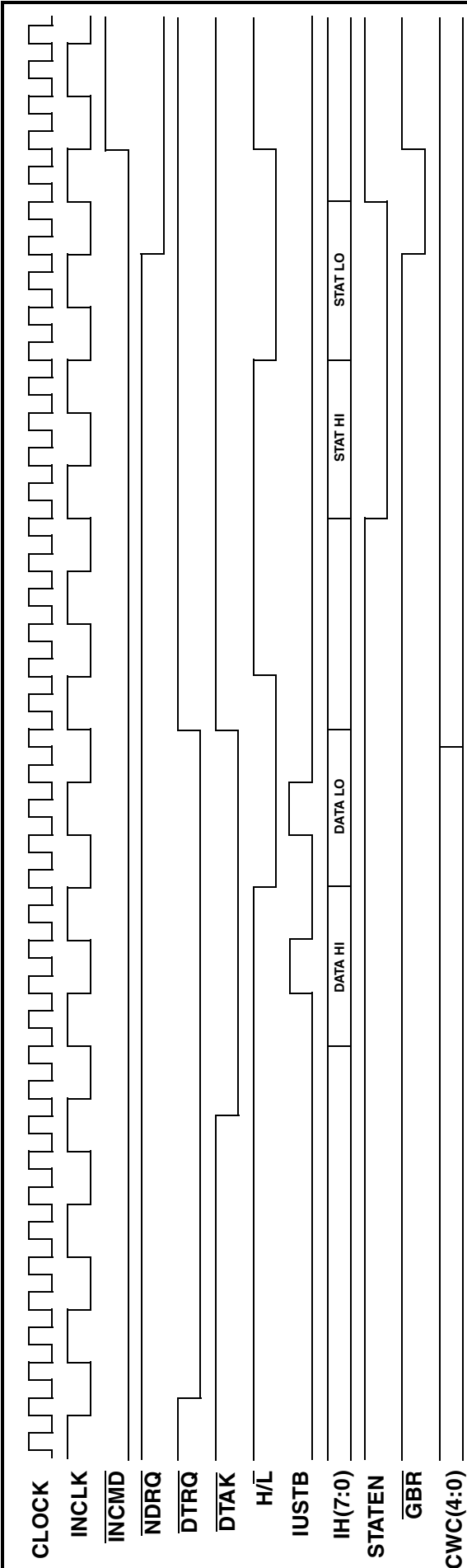


Figure 19 INCLK TIMING – RECEIVE (DTAK DELAYED)

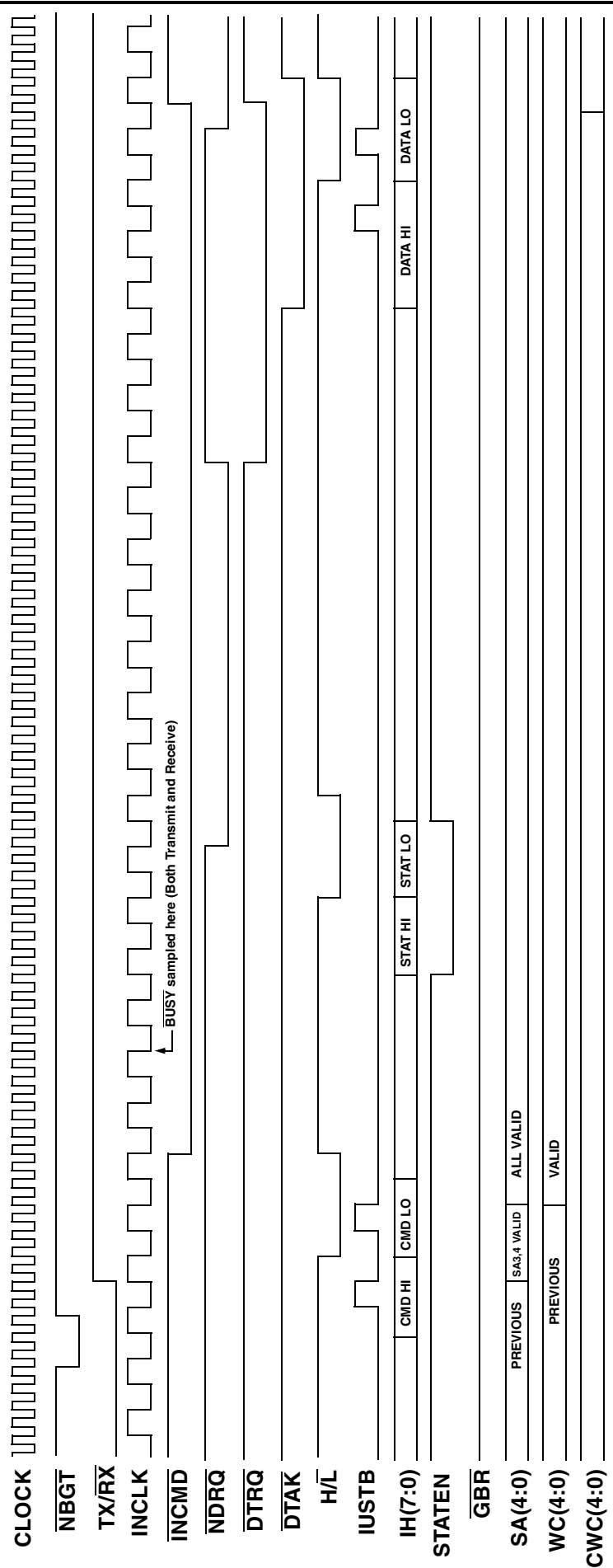


Figure 20 INCLK TIMING – TRANSMIT (DTAK DELAYED)

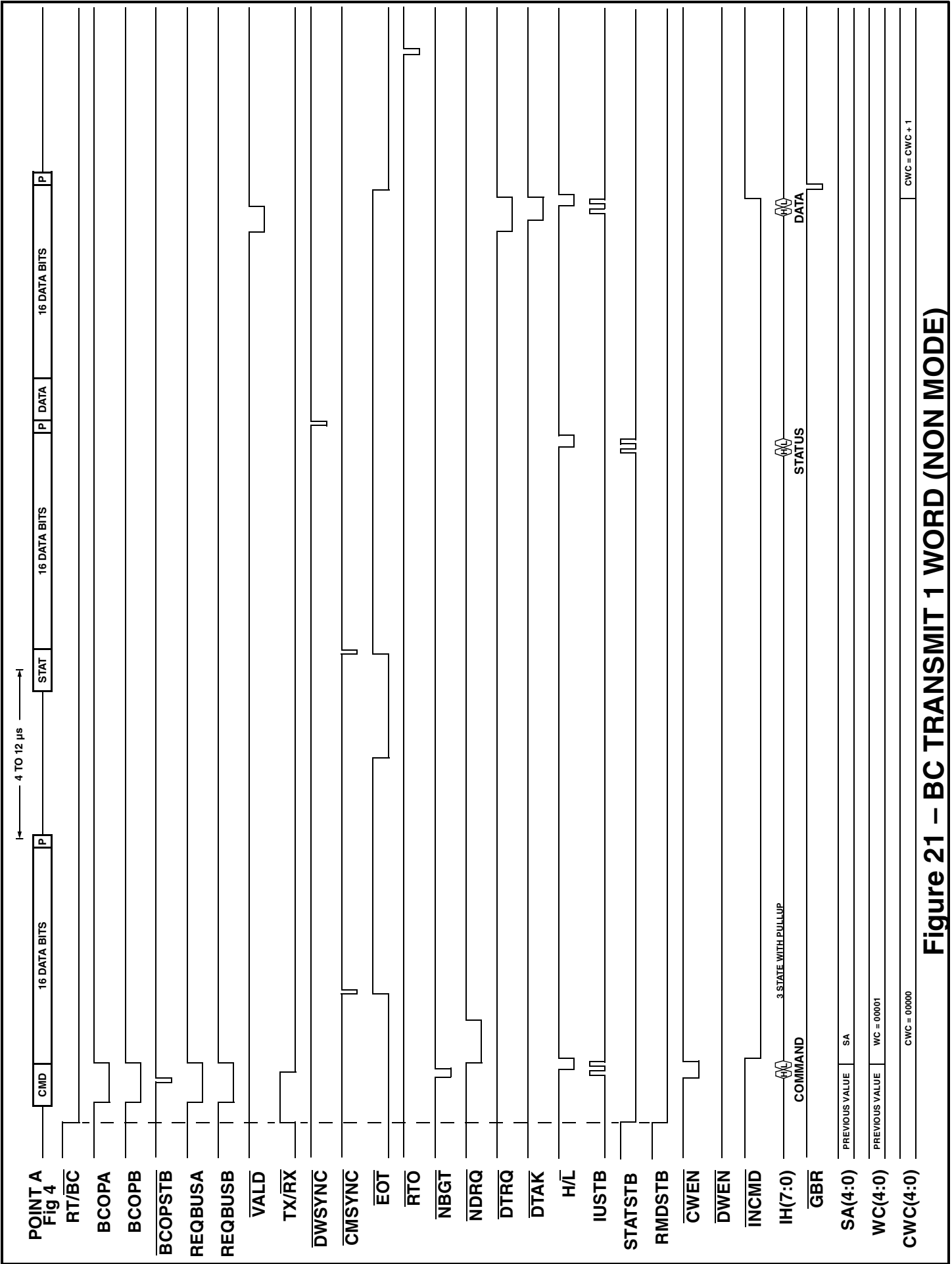


Figure 21 – BC TRANSMIT 1 WORD (NON MODE)

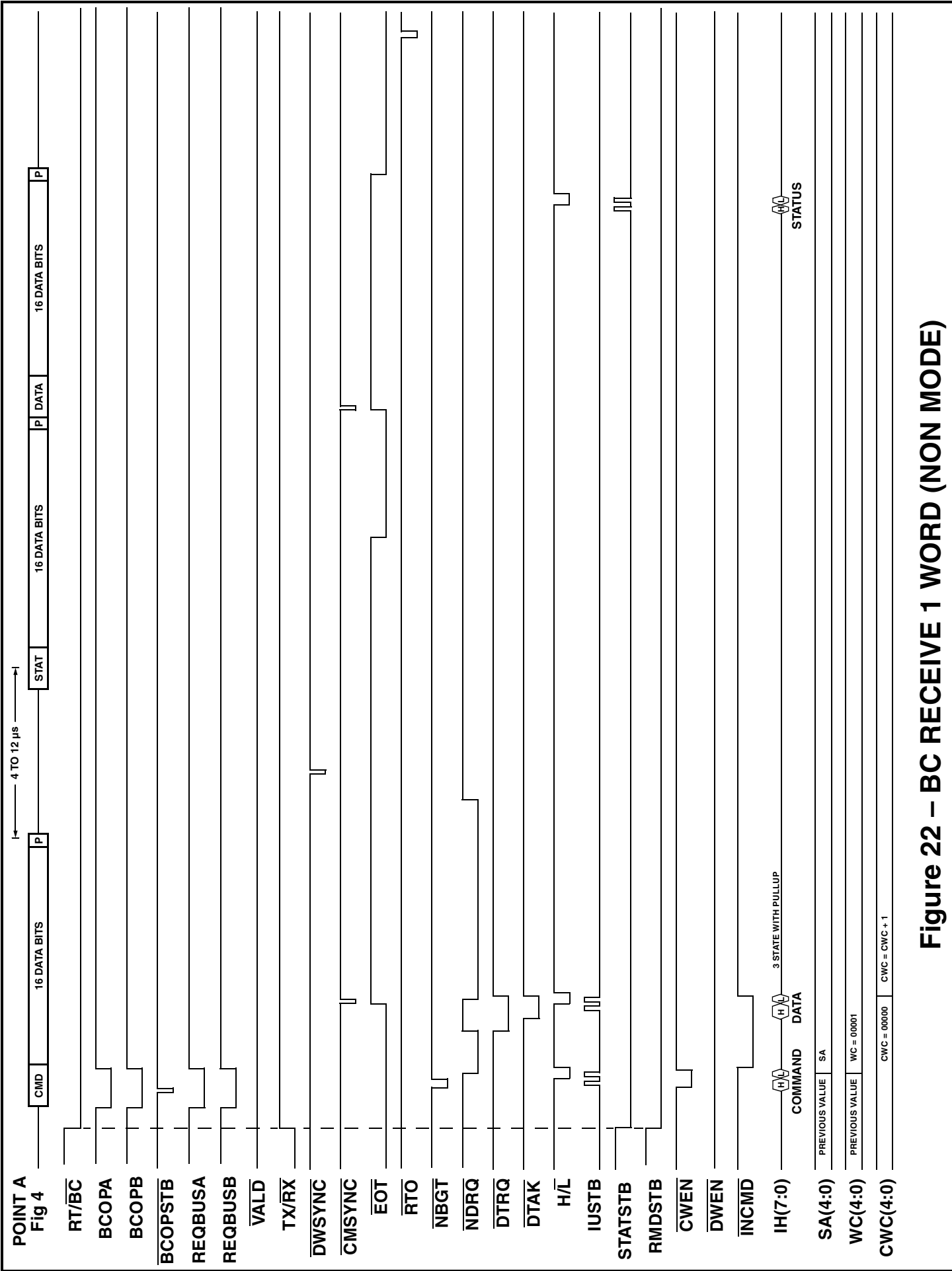


Figure 22 – BC RECEIVE 1 WORD (NON MODE)

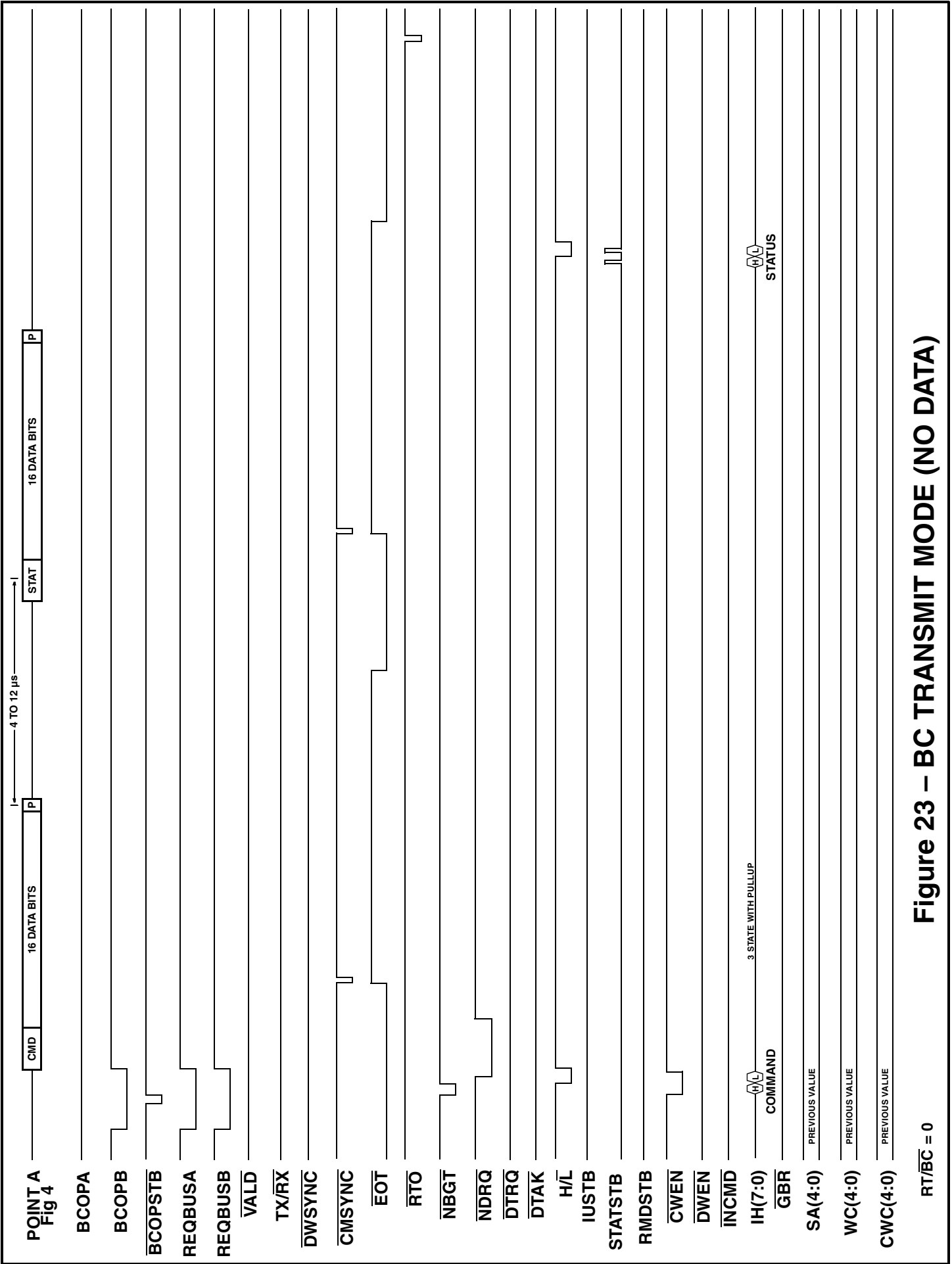


Figure 23 – BC TRANSMIT MODE (NO DATA)

RT/BC = 0

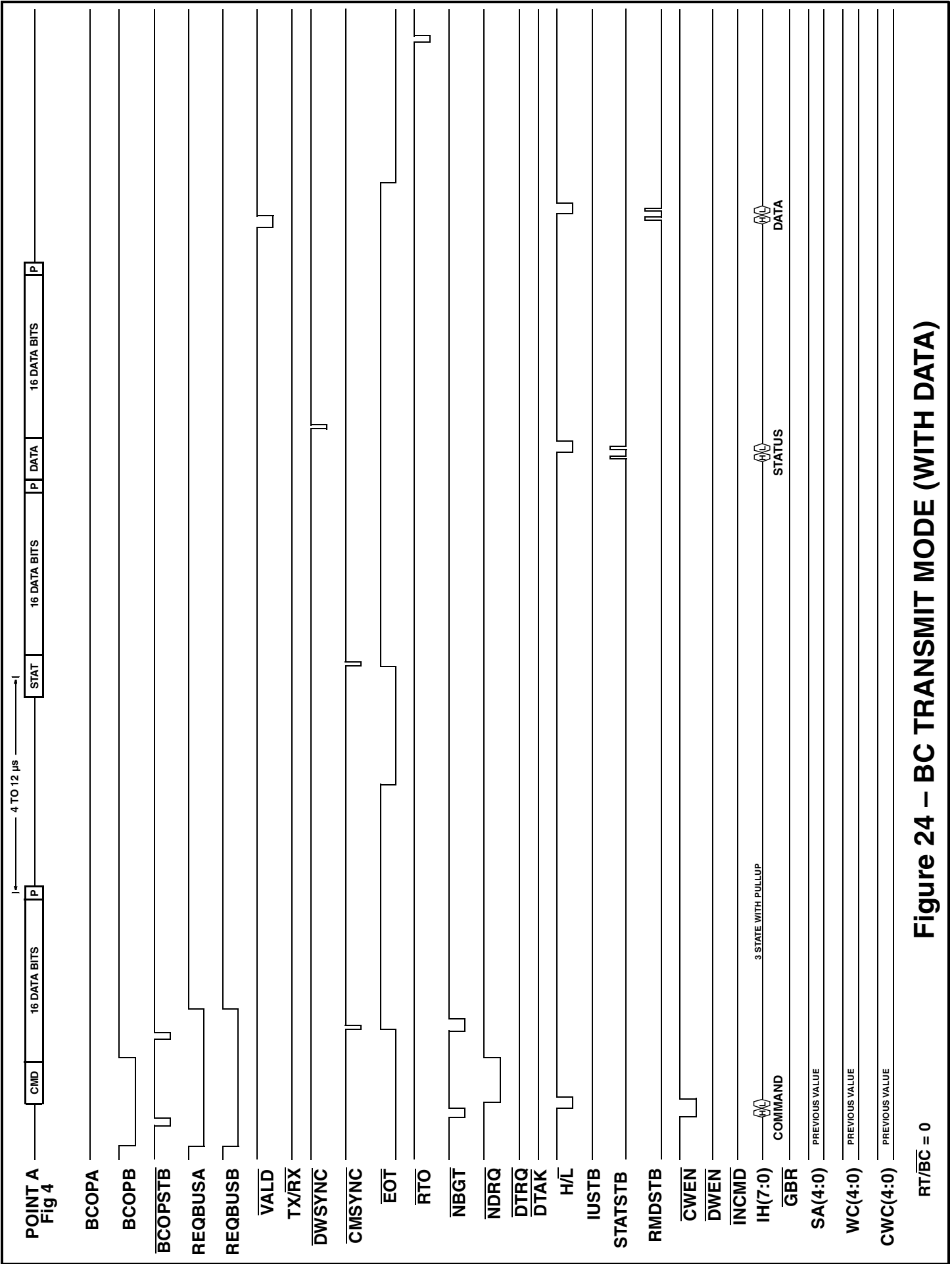


Figure 24 – BC TRANSMIT MODE (WITH DATA)

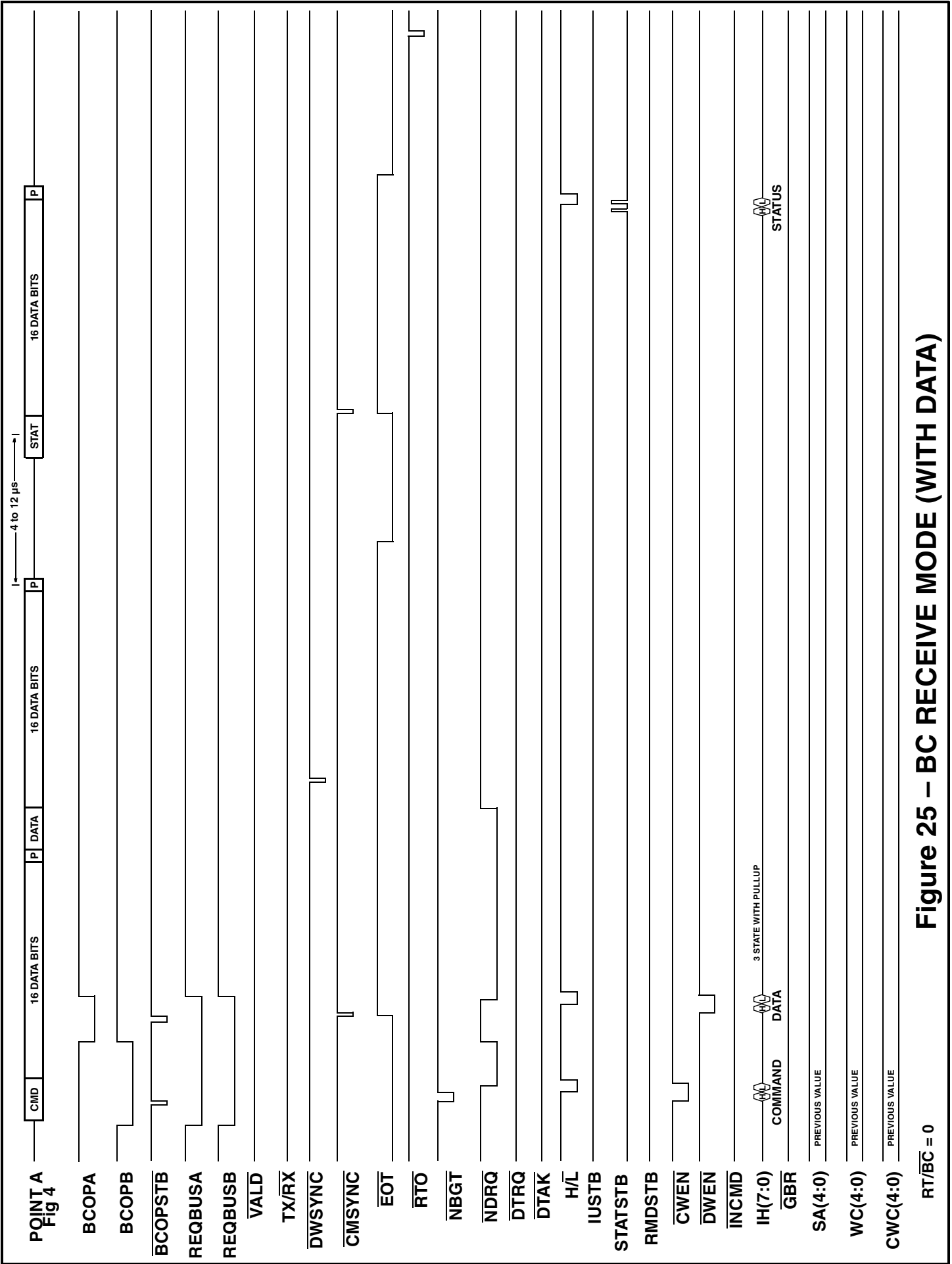


Figure 25 – BC RECEIVE MODE (WITH DATA)

RT/BC = 0

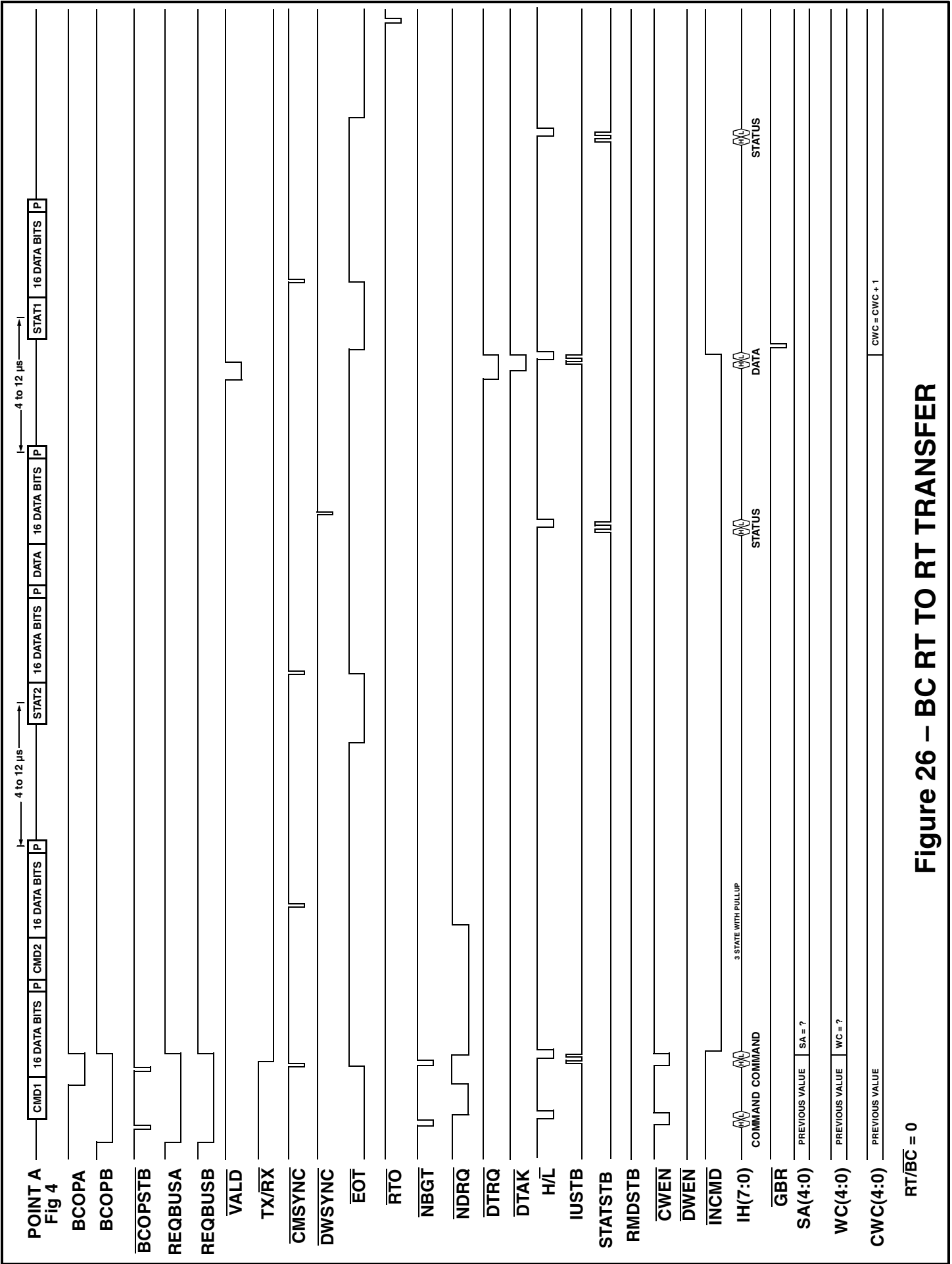
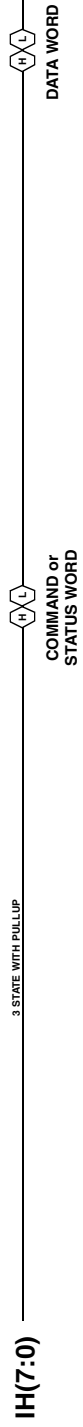
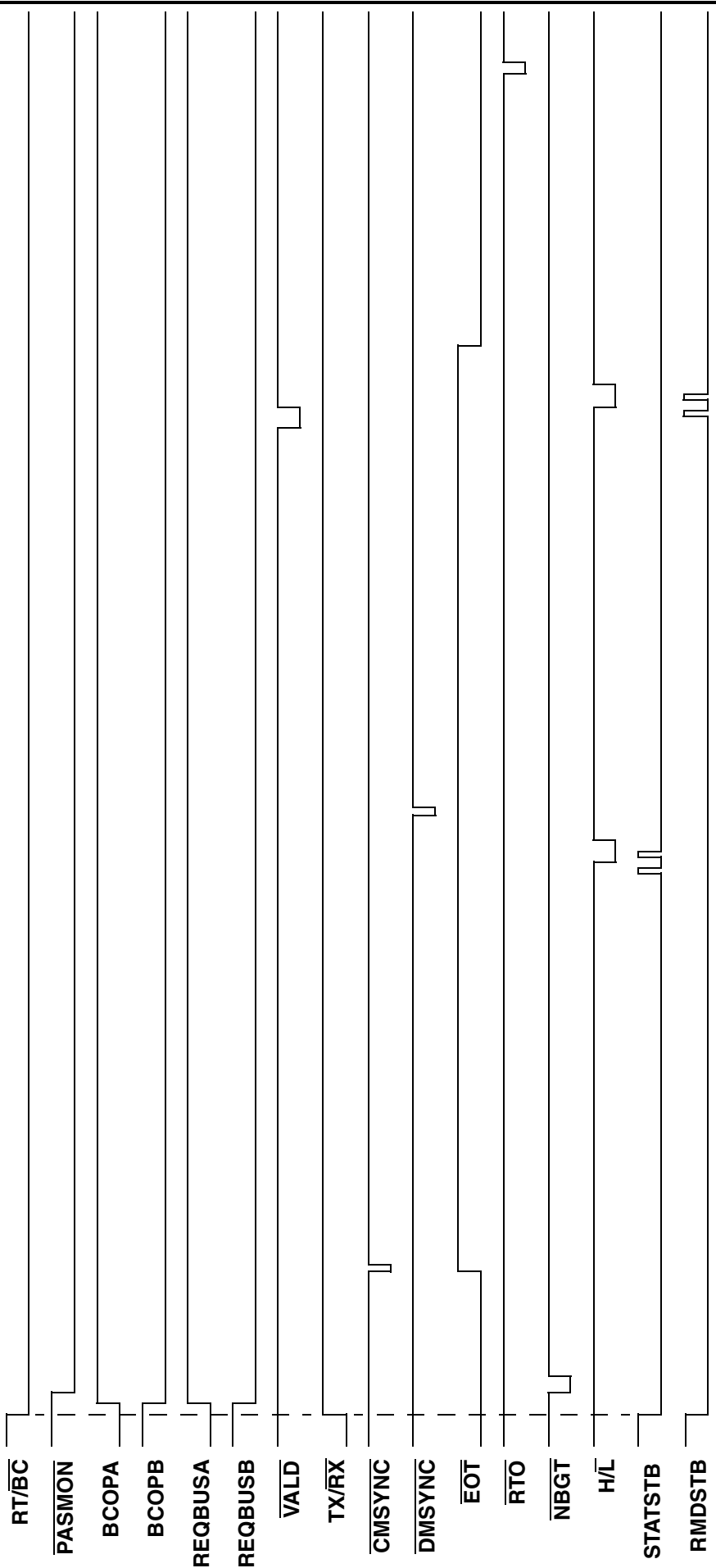


Figure 26 – BC RT TO RT TRANSFER



3 STATE WITH PULLUP

Figure 27 MONITOR MODE

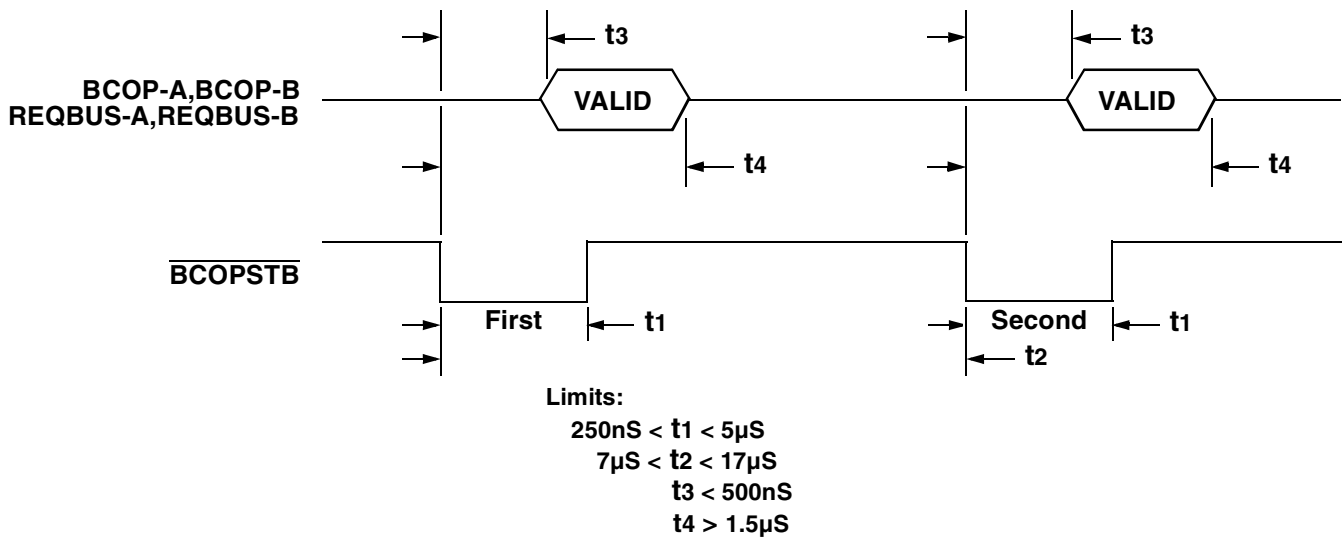
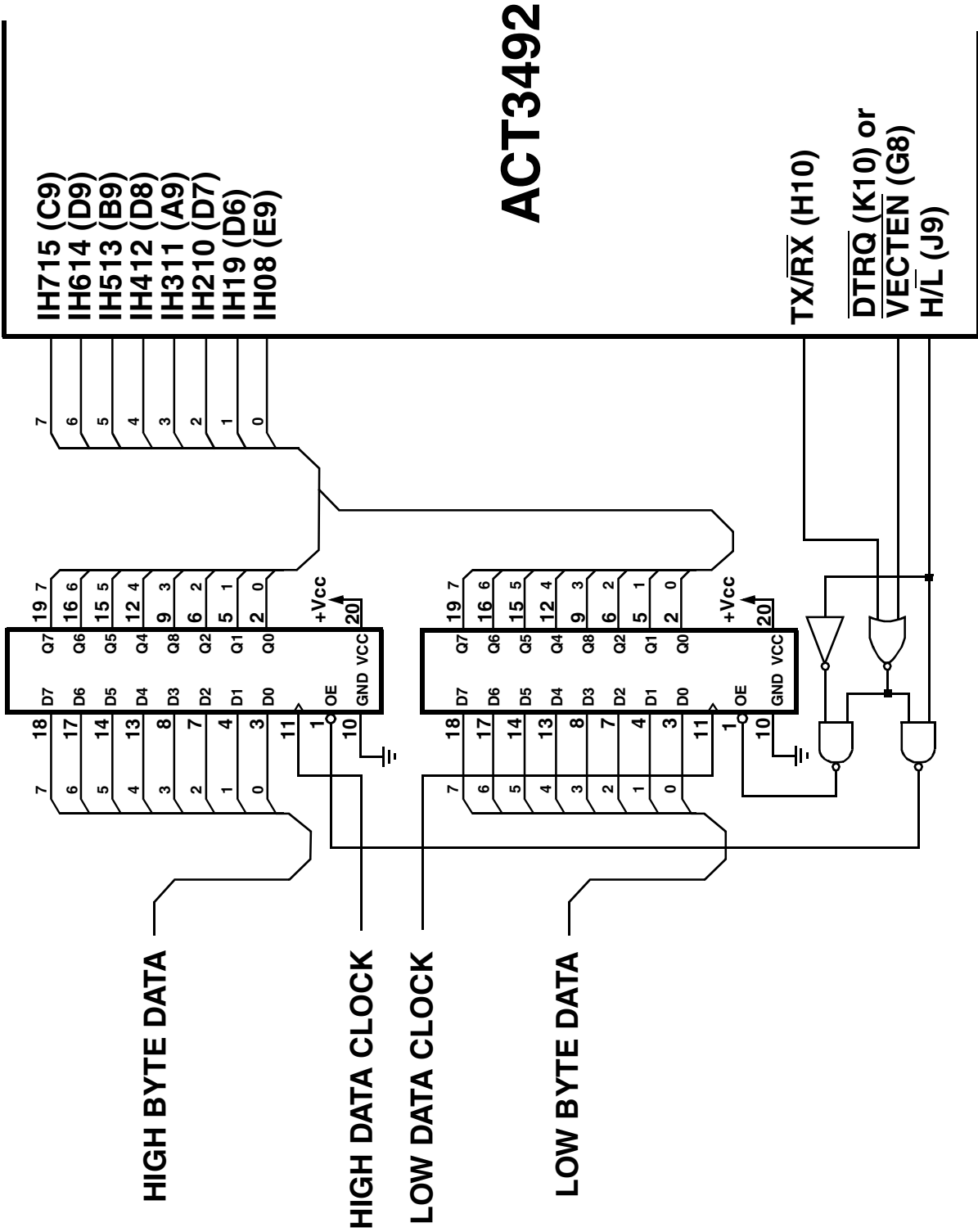


Figure 28 – BCOP Sequence Timing

TRANSFER TYPE	FIRST OR ONLY BCOPSTB		SECOND BCOPSTB	
	BCOP-B	BCOP-A	BCOP-B	BCOP-A
Normal Data (BC to RT / RT to BC)	0	0	N/A	N/A
RT to RT	0	1	0	0
Mode Codes (No Data) [T/R̄ = 0] 00h Dynamic Bus Control 01h Synchronize (No DATA) 02h Transmit Status 03h Initiate Self Test 04h Transmitter Shutdown 05h Override TX Shutdown 06h Inhibit TF Flag 07h Override Inhibit TF Flag 08h Reset Remote Terminal	0	1	N/A	N/A
Mode Codes (Data RT to BC) [T/R̄ = 1] 10h Transmit Vector Word 12h Transmit Last Command 13h Transmit Bit Word	0	1	1	1
Mode Codes (Data BC to RT) [T/R̄ = 0] 11h Synchronize (With DATA) 14h Selected TX Shutdown 15h Override Selected TX Shutdown	0	1	1	0

Table 1 – BCOP Sequences



DTAK may be connected to DTRQ, Ground or controlled

Figure 29 TYPICAL TRANSMIT DATA INTERFACE

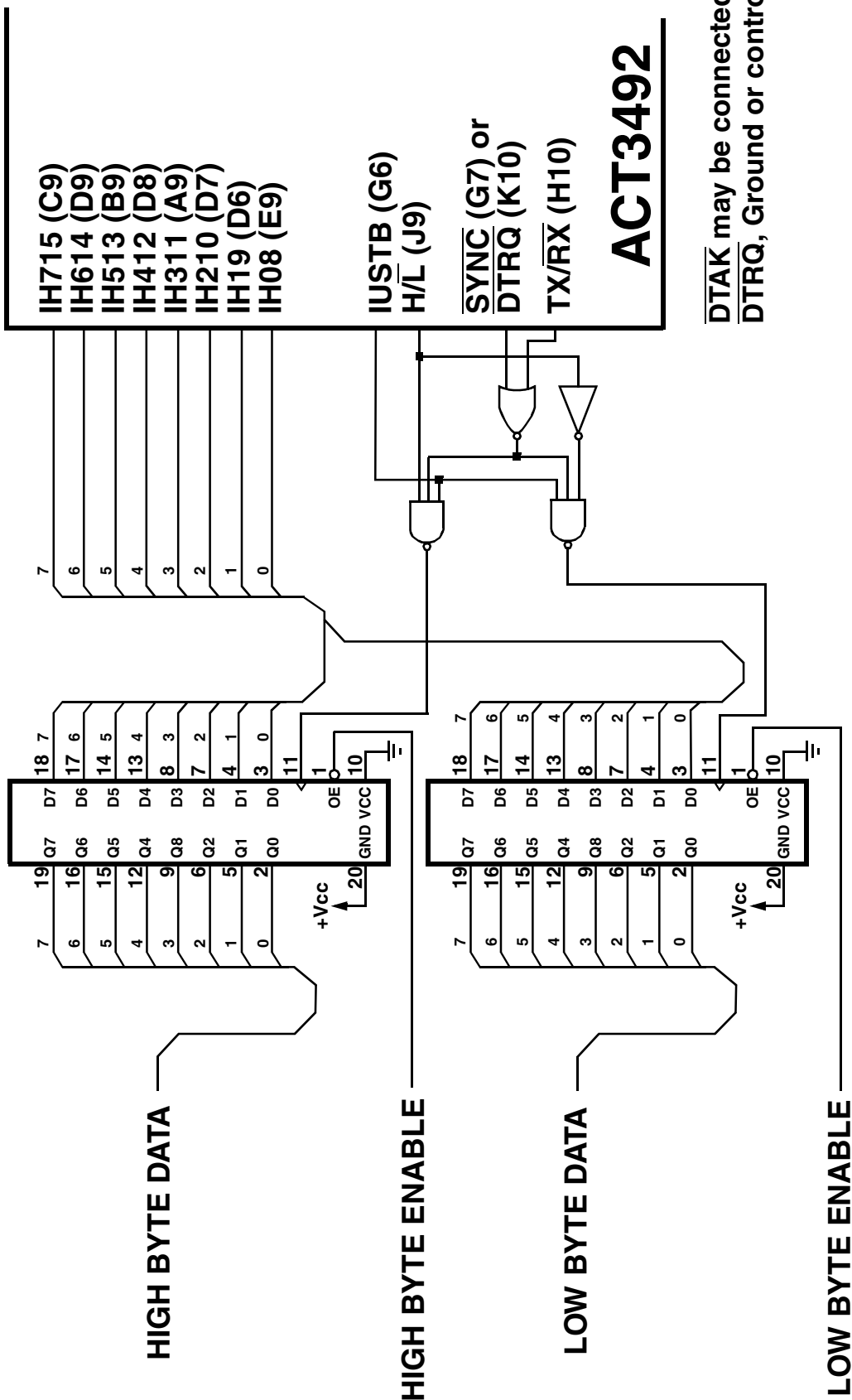


Figure 30 TYPICAL RECEIVE DATA INTERFACE

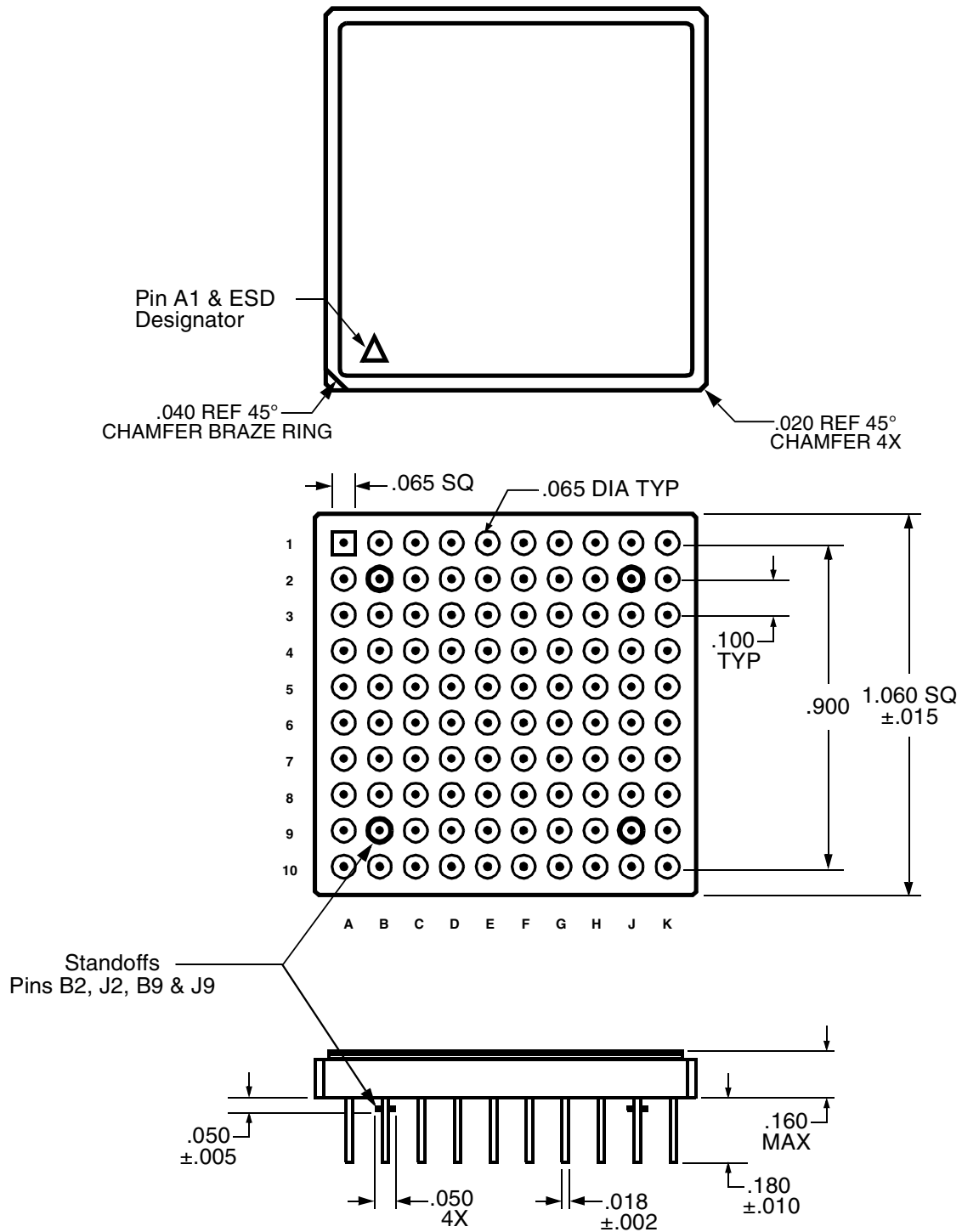
Package Pin Out Description By Pin - ACT3492

Pin #	Function	Pin #	Function	Pin #	Function
A1	\overline{RTADER}	D5	$\overline{LSTCMD/CWEN}$	G9	\overline{NBGT}
A2	+5VAB	D6	IH19	G10	INCLK
A3	$\overline{SERVREQ}$	D7	IH210	H1	GNDB
A4	WC4	D8	IH412	H2	SA4
A5	\overline{SSERR}	D9	IH614	H3	\overline{DRVINH}
A6	WC2	D10	\overline{NDRQ}	H4	CWC0
A7	\overline{LTEN}	E1	+5VAA	H5	RTAD3
A8	\overline{LTTRIG}	E2	\overline{LTFAIL}	H6	REQBUSB
A9	IH311	E3	\overline{MANER}	H7	SA2
A10	$\overline{NEXTSTAT}$	E4	6MCK	H8	CWC1
B1	TXRX A2	E5	REQBUSA	H9	\overline{EOT}
B2	TXRX A1	E6	$\overline{STATUPDATE}$	H10	TX/RX
B3	\overline{DBCACC}	E7	\overline{ENABLE}	J1	TXRX B1
B4	RT/ \overline{BC}	E8	MEREQ	J2	TXRX B2
B5	\overline{HSFAIL}	E9	IH08	J3	\overline{PASS}
B6	WC3	E10	+5V LOGIC	J4	$\overline{BITDECODE}$
B7	WC0	F1	+5VBB	J5	RTAD2
B8	MASTER RESET	F2	ERROR	J6	RTADPAR
B9	IH513	F3	\overline{RTO}	J7	\overline{GBR}
B10	BCOPA	F4	RTAD4	J8	CWC3
C1	GNDA	F5	BCSTEN 1	J9	H/L
C2	\overline{VALD}	F6	\overline{DTAK}	J10	SA0
C3	\overline{TXTO}	F7	$\overline{BCOPSTB}$	K1	CWC4
C4	\overline{RESET}	F8	\overline{PASMON}	K2	+5VBA
C5	\overline{DBCREQ}	F9	DIG GND 1 / CASE	K3	SA3
C6	$\overline{BITEN/RMDSTB}$	F10	DIG GND 2 / CASE	K4	CWC2
C7	\overline{BUSY}	G1	TXRX B1	K5	RTAD1
C8	WC1	G2	TXRX B2	K6	RTAD0
C9	IH715	G3	\overline{DWSYNC}	K7	$\overline{STATEN/STATSTB}$
C10	BCOPB	G4	\overline{CMSYNC}	K8	SA1
D1	TXRX A2	G5	BCSTEN 0	K9	\overline{INCMD}
D2	TXRX A1	G6	IUSTB	K10	\overline{DTRQ}
D3	\overline{PARER}	G7	\overline{SYNC}		
D4	\overline{TEST}	G8	$\overline{VECTEN/DWEN}$		

Package Pin Out Description By Function - ACT3492

Function	Pin #	Function	Pin #	Function	Pin #
+5VAA	E1	H \bar{L}	J9	RTAD4	F4
+5VAB	A2	H \bar{S} FAIL	B5	RTADER	A1
+5VBA	K2	IH08	E9	RTADPAR	J6
+5VBB	F1	IH19	D6	RTO	F3
+5V LOGIC	E10	IH210	D7	SA0	J10
6MCK	E4	IH311	A9	SA1	K8
BCOPA	B10	IH412	D8	SA2	H7
BCOPB	C10	IH513	B9	SA3	K3
BCOPSTB	F7	IH614	D9	SA4	H2
BCSTEN 0	G5	IH715	C9	SERVREQ	A3
BCSTEN 1	F5	INCLK	G10	SSERR	A5
BITDECODE	J4	INCMD	K9	STATEN/STATSTB	K7
BITEN/RMDSTB	C6	IUSTB	G6	STATUPDATE	E6
BUSY	C7	LSTCMD/CWEN	D5	SYNC	G7
CMSYNC	G4	LTEN	A7	TEST	D4
CWC0	H4	LTFAIL	E2	TX/RX	H10
CWC1	H8	L \bar{T} TRIG	A8	TXRX A1	B2
CWC2	K4	MANER	E3	TXRX A2	B1
CWC3	J8	MASTER RESET	B8	TXRX B1	G1
CWC4	K1	MEREQ	E8	TXRX B2	G2
DBCACC	B3	NBGT	G9	TXRX A1	D2
DBCREQ	C5	NDRQ	D10	TXRX A2	D1
DIG GND 1 / CASE	F9	NEXTSTAT	A10	TXRX B1	J1
DIG GND 2 / CASE	F10	PARER	D3	TXRX B2	J2
DRVINH	H3	PASMON	F8	TXTO	C3
DTAK	F6	PASS	J3	VALD	C2
DTRQ	K10	REQBUSA	E5	VECTEN/DWEN	G8
DWSYNC	G3	REQBUSB	H6	WC0	B7
ENABLE	E7	RESET	C4	WC1	C8
EOT	H9	RT/BC	B4	WC2	A6
ERROR	F2	RTAD0	K6	WC3	B6
GBR	J7	RTAD1	K5	WC4	A4
GNDA	C1	RTAD2	J5		
GNDB	H1	RTAD3	H5		

Ceramic CoFired PGA Package Outline





Ordering Information

Model Number	DESC Part Number	Package
ACT3492	Pending	1.06" x 1.06" Ceramic Plug In

Aeroflex Circuit Technology
35 South Service Road
Plainview New York 11803

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Specifications subject to change without notice.