

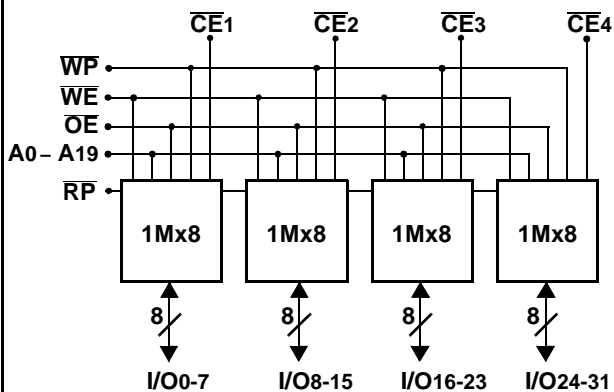
# ACT-F1M32 High Speed 32 Megabit Boot Block FLASH Multichip Module



## Features

- 4 Low Voltage/Power Intel 1M x 8 FLASH Die in One MCM Package
- Overall Configuration is 1M x 32
- +5V Operation (Standard) or +3.3V (Consult Factory)
- Access Times of 80, 100 and 120 nS ( 5V Vcc)
- +5V or +12V Programming
- Erase/Program Cycles
  - 100,000 Commercial
  - 10,000 Military and Industrial
- Sector Architecture (Each Die)
  - One 16K Protected Boot Block (*Bottom Boot Block Standard, Top Boot Block Special Order*)
  - Two 8K Parameter Blocks
  - One 96K Main Block
  - Seven 128K Main Blocks
- Single Block Erase (All bits set to 1)
- Hardware Data Protection Feature
- Independent Boot Block Locking
- MIL-PRF-38534 Compliant MCMs Available
- Packaging – Hermetic Ceramic
  - 68 Lead, .94" x .94" x .180" Dual-Cavity Small Outline Gull Wing, Aeroflex code# "F14" (*Drops into the 68 Lead JEDEC .99"SQ CQFJ footprint*)
- Internal Decoupling Capacitors for Low Noise Operation
- Commercial, Industrial and Military Temperature Ranges

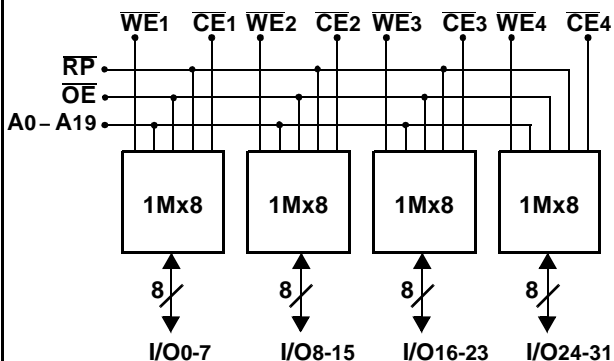
**Block Diagram – CQFP(F14)**  
*Standard Configuration*



Pin Description

I/O0-31	Data I/O
A0-19	Address Inputs
WE	Write Enables
CE1-4	Chip Enables
OE	Output Enable
WP	Write Protect
RP	Reset/Powerdown
VCC	Power Supply
GND	Ground
NC	Not Connected

**Block Diagram – CQFP(F14)**  
*Optional Configuration*



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## General Description

Utilizing Intel's SmartVoltage Boot Block Flash Memory SmartDie™, the ACT-F1M32 is a high speed, 32 megabit CMOS flash multichip module (MCM) designed for full temperature range military, space, or high reliability applications.

The ACT-F1M32 consists of four high-performance Intel X28F800BV 8 Mbit (8,388,608 bit) memory die. Each die contains separately erasable blocks, including a hardware lockable boot block (16,384 bytes), two parameter blocks (8,192 bytes each), and 8 main blocks (one block of 98,304 bytes and seven blocks of 131,072 bytes) This defines the boot block flash family architecture.

The command register is written by bringing WE to a logic low level (V<sub>IL</sub>), while CE is low and OE is high (V<sub>IH</sub>). Reading is

## General Description, Cont'd

accomplished by chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) being logically active. Access time grades of 80nS, 100nS and 120nS maximum are standard.

The ACT-F1M32 is packaged in a hermetically sealed co-fired ceramic 68 lead, .94" SQ Ceramic Gull Wing CQFP package. This allows operation in a military environment temperature range of -55°C to +125°C.

The ACT-F1M32 provides program and erase capability at 5V or 12V and allows reads with Vcc at 5V or 3.3V(Not tested). Since many designs read from flash memory a large percentage of the time, read operation using 3.3V can provide great power savings. Consult the factory for 3.3V tested parts. In applications where read performance is critical, faster access times are obtainable with the 5V Vcc part detailed herein.

For program and erase operations, 5V Vpp operation eliminates the need for in system voltage converters. The 12V Vpp operation provides reduced (approx 60%) program and erase times where 12V is available in the system. For design simplicity, however, connect Vcc and Vpp to the same 5V  $\pm 10\%$  source.

Each block can be independently

erased and programmed 100,000 times at commercial temperature or 10,000 times at extended temperature.

The boot block is located at either the bottom (Standard) or the top (Special Order) of the address map in order to accommodate different microprocessor protocols for boot code location. Locking and unlocking of the boot block is controlled by  $\overline{WP}$  and/or  $\overline{RP}$ .

Intel's boot block architecture provides a flexible solution for the different design needs of various applications. The asymmetrically-blocked memory map allows the integration of several memory components into a single flash device. The boot block provides a secure boot PROM; the parameter blocks can emulate EEPROM functionality for parameter store with proper software techniques; and the main blocks provide code and data storage with access times fast enough to execute code in place, decreasing RAM requirements.

For Detail Information regarding the operation of the 28F800BV Memory die, see the Intel datasheet (order number 290539-002).

## Absolute Maximum Ratings

Parameter	Range	Units
Case Operating Temperature Range	-55 to +125	°C
Storage Temperature Range	-65 to +150	°C
Voltage on Any Pin with Respect to GND (except V <sub>CC</sub> , V <sub>PP</sub> , A <sub>9</sub> and $\overline{RP}$ ) <sup>(1)</sup>	-2.0 to +7.0	V
Voltage on Pins A <sub>9</sub> or $\overline{RP}$ with Respect to GND (except V <sub>CC</sub> , V <sub>PP</sub> , A <sub>9</sub> and $\overline{RP}$ ) <sup>(1,2)</sup>	-2.0 to +13.5	V
V <sub>PP</sub> Program Voltage with Respect to GND during Block Erase/ and Word/Byte Write <sup>(1,2)</sup>	-2.0 to +14.0	V
V <sub>CC</sub> Supply Voltage with Respect to Ground <sup>(1)</sup>	-2.0 to +7.0	V
Output Short Circuit Current <sup>(3)</sup>	100	mA

Notes:

1. Minimum DC voltage is -0.5V on input/output pins. During Transitions, inputs may undershoot to -2.0V for periods < 20nS. Maximum DC voltage on input/output pins is V<sub>CC</sub> + 0.5V, which may overshoot to V<sub>CC</sub> + 2.0V for periods < 20nS.

2. Maximum DC voltage on V<sub>PP</sub> may overshoot to +14.0V for periods < 20nS. Maximum DC voltage on  $\overline{RP}$  or A<sub>9</sub> may overshoot to V<sub>CC</sub> + 0.5V for periods < 20nS

3. Output shorted for no more than 1 second. No more than one output shorted at one time.

NOTICE: Stresses above those listed under "Absolute Maximums Rating" may cause permanent damage. These are stress rating only. Operation beyond the "Operation Conditions" is not recommended and extended exposure beyond the "Operation Conditions" may effect device reliability.

## Recommended Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V <sub>CC</sub>	5V Power Supply Voltage (10%)	+4.5	+5.5	V
	3.3V Power Supply Voltage (±0.3V) (Consult Factory)	+3.0	+3.6	V
V <sub>IH</sub>	Input High Voltage (3.3V & 5V V <sub>CC</sub> )	+2.0	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input Low Voltage (3.3V & 5V V <sub>CC</sub> )	-0.5	+0.8	V
T <sub>A</sub>	Operating Temperature (Military)	-55	+125	°C

## Capacitance

(f = 1MHz, T<sub>A</sub> = 25°C)

Symbol	Parameter	Maximum	Units
CAD	A0 – A19 Capacitance	50	pF
COE	$\overline{OE}$ Capacitance	50	pF
CCE	$\overline{CE}$ Capacitance	20	pF
CRP	$\overline{RP}$ Capacitance	50	pF
CWE	$\overline{WE}$ Capacitance	60	pF
CWP	$\overline{WP}$ Capacitance	50	pF
CI/O	I/O0 – I/O31 Capacitance	20	pF

Capacitance Guaranteed by design, but not tested.

## DC Characteristics – CMOS Compatible

(T<sub>A</sub> = -55°C to +125°C, V<sub>CC</sub> = +4.5V to + 5.5V(5V Operation), or +3.0V to +3.6V(3.3V Operation), Unless otherwise specified)

Parameter	Sym	Conditions	+3.3V V <sub>CC</sub> <sup>(1)</sup>		+5.0V V <sub>CC</sub>		Units
			Typical		Standard		
			Min	Max	Min	Max	
Input Load Current	I <sub>IL</sub>	V <sub>CC</sub> = V <sub>CC</sub> Max., V <sub>IN</sub> = V <sub>CC</sub> or GND	-1	+1	-1	+1	μA
Output Leakage Current	I <sub>LO</sub>	V <sub>CC</sub> = V <sub>CC</sub> Max., V <sub>IN</sub> = V <sub>CC</sub> or GND	-10	+10	-10	+10	μA
V <sub>CC</sub> Standby Current	I <sub>CCS</sub>	V <sub>CC</sub> = V <sub>CC</sub> Max., $\overline{CE}$ = $\overline{RP}$ = $\overline{WP}$ = V <sub>CC</sub> ± 0.2V		440		600	μA
V <sub>CC</sub> Deep Power-Down Current	I <sub>CCD</sub>	V <sub>CC</sub> = V <sub>CC</sub> Max., V <sub>IN</sub> = V <sub>CC</sub> or GND, $\overline{RP}$ = GND ± 0.2V		32		32	μA
V <sub>CC</sub> Read Current	I <sub>CCR</sub>	V <sub>CC</sub> = V <sub>CC</sub> Max., $\overline{CE}$ = GND, f = 10MHz (5V), 5MHz (3.3V), I <sub>OUT</sub> = 0 mA, Inputs = GND ± 0.2V or V <sub>CC</sub> ± 0.2V		120		260	mA
V <sub>CC</sub> Write Current	I <sub>CCW1</sub>	V <sub>PP</sub> = V <sub>PPH1</sub> (at 5V), Word Write in Progress (x32)		120		200	mA
	I <sub>CCW2</sub>	V <sub>PP</sub> = V <sub>PPH2</sub> (at 12V), Word Write in Progress (x32)		100		180	mA
V <sub>CC</sub> Erase Current	I <sub>CC1</sub>	V <sub>PP</sub> = V <sub>PPH1</sub> (at 5V), Block Erase in Progress		120		180	mA
	I <sub>CC2</sub>	V <sub>PP</sub> = V <sub>PPH2</sub> (at 12V), Block Erase in Progress		100		160	mA
V <sub>CC</sub> Erase Suspend Current	I <sub>CCES</sub>	$\overline{CE}$ = V <sub>IH</sub> , Block Erase Suspend		32		48	mA
V <sub>PP</sub> Standby Current	I <sub>PPS</sub>	V <sub>PP</sub> < V <sub>PPH2</sub>		60		60	μA

## DC Characteristics – CMOS Compatible

(TA = -55°C to +125°C, VCC = +4.5V to + 5.5V(5V Operation), or +3.0V to +3.6V(3.3V Operation), Unless otherwise specified)

Parameter	Sym	Conditions	+3.3V Vcc <sup>(1)</sup>		+5.0V Vcc		Units
			Min	Max	Min	Max	
V <sub>PP</sub> Deep Power Down Current	IPPD	$\overline{RP} = GND \pm 0.2V$		40		40	μA
V <sub>PP</sub> Read Current	IPPR	$V_{PP} \geq V_{PPH2}$		800		800	μA
V <sub>PP</sub> Write Current	IPPW1	$V_{PP} = V_{PPH1}$ (at 5V), Word Write in Progress (x32)		120		120	mA
	IPPW2	$V_{PP} = V_{PPH2}$ (at 12V), Word Write in Progress (x32)		100		100	mA
V <sub>PP</sub> Erase Current	IPPE1	$V_{PP} = V_{PPH1}$ (at 5V), Block Erase in Progress		120		100	mA
	IPPE2	$V_{PP} = V_{PPH2}$ (at 12V), Block Erase in Progress		100		80	mA
V <sub>PP</sub> Erase Suspend Current	IPPEs	$V_{PP} = V_{PPH}$ , Block Erase Suspend in Progress		800		800	μA
R <sub>P</sub> Boot Block Unlock Current	IRP	$\overline{RP} = V_{HH}$ , $V_{PP} = 12V$		2		2	mA
Output Low Voltage	VOL	$V_{CC} = V_{CCMin.}$ , IOL = 5.8 mA (5V), 2 mA (3.3V)		0.45		0.45	V
Output High Voltage	VOH1	$V_{CC} = V_{CCMin.}$ , IOH = -2.5 mA	0.85 x V <sub>CC</sub>		0.85 x V <sub>CC</sub>		V
	VOH2	$V_{CC} = V_{CCMin.}$ , IOH = -100 μA	V <sub>CC</sub> - 0.4V		V <sub>CC</sub> - 0.4V		V
V <sub>PP</sub> Lock-Out Voltage	VPPLK	Complete Write Protection	0.0	1.5	0.0	1.5	V
V <sub>PP</sub> (Program/Erase Operations)	VPPH1	$V_{PP} = \text{at } 5V$	4.5	5.5	4.5	5.5	V
V <sub>PP</sub> (Program/Erase Operations)	VPPH2	$V_{PP} = \text{at } 12V$	11.4	12.6	11.4	12.6	V
V <sub>CC</sub> Erase/Write Lock Voltage	VLKO	Locked Condition	0	2.0	0	2.0	V
R <sub>P</sub> Unlock Voltage	VHH	Boot Block Write/Erase, $V_{PP} = 12V$	11.4	12.6	11.4	12.6	V

Notes:

1. Performance at V<sub>CC</sub> = +4.5V to +5.5V is guaranteed. Performance at V<sub>CC</sub> = +3.3V is typical (Not tested).

## AC Characteristics – Write/Erase/Program Operations – WE Controlled

(TA = -55°C to +125°C, VCC = +4.5V to + 5.5V(5V Operation), or +3.0V to +3.6V(3.3V Operation), Unless otherwise specified)

Parameter	Symbol JEDEC Standard	+3.3V Vcc <sup>(2)</sup>		+4.5V to +5.5V Vcc				Units		
		Typical		80nS		100nS			120nS	
		120nS	Min Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>AVAV</sub>	120		80		100		120		nS
R <sub>P</sub> High Recovery to $\overline{WE}$ Going Low	t <sub>PHWL</sub>	1.5		.45		.45		.45		μS
$\overline{CE}$ Setup to $\overline{WE}$ Going Low	t <sub>ELWL</sub>	0		0		0		0		nS
Boot Block Unlock Setup to $\overline{WE}$ Going High <sup>(1)</sup>	t <sub>PHHWH</sub>	200		100		100		100		nS
V <sub>PP</sub> Setup to $\overline{WE}$ Going High <sup>(1)</sup>	t <sub>VPWH</sub>	200		100		100		100		nS
Address Setup to $\overline{WE}$ Going High	t <sub>AVWH</sub>	90		60		60		60		nS
Data Setup to $\overline{WE}$ Going High	t <sub>DVWH</sub>	70		60		60		60		nS
$\overline{WE}$ Pulse Width	t <sub>WLWH</sub>	90		60		60		60		nS
Data Hold Time from $\overline{WE}$ High	t <sub>WHDx</sub>	0		0		0		0		nS
Address Hold Time from $\overline{WE}$ High	t <sub>WHAX</sub>	0		0		0		0		nS
$\overline{CE}$ Hold Time from $\overline{WE}$ High	t <sub>WHEH</sub>	0		0		0		0		nS
$\overline{WE}$ Pulse Width High	t <sub>WHWL</sub>	30		20		20		20		nS
Duration of Word Write Operation <sup>(1)</sup> (x32)	t <sub>WHQV1</sub>	6		6		6		6		μS
Duration of Erase Operation (Boot) <sup>(1)</sup>	t <sub>WHQV2</sub>	0.3		0.3		0.3		0.3		Sec
Duration of Erase Operation (Parameter) <sup>(1)</sup>	t <sub>WHQV3</sub>	0.3		0.3		0.3		0.3		Sec
Duration of Erase Operation (Main) <sup>(1)</sup>	t <sub>WHQV4</sub>	0.6		0.6		0.6		0.6		Sec
V <sub>PP</sub> Hold from Valid SRD <sup>(1)</sup>	t <sub>QVVL</sub>	0		0		0		0		nS
R <sub>P</sub> V <sub>HH</sub> Hold from Valid SRD <sup>(1)</sup>	t <sub>QVPH</sub>	0		0		0		0		nS
Boot Block Lock Delay <sup>(1)</sup>	t <sub>PHBR</sub>		200		100		100		100	nS

Notes:

1. Guaranteed by design, not tested.

2. Performance at V<sub>CC</sub> = +4.5V to +5.5V is guaranteed. Performance at V<sub>CC</sub> = +3.3V is typical (Not tested).

## AC Characteristics – Write/Erase/Program Operations, $\overline{CE}$ Controlled

(TA = -55°C to +125°C, Vcc = +4.5V to +5.5V(5V Operation), or +3.0V to +3.6V(3.3V Operation), Unless otherwise specified)

Parameter	Symbol JEDEC Standard	+3.3V Vcc <sup>(2)</sup> Typical		+4.5V to +5.5V Vcc				Units		
		120nS		80nS		100nS			120nS	
		Min	Max	Min	Max	Min	Max		Min	Max
Write Cycle Time	tAVAV	120		80		100		120		nS
$\overline{RP}$ High Recovery to $\overline{CE}$ Low	tPHL	1.5		.45		.45		.45		μS
$\overline{WE}$ Setup to $\overline{CE}$ Going Low	tWLEL	0		0		0		0		nS
Boot Block Unlock Setup to $\overline{CE}$ Going High <sup>(1)</sup>	tPHHEH	200		100		100		100		nS
VPP Setup to $\overline{CE}$ Going High <sup>(1)</sup>	tVPEH	200		100		100		100		nS
Address Setup to $\overline{CE}$ Going High	tAVEH	90		60		60		60		nS
Data Setup to $\overline{CE}$ Going High	tDVEH	70		60		60		60		nS
$\overline{CE}$ Pulse Width	tLEH	90		60		60		60		nS
Data Hold Time from $\overline{CE}$ High	tEHDX	0		0		0		0		nS
Address Hold Time from $\overline{CE}$ High	tEHAX	0		0		0		0		nS
$\overline{WE}$ Hold Time from $\overline{CE}$ High	tEWH	0		0		0		0		nS
$\overline{CE}$ Pulse Width High	tHEL	20		20		20		20		nS
Duration of Word Write Operation <sup>(1)</sup> (x32)	tEHQV1	6		6		6		6		μS
Duration of Erase Operation (Boot) <sup>(1)</sup>	tEHQV2	0.3		0.3		0.3		0.3		Sec
Duration of Erase Operation (Parameter) <sup>(1)</sup>	tEHQV3	0.3		0.3		0.3		0.3		Sec
Duration of Erase Operation (Main) <sup>(1)</sup>	tEHQV4	0.6		0.6		0.6		0.6		Sec
VPP Hold from Valid SRD <sup>(1)</sup>	tQVVL	0		0		0		0		nS
$\overline{RP}$ VHH Hold from Valid SRD <sup>(1)</sup>	tQVPH	0		0		0		0		nS
Boot Block Lock Delay <sup>(1)</sup>	tPHBR		200		100		100		100	nS

NOTES:

1. Sampled, but not 100% tested.

2. Performance at Vcc = +4.5V to +5.5V is guaranteed. Performance at Vcc = +3.3V is typical (Not Tested).

## AC Characteristics – Read Only Operations

(TA = -55°C to +125°C, Vcc = +4.5V to +5.5V(5V Operation), or +3.0V to +3.6V(3.3V Operation), Unless otherwise specified)

Parameter	Symbol JEDEC Standard	+3.3V Vcc <sup>(2)</sup> Typical		+4.5V to +5.5V Vcc				Units		
		120nS		80nS		100nS			120nS	
		Min	Max	Min	Max	Min	Max		Min	Max
Read Cycle Time	tAVAV	120		80		100		120		nS
Address to Output Delay	tAVQV		120		80		100		120	nS
$\overline{CE}$ to Output Delay	tELQV		120		80		100		120	nS
$\overline{RP}$ to Output Delay	tPHQV		1.5		.45		.45		.45	μS
$\overline{OE}$ to Output Delay	tGLQV		65		40		40		40	nS
$\overline{CE}$ to Output in Low Z <sup>(1)</sup>	tELQX	0		0		0		0		nS
$\overline{CE}$ to Output in High Z <sup>(1)</sup>	tEHQZ		55		30		30		30	nS
$\overline{OE}$ to Output in Low Z <sup>(1)</sup>	tGLQX	0		0		0		0		nS
$\overline{OE}$ to Output in High Z <sup>(1)</sup>	tGHQZ		45		30		30		30	nS
Output Hold from Address, $\overline{CE}$ , or $\overline{OE}$ Change, Whichever Occurs First <sup>(1)</sup>	tOH	0		0		0		0		nS

Notes:

1. Guaranteed by design, but not tested.

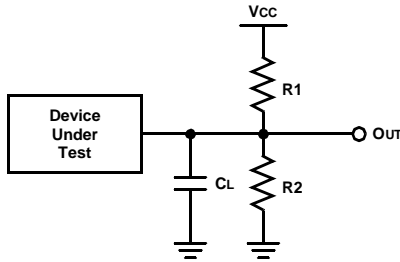
2. Performance at Vcc = +4.5V to +5.5V is guaranteed. Performance at Vcc = +3.3V is typical (Not Tested).

## AC Test Circuit

Test Configuration Component Values

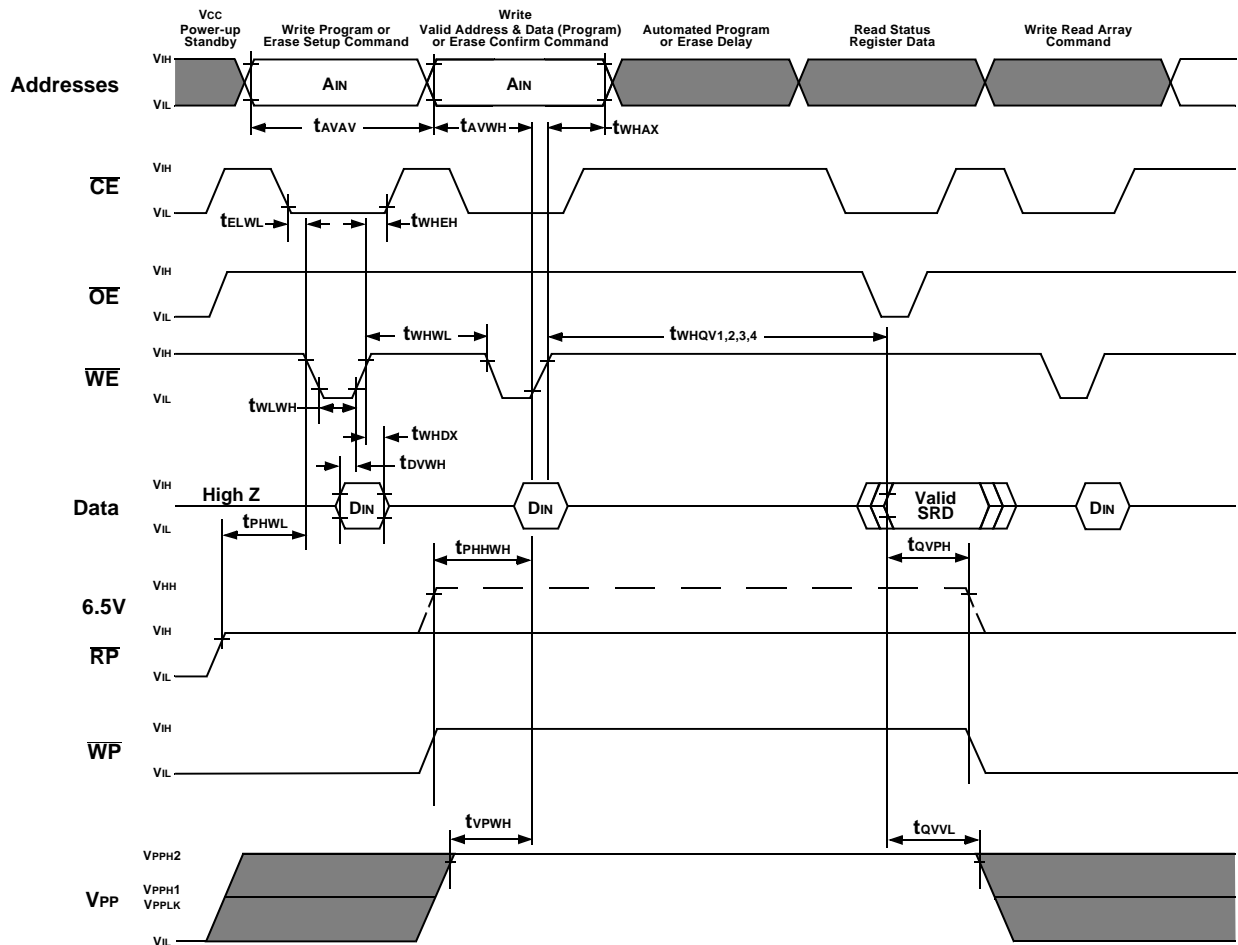
Test Configuration	CL (pF)	R1 ( $\Omega$ )	R2 ( $\Omega$ )
3.3V Standard Test	50	990	770
5V Standard Test	50	580	390

NOTES:  
CL includes jig capacitance.

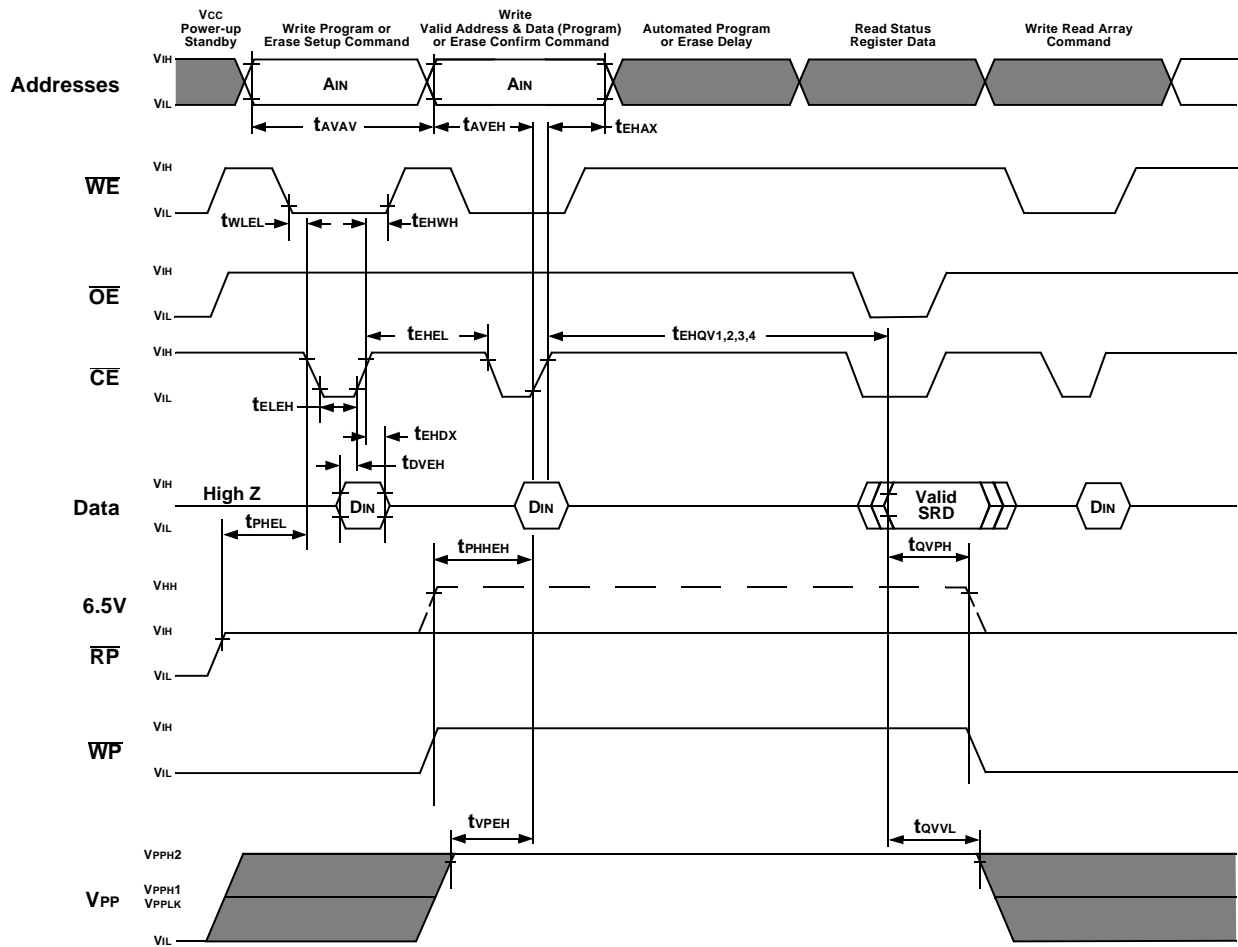


Parameter	Typical	Units
Input Pulse Level	0 – 3.0	V
Input Rise and Fall	5	nS
Input and Output Timing Reference Level	1.5	V

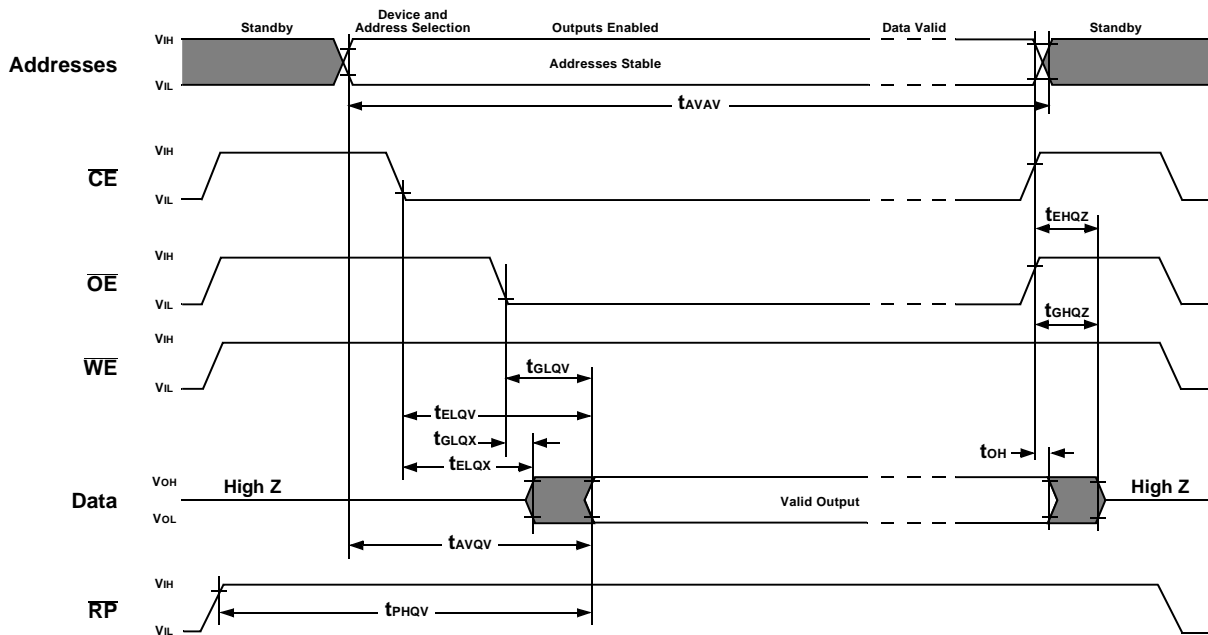
## AC Waveforms for Write and Erase Operations, $\overline{WE}$ Controlled



## AC Waveforms for Write and Erase Operations, $\overline{CE}$ Controlled



## AC Waveform For Read Operations

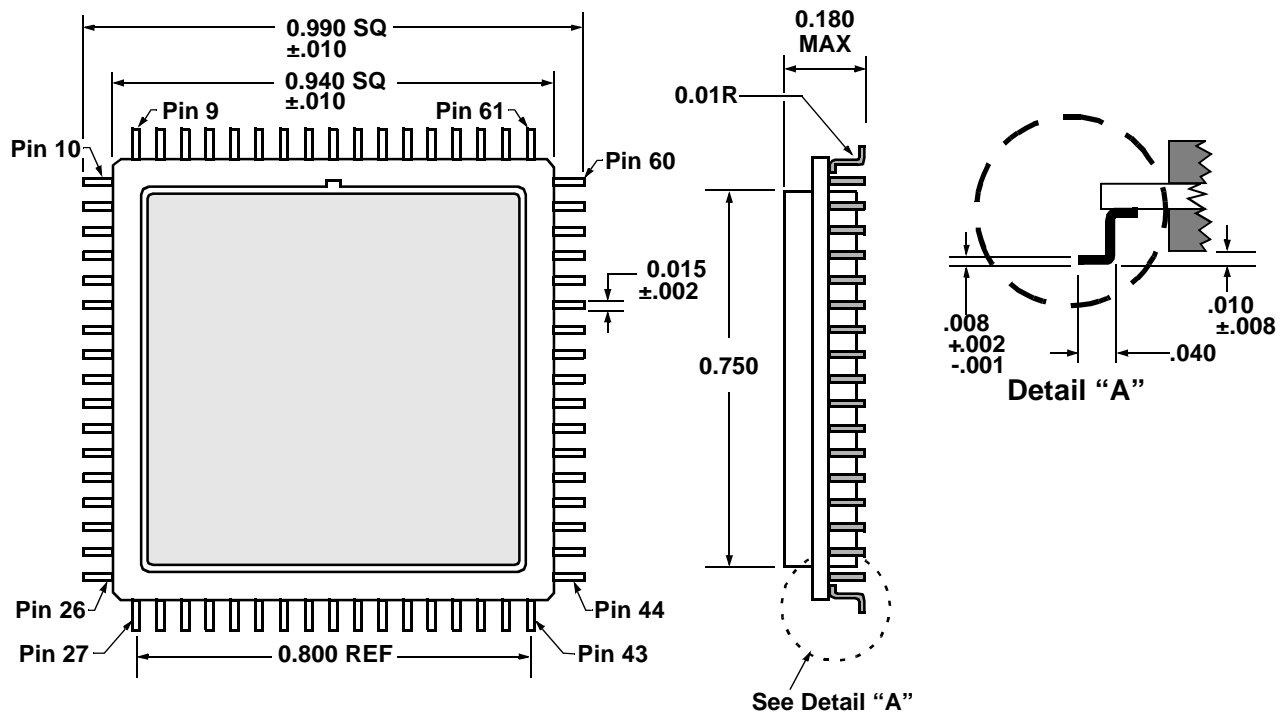


## Pin Numbers & Functions

<b>68 Pins — Dual-Cavity CQFP (Standard Configuration)</b>							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CE3}$	19	I/O8	36	$\overline{CE2}$	53	I/O23
3	A5	20	I/O9	37	A17	54	I/O22
4	A4	21	I/O10	38	$\overline{WP}$	55	I/O21
5	A3	22	I/O11	39	NC	56	I/O20
6	A2	23	I/O12	40	NC	57	I/O19
7	A1	24	I/O13	41	A18	58	I/O18
8	A0	25	I/O14	42	A19	59	I/O17
9	$\overline{RP}$	26	I/O15	43	V <sub>PP</sub>	60	I/O16
10	I/O0	27	V <sub>CC</sub>	44	I/O31	61	V <sub>CC</sub>
11	I/O1	28	A11	45	I/O30	62	A10
12	I/O2	29	A12	46	I/O29	63	A9
13	I/O3	30	A13	47	I/O28	64	A8
14	I/O4	31	A14	48	I/O27	65	A7
15	I/O5	32	A15	49	I/O26	66	A6
16	I/O6	33	A16	50	I/O25	67	$\overline{WE}$
17	I/O7	34	$\overline{CE1}$	51	I/O24	68	$\overline{CE4}$

Consult Factory for Special order (*Optional Configuration*): Pin 38 -  $\overline{WE2}$ , Pin 39 -  $\overline{WE3}$ , Pin 40 -  $\overline{WE4}$  and Pin 67 -  $\overline{WE1}$

### "F14" — CQFP Dual-Cavity Flat Package



All dimensions in inches

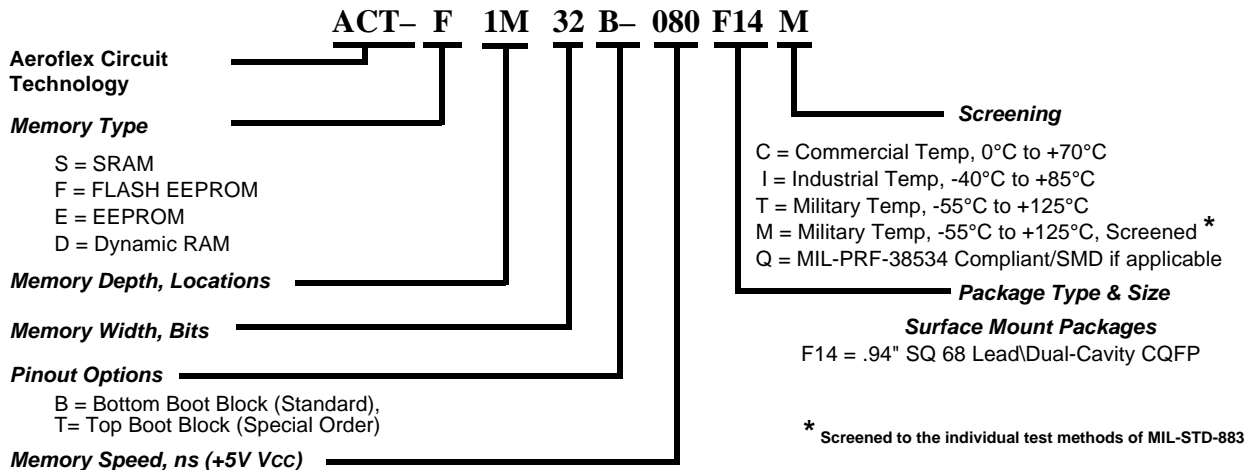




## Ordering Information

Model Number	Screening	Speed	Package
ACT-F1M32B-080F14C	Commercial (0°C to +70°C)	80 nS	CQFP
ACT-F1M32B-100F14C	Commercial (0°C to +70°C)	100 nS	CQFP
ACT-F1M32B-120F14C	Commercial (0°C to +70°C)	120 nS	CQFP
ACT-F1M32B-080F14I	Industrial (-40°C to +85°C)	80 nS	CQFP
ACT-F1M32B-100F14I	Industrial (-40°C to +85°C)	100 nS	CQFP
ACT-F1M32B-120F14I	Industrial (-40°C to +85°C)	120 nS	CQFP
ACT-F1M32B-080F14M	Military (-55°C to +125°C)	80 nS	CQFP
ACT-F1M32B-100F14M	Military (-55°C to +125°C)	100 nS	CQFP
ACT-F1M32B-120F14M	Military (-55°C to +125°C)	120 nS	CQFP
ACT-F1M32B-080F14Q	DESC Drawing Pending MIL-PRF-38534 Compliant	80 nS	CQFP
ACT-F1M32B-100F14Q	DESC Drawing Pending MIL-PRF-38534 Compliant	100 nS	CQFP
ACT-F1M32B-120F14Q	DESC Drawing Pending MIL-PRF-38534 Compliant	120 nS	CQFP

## Part Number Breakdown



Specifications subject to change without notice

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