

Mixed-Signal Products
AX07CF064 Product Summary
ARM7® Microcontroller with Embedded Flash
Preliminary Data Sheet

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www.aeroflex.com/ARM7



FEATURES

- ARM7TDMI Core
- 64K Flash
- 4K SRAM
- Can address up to 384KB 8-bit external memory (64KB x 6)
- 10-bit, 5-channel ADC
- Power Management Unit (PMU)
- 2-channel UART
- 8-bit Watchdog Timer
- 16-bit, 6-channel Timers/PWM
- Up to 55 I/O Ports
- 6 External Interrupt pins
- 11 Internal Interrupts
- 50MHz Maximum Operating Frequency
- 3.3V Operation*
- 80-pin TQFP package
- 0.35u CMOS
- 430mW power (@50MHz)
- 40° to 85°C Operating Temperature

*An additional 5V supply is required for programming the flash memory. If in-circuit programming is not required this supply is not required. Factory programming is available.

General Description

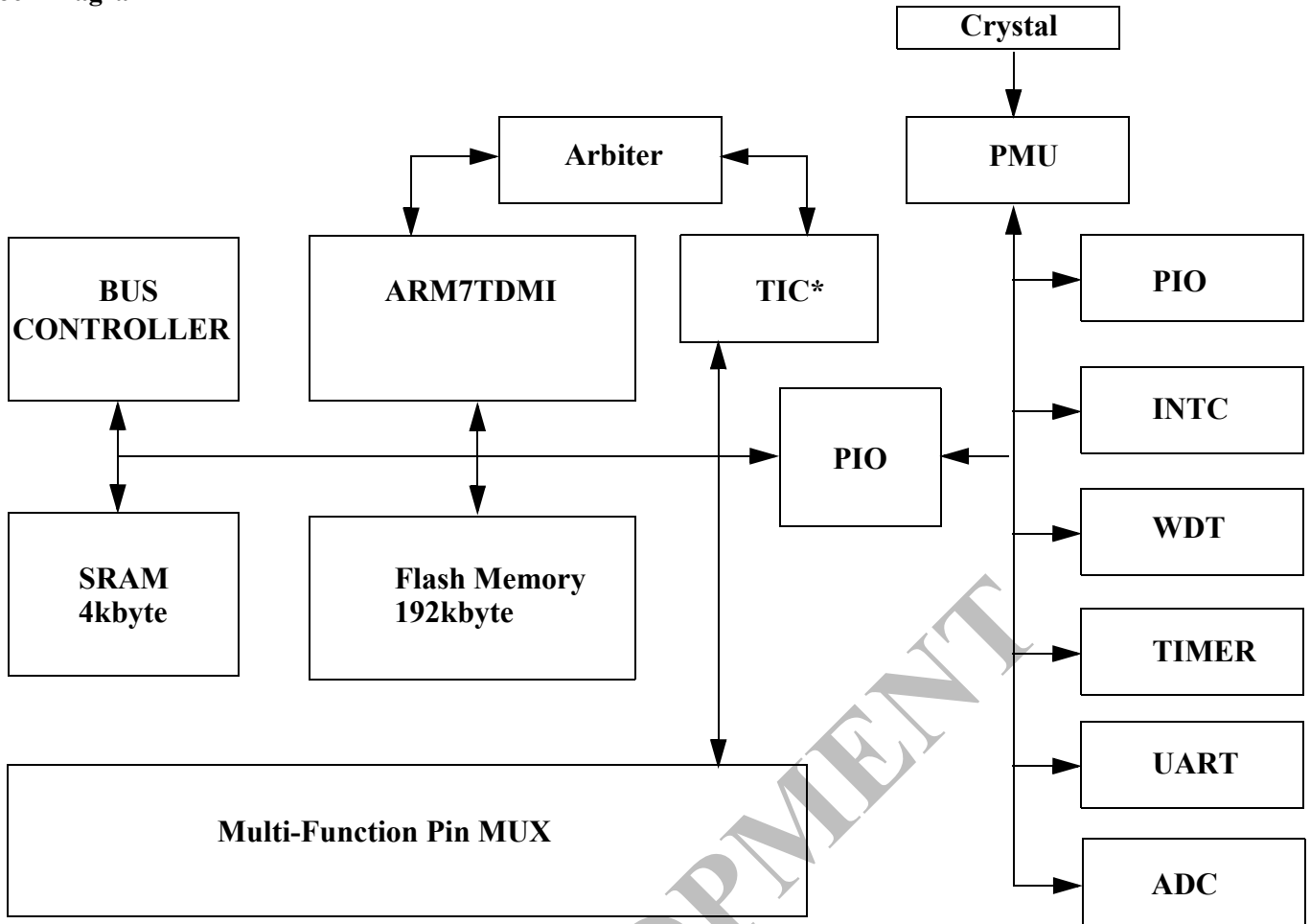
The AX07CF064 is a 32-bit MCU with embedded flash memory based on the ARM7TDMI core. The AX07CF064 is a sub-set of the popular AX07CF92 with reduced flash memory and functionality, intended for space- or cost-conscious applications. The AX07CF064 contains the following functions: 64Kbytes flash memory, 4Kbytes SRAM, 3-channel 16-bit timer, watch dog timer, 2-channel UART, programmable priority interrupt controller, 55 bits PIO, bus controller including chip select logic. These functions are implemented using the AMBA on-chip modular architecture.

The major functional blocks are described in more detail on the following pages. A complete users manual can be downloaded from our website at www.aeroflex.com/ARM7.



AX07CF xxx-80 Pinout			80-pin TQFP Package		
Pin Number	Default Function*	Alternate Function	Pin Number	Default Function*	Alternate Function
1	Vdd		41	Vss	
2	TIOCA4	CS5/PB2	42	nWAIT	P60
3	TIOCB4	CS4/PB3	43	nBREQ	P61
4	TMS	PB4	44	nBACK	P62
5	TDO	PB5	45	CLKO	P67
6	TDI	PB6	46	nSTBY	
7	TCK	PB7	47	nRES	
8	TVppd		48	nTRST	P97
9	Vss		49	Vss	
10	TxD0	P90	50	XTALout	
11	RxD0	P91	51	XTALin	
12	TxD1	P92	52	Vdd	
13	RxD1	P93	53	P63	nAS
14	P40	D0	54	P64	nRD
15	P41	D1	55	P65	nHWR
16	P42	D2	56	P66	nLWR
17	P43	D3	57	MODE0	
18	Vss		58	MODE1	
19	P44	D4	59	MODE2	
20	P45	D5	60	AVdd	
21	P46	D6	61	AVref	
22	P47	D7	62	AN0	
23	Vdd		63	AN1	

Block Diagram



*TIC: Test Interface Controller

Operation Modes

The AX07CF064 has three operation modes as shown in Table 1. The external pin functionality can be changed by setting the external Mode pin and/or by configuring the on-chip Pin Mux registers. Modes enabling external data buses will have a corresponding reduction in pins available for general purpose I/O ports. When changing modes the memory is remapped accordingly.

The usual mode of operation is Flash-boot mode (mode 5), when the device will boot from the on-chip flash. Boot mode (mode 7) is for use when a user program is not available, such as the first time on-board programming is performed, or if the user program is accidentally erased.

Table 1: Mode Description

MODE	MODE DESCRIPTION
0, 1	Reserved for Test
2	Boot from external 8-bit data bus with 64KBytes of Address Range
3	Reserved
4	Reserved
5	Flash-boot mode (microcomputer mode)
6	Reserved
7	UART-boot mode (microcomputer mode)

Flash memory can be reprogrammed in any mode, however in modes the control program for program/erase operations must first be transferred to, and executed from RAM, since the flash memory itself cannot be read while being programmed or erased.

The Mode pins also determine if only on-chip memory is to be used (microcomputer mode, modes 5 and 7) or if external memory is also available (mode 2 which bypasses the on-board flash completely).

The ARM7 TDMI Core

The ARM7 TDMI is a member of the ARM family of general-purpose 32-bit microprocessors, which offer high performance and very low power consumption. This processor employs a unique architectural strategy known as THUMB, which makes it ideally suited to high volume applications with memory restrictions or applications where code density is an issue. The key idea behind THUMB is a super reduced instruction set. Essentially, the ARM7TDMI has two instruction sets, the standard 32-bit ARM set and the 16-bit THUMB set. The THUMB set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor by using 16-bit registers. This is possible because THUMB code operates on the same 32-bit register set as ARM code.

- 32bit RISC architecture
- Low power consumption
- ARM7TDMI core with:
 - On-chip ICEbreaker debug support
 - 32-bit x 8 hardware multiplier
 - Thumb decompressor

- Utilizes the ARM7TDMI embedded processor
 - High performance 32-bit RISC architecture
 - High density 16 bit instruction set (THUMB code)
- Fully static operation: 0 ~ 50MHz
- 3-stage pipeline architecture (Fetch, decode, and execution stages)
- Enhanced ARM software toolkit

THUMB code is able to provide up to 65% of the code size of ARM, and 160% of the performance of an equivalent ARM processor connected to a 16-bit memory system.

Bus Controller

The AX07CF064 has an on-chip bus controller that manages the external address space divided into six areas, which can consist of SRAM, ROM, Flash-memory or off-chip peripheral devices. The bus specifications, such as bus width and number of access states, can be set independently for each area, enabling multiple memories to be connected easily.

- 8-bit access
- Active-low chip select signals (nCS0 to nCS5) can be output for areas 0 to 5
- Bus specifications can be set independently for each area
- Support Little-Endian Memory Format
- Variable wait states (up to 64 waits)
- Bus transfers can be extended using the nWAIT signal.
- Each area is 16MB in size (when SM='0' in PMU), or 1MB (when SM='1' in PMU) in size and can be programmed individually. (These sizes apply to the memory map within the device. Regardless of use only 16-bits are used in each area to access up to 64KB of external memory).

Power Management Unit

The PMU block is used to optimize device power dissipation. It consists of a clock controller and a reset controller. The user can control the internal clocks of the embedded peripherals and the main clock of the MCU by setting the PMU registers. The MCU has three reset sources: external power-on reset, soft-reset by PMU, and overflow reset by WDT. The PMU has status registers that hold the reset value and PMU status. To improve power management, support for a power-saving mode is included whereby bus clocks may be disabled (or dropped to a lower frequency).

Programmable Interrupt Controller

- Asynchronous interrupt controller
- 6 external interrupt sources
- 11 internal interrupt sources
- Low interrupt latency
- Selectable level- or edge-trigger on all interrupt source inputs
- Each interrupt source and output signal is maskable
- Selectable output paths (IRQ or FIQ) for each interrupt source

Watchdog Timers

- Watchdog timer mode and interval timer mode
- Generates an interrupt signal to the interrupt controller in either mode
- Outputs reset signals to the PMU (Power Management Unit)
- Eight counter clock sources
- Selection of whether to reset the chip internally or not
- Two types of reset signal: power-on reset and manual reset

The AX07CF064 has a one-channel watchdog timer (WDT) for monitoring system operations. If the system locks up and the timer counter overflows without being rewritten correctly by the CPU, a reset signal is output to the PMU. When this watchdog function is not needed, the WDT can be used as an interval timer. In the interval timer mode, an interval timer interrupt is generated at each counter overflow. The WDT has a clock generator that produces eight counter clock sources. The clock signals are obtained by dividing down the frequency of the system clock. Users can select one of eight internal clock sources for input to the counter.

General Purpose Timer Unit

- Three channels with 16-bit counters
- Six different pulse outputs
- Six different pulse inputs
- Independent functionality with 12 general registers
- Compare match waveform output function

- Input capture function
- Counter-clearing function at compare match or input capture mode
- Synchronizing mode
- PWM mode
- 18 interrupt sources
- Selectable 4 internal clock sources and 4 external clock sources

The AX07CF064 has a general-purpose timer unit (GPTU) with six channels of 16-bit timers. There are two counter operation modes: a free-running mode and a periodic mode. Each channel has independent operating modes. There are common functions for each channel: counter operation, input capture, compare match, PWM, and synchronized clear and write.

UARTs

The UART module is functionally identical to the 16550. The UART can be put into an alternate mode (FIFO mode) to relieve the CPU of excessive software overhead. In this mode internal FIFOs are activated allowing 16 bytes plus 3 bits of error data per byte in the RCVR FIFO, to be stored in both receive and transmit modes. All the logic is on the chip to minimize the system overhead and maximize system efficiency.

The UART performs serial-to-parallel conversion on data characters received from a peripheral device and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during operation. Status information includes the type and condition of the transfer operations performed by the UART, as well as any error conditions (parity, overrun, framing, or break interrupt).

The UART includes a programmable baud rate generator that is capable of dividing the timing reference clock input by divisors of 1 to 65535 and producing a 16x clock for driving the internal transmitter logic. Provisions are also included to use this 16x clock to drive the receiver logic. In addition to baud rate generation, the UART also includes a clock divider which divides the input system clock by setting an 8-bit divider register.

The UART has a processor interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing required to handle the communications link. The standard 16450/16550 UART features modem control signals which are duplicated internally, but are concealed from the outside.

- Compatible with 16550 UART, except modem control functions
- After reset, all registers are identical to the 16450 register set.
- The FIFO mode transmitter and receiver are each buffered with 16-byte FIFO's to reduce the number of interrupts presented to the CPU.
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from the serial data.
- Hold and shift registers in the 16450 mode eliminate the need for precise synchronization between the CPU and serial data.
- Independently controlled transmit, receive, line status and data set interrupts.
- Programmable baud generator divides any input clock by 1 to 65535 and generates 16x clock
- Input clock divider by setting an 8-bit divider register.
- Independent receiver clock input.
- Fully programmable serial-interface characteristics:
 - 5-, 6-, 7- or 8-bit characters
 - Even, odd, or no-parity bit generation and detection
 - 1-, 1.5- or 2-stop bit generation and detection
 - Baud generation (DC to 256k baud)
- False start bit detection.
- Complete status reporting capabilities.
- Line break generation and detection.
- Internal diagnostic capabilities.
- Loopback controls for communications link fault isolation
- Full prioritized interrupt system controls.

General Purpose I/O Ports

The GPIO is an APB peripheral which provides 55 bits of programmable input/output divided into 9 ports; port A, port B, port 1, port 2, port 4, port 6, port 7, and port 8, and port 9. Each pin is configurable as either an input or an output. At system reset, ports A, 1, 8, 9 are set by default to inputs and ports B, 2, 4, 6, 7 set to outputs.

Each port has a data register and a data direction register. The data direction register defines whether each individual pin is an input or an output. The data register is used to read the value of the GPIO pins, both input and output, as well as to set the values of pins that are configured as outputs. The input pins are 5-V tolerant.

On-chip SRAM

The AX07CF064 has 4-kbytes of high-speed static RAM on-chip. The RAM is connected to the CPU by a 32-bit ASB (Advanced System Bus) bus. The CPU accesses byte data,

half-word data, and word data in one cycle, making the RAM useful for rapid data transfer.

Data can be read from the on-chip SRAM, or data can be written to the SRAM in a single clock cycle through the ASB bus. The SRAM is implemented as a single module with 32-bit data bus and control lines. The single cycle access makes the SRAM ideal for use as a program area, stack area, or data area, which requires high-speed access. The contents of the on-chip SRAM are retained in both standby and power-down modes. Since the on-chip RAM is connected to the CPU by an internal 32-bit data bus, it can be written and read by word access. It can also be written and read by half-word or byte access.

On-chip Flash Memory

The AX07CF064 has 64-Kbytes of on-chip flash memory. This memory is organized as 4 blocks, 2x8K and 2x24K. The flash memory is connected to the CPU by a 32-bit data bus. The CPU accesses both half-word and word data in several states depending on the wait register value.

- Memory organization: 32K x 16 (512kbit)
- Operating Voltage: 3.0V ~ 3.6V (Vcc)
- Programming Voltage: 4.5~5.5V (FTVPPD)
- Random access time: 90nsec
- Program time: typ. 100usec/word
- Erase block size: 24KB x 2, 8KB x 2
- Block erase time: typ. 1.5sec/32KB (pre program + erase)
- Multiple block erase command support (maximum 4 blocks)
- Endurance: Min. 100 cycles
- Both on-chip (user/boot mode) and on-board (PROM mode) program/erase support
- Bi-directional Data IO
- Operating current: Standby mode: 10uA
- Read/Program/Erase mode: max. 20mA

The Flash memory can be programmed either externally (UART boot mode) or from the user program (Flash boot mode). In the latter case the control program for erase/program must first be transferred to, and executed from RAM.

Analog-to-Digital Converter

The AX07CF064 has a 10-bit successive-approximation A/D converter with six analog input channels. The input channels are multiplexed into the converter. The serial output is configured to interface with standard shift registers. The differential analog voltage input allows for common-mode rejection or offset of the analog zero input voltage value. The voltage refer-

ence input can be adjusted to effectively scale the input voltage span while retaining the full 10 bits of resolution.

- 10-bit resolution
- 5 input channels
- Reference voltage input (AVREF) to scale the analog input range
- High-speed conversion: minimum 2us per channel (with 8MHz ADC clock)
- Analog input range: GND to AVREF
- A/D conversion results are transferred to individual data registers for each channel.
- Sample-and-hold function
- Optional A/D End Interrupt

IN DEVELOPMENT