



## A616316 Series

**Preliminary**

**64K X 16 BIT HIGH SPEED CMOS SRAM**

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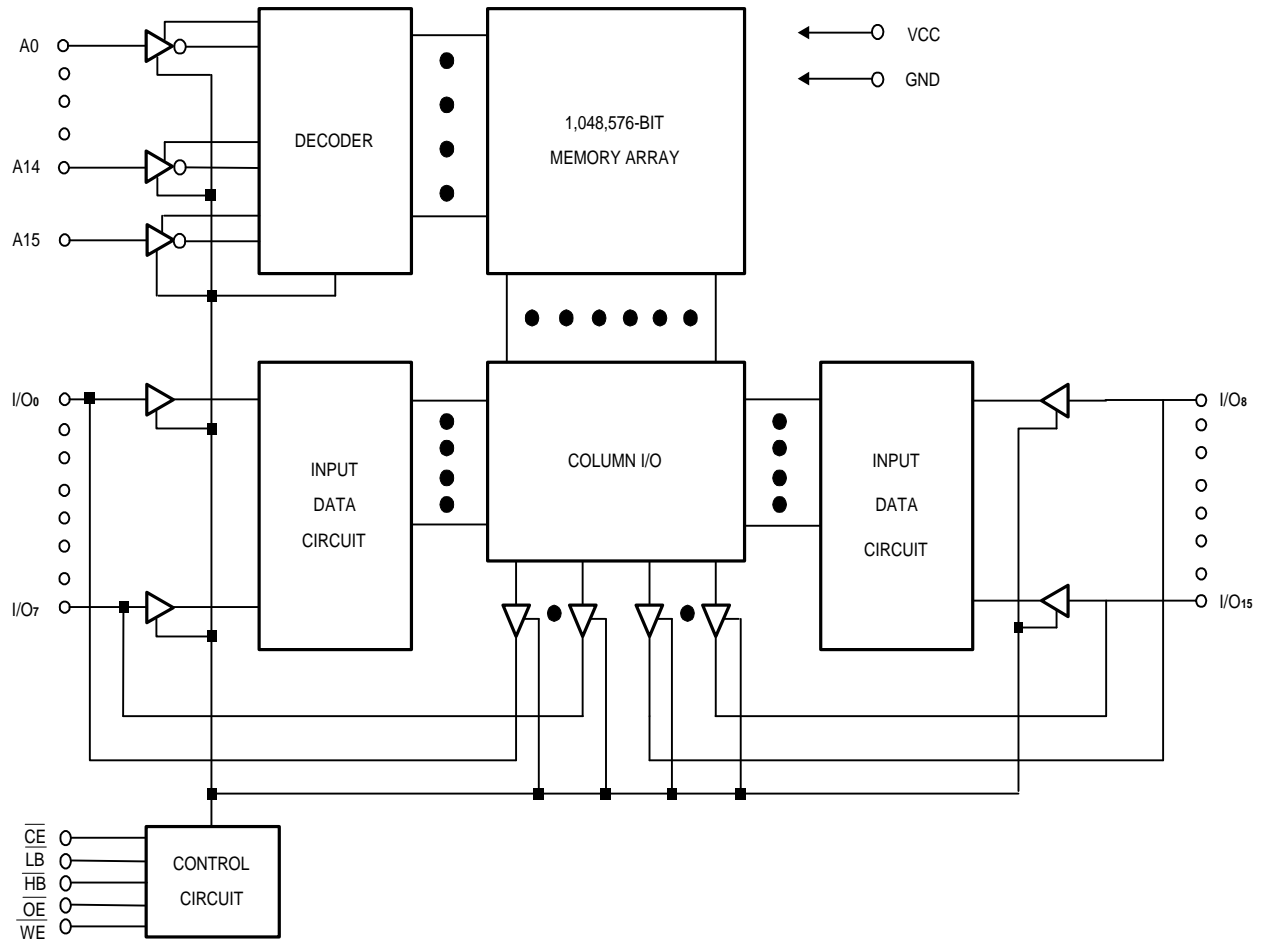
### Document Title

**64K X 16 BIT HIGH SPEED CMOS SRAM**

### Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Issue Date</u>	<u>Remark</u>
0.0	Initial issue	July 14, 2000	Preliminary



**Block Diagram**


**Pin Description - SOJ/TSOP(II)**

Pin No.	Symbol	Description
1 - 5, 18 - 21, 24 - 27, 42 - 44	A0 - A15	Address Inputs
6	$\overline{CE}$	Chip Enable Input
7 - 10, 13 - 16, 29 - 32, 35 - 38	I/O <sub>0</sub> - I/O <sub>15</sub>	Data Input/Outputs
17	$\overline{WE}$	Write Enable Input
39	$\overline{LB}$	Byte Enable Input (I/O <sub>0</sub> to I/O <sub>7</sub> )
40	$\overline{HB}$	Byte Enable Input (I/O <sub>8</sub> to I/O <sub>15</sub> )
41	$\overline{OE}$	Output Enable Input
11, 33	VCC	Power
12, 34	GND	Ground
22, 23, 28	NC	No Connection

**Recommended DC Operating Conditions**

 (T<sub>A</sub> = 0°C to + 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	-	VCC + 0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3	-	0.8	V
C <sub>L</sub>	Output Load	-	-	30	pF



**Absolute Maximum Ratings\***

VCC to GND ..... -0.5V to +7.0V  
 IN, IN/OUT Volt to GND ..... -0.5V to VCC + 0.5V  
 Operating Temperature, Topr ..... 0°C to +70°C  
 Storage Temperature, Tstg ..... -55°C to +125°C  
 Power Dissipation, P<sub>T</sub> ..... 1.0W  
 Soldering Temp. & Time ..... 260°C, 10 sec

**\*Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**DC Electrical Characteristics** (T<sub>A</sub> = 0°C to + 70°C, VCC = 5V±10%, GND = 0V)

Symbol	Parameter	A616316-12		A616316-15		Unit	Conditions
		Min.	Max.	Min.	Max.		
I <sub>LI</sub>	Input Leakage	-	2	-	2	μA	V <sub>IN</sub> = GND to VCC
I <sub>LO</sub>	Output Leakage	-	2	-	2	μA	$\overline{CE} = V_{IH}, \overline{OE} = V_{IH}$ V <sub>I/O</sub> = GND to VCC
I <sub>CC1</sub> (2)	Dynamic Operating Current	-	170	-	165	mA	$\overline{CE} = V_{IL}, I_{I/O} = 0$ mA Min. Cycle, Duty = 100%
I <sub>SB</sub>	Standby Power Supply Current	-	25	-	25	mA	$\overline{CE} = V_{IH}$
I <sub>SB1</sub>		-	8	-	8	mA	$\overline{CE} \geq VCC - 0.2V,$ V <sub>IN</sub> ≥ VCC -0.2V or V <sub>IN</sub> ≤ 0.2V
V <sub>OL</sub>	Output Low Voltage	-	0.4	-	0.4	V	I <sub>OL</sub> = 8 mA
V <sub>OH</sub>	Output High Voltage	2.4	-	2.4	-	V	I <sub>OH</sub> = -4 mA

- Notes: 1. V<sub>IL</sub> = -3.0V for pulses less than 20 ns.  
 2. I<sub>CC1</sub> is dependent on output loading, cycle rates, and Read/Write patterns.

**Truth Table**

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{HB}$	I/O <sub>0</sub> to I/O <sub>7</sub> Mode	I/O <sub>8</sub> to I/O <sub>15</sub> Mode	VCC Current
H	X	X	X	X	Not selected	Not selected	I <sub>SB1</sub> , I <sub>SB</sub>
L	L	H	L	L	Read	Read	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC</sub>
			L	H	Read	High - Z	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC</sub>
			H	L	High - Z	Read	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC</sub>
L	X	L	L	L	Write	Write	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC</sub>
			L	H	Write	Not Write/Hi - Z	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC</sub>
			H	L	Not Write/Hi - Z	Write	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC</sub>
L	H	H	L	X	High - Z	High - Z	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC</sub>
			X	L	High - Z	High - Z	I <sub>CC1</sub> , I <sub>CC2</sub> , I <sub>CC</sub>
X	X	X	H	H	Not selected	Not selected	I <sub>SB1</sub> , I <sub>SB</sub>

Note: X = H or L

**Capacitance** (T<sub>A</sub> = 25°C, f = 1.0MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C <sub>IN</sub> *	Input Capacitance	-	6	pF	V <sub>IN</sub> = 0V
C <sub>IO</sub> *	Input/Output Capacitance	-	8	pF	V <sub>IO</sub> = 0V

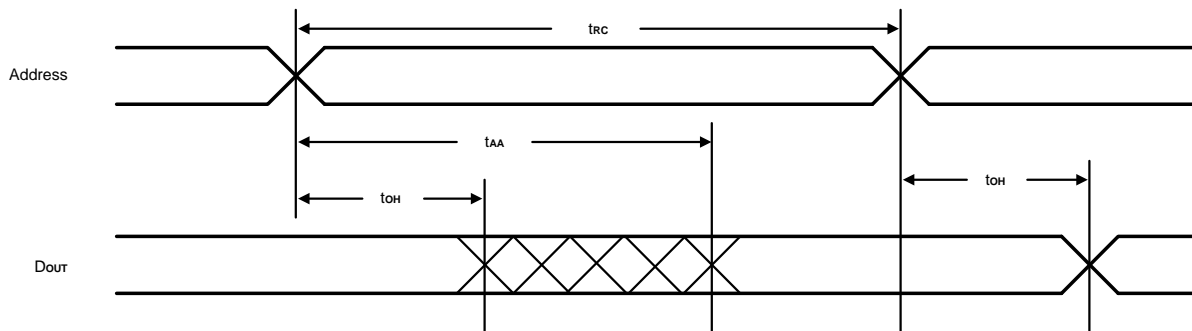
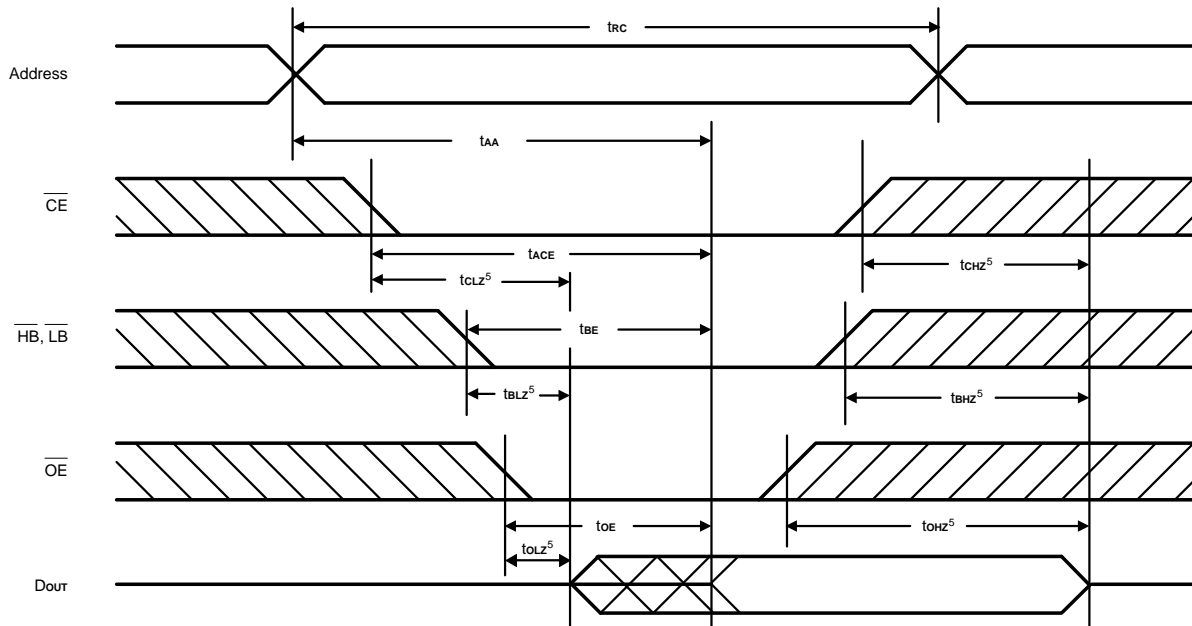
\* These parameters are sampled and not 100% tested.



**AC Characteristics** ( $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ,  $V_{CC} = 5\text{V}\pm 10\%$ )

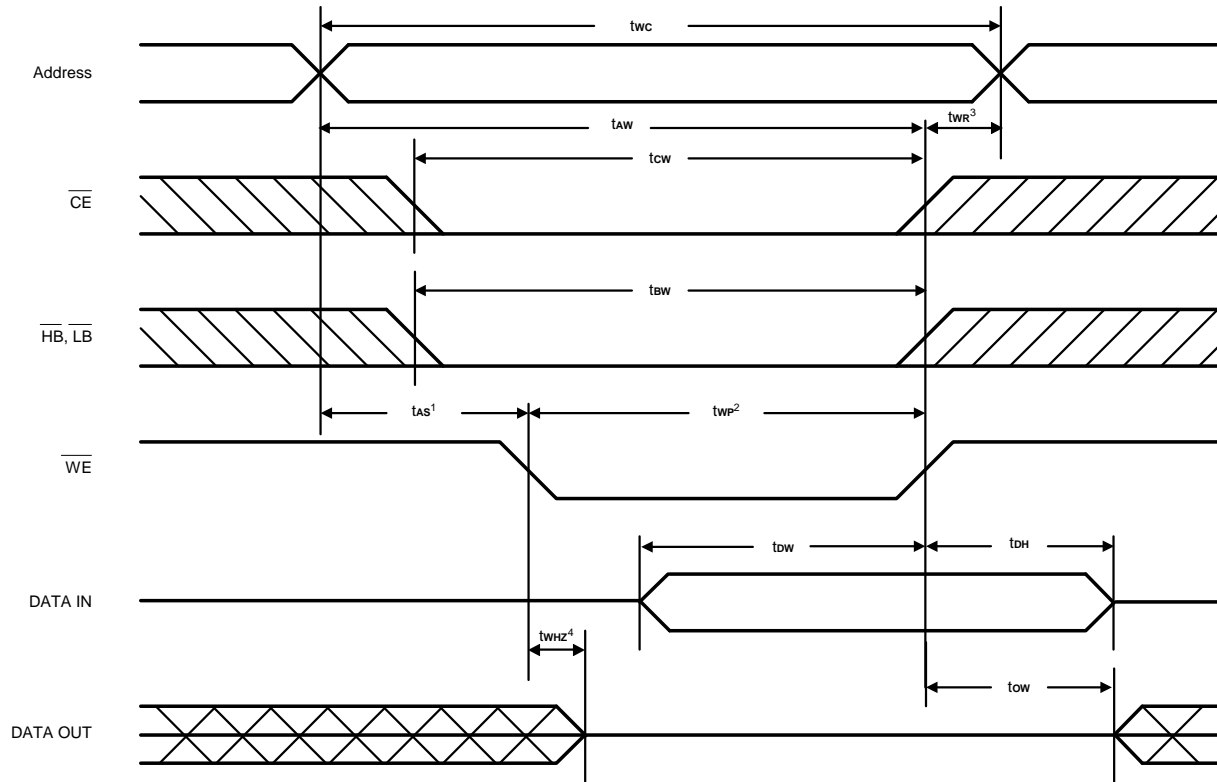
Symbol	Parameter	A616316-12		A616316-15		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
trc	Read Cycle Time	12	-	15	-	ns
tAA	Address Access Time	-	12	-	15	ns
tACE	Chip Enable Access Time	-	12	-	15	ns
toE	Output Enable to Output Valid	-	6	-	8	ns
tCLZ	Chip Enable to Output in Low Z	3	-	3	-	ns
toLZ	Output Enable to Output in Low Z	0	-	0	-	ns
tCHZ	Chip Disable Output in High Z	0	6	-	8	ns
toHZ	Output Disable to Output in High Z	0	6	0	8	ns
toH	Output Hold from Address Change	3	-	3	-	ns
Write Cycle						
tWC	Write Cycle Time	12	-	15	-	ns
tCW	Chip Enable to End of Write	10	-	12	-	ns
tAS	Address Setup Time of Write	0	-	0	-	ns
tAW	Address Valid to End of Write	10	-	12	-	ns
tWP	Write Pulse Width	10	-	12	-	ns
tWR	Write Recovery Time	0	-	0	-	ns
tWHZ	Write to Output in High Z	0	6	0	8	ns
tdW	Data to Write Time Overlap	6	-	7	-	ns
tdH	Data Hold from Write Time	0	-	0	-	ns
tOW	Output Active from End of Write	3	-	3	-	ns

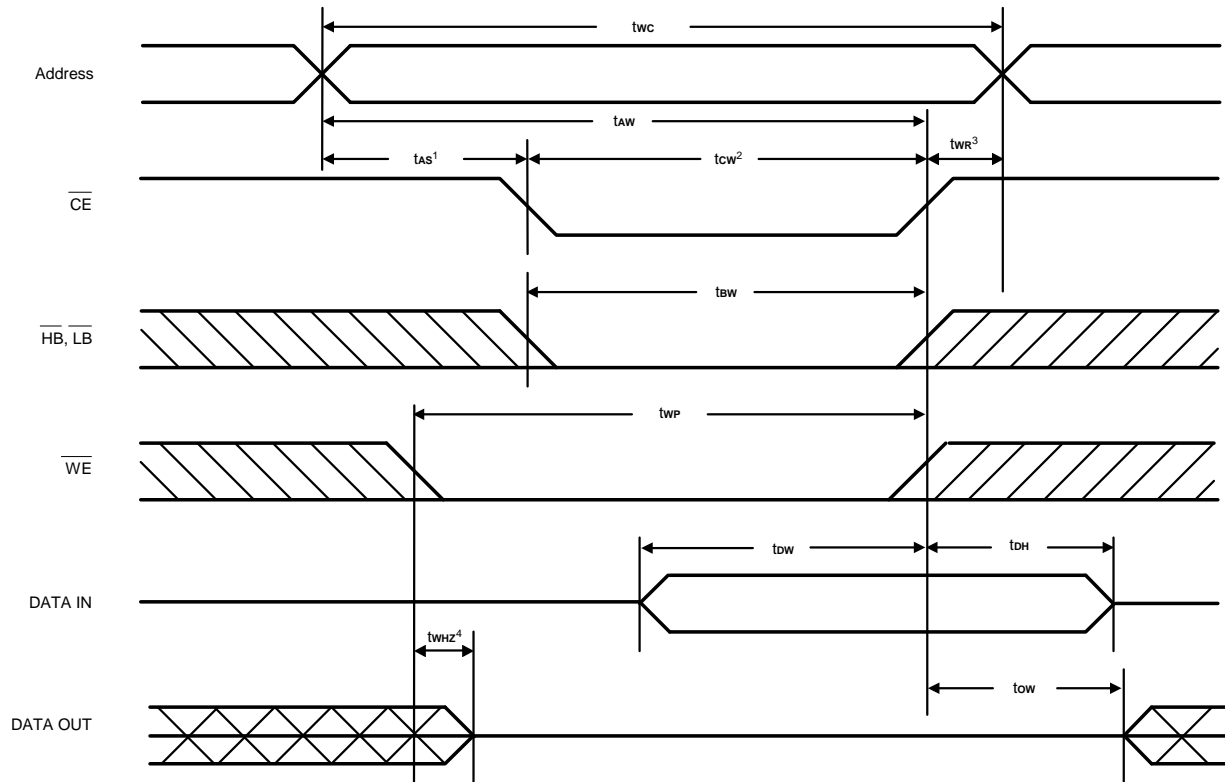
Notes: tCHZ, toHZ and tWHZ are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

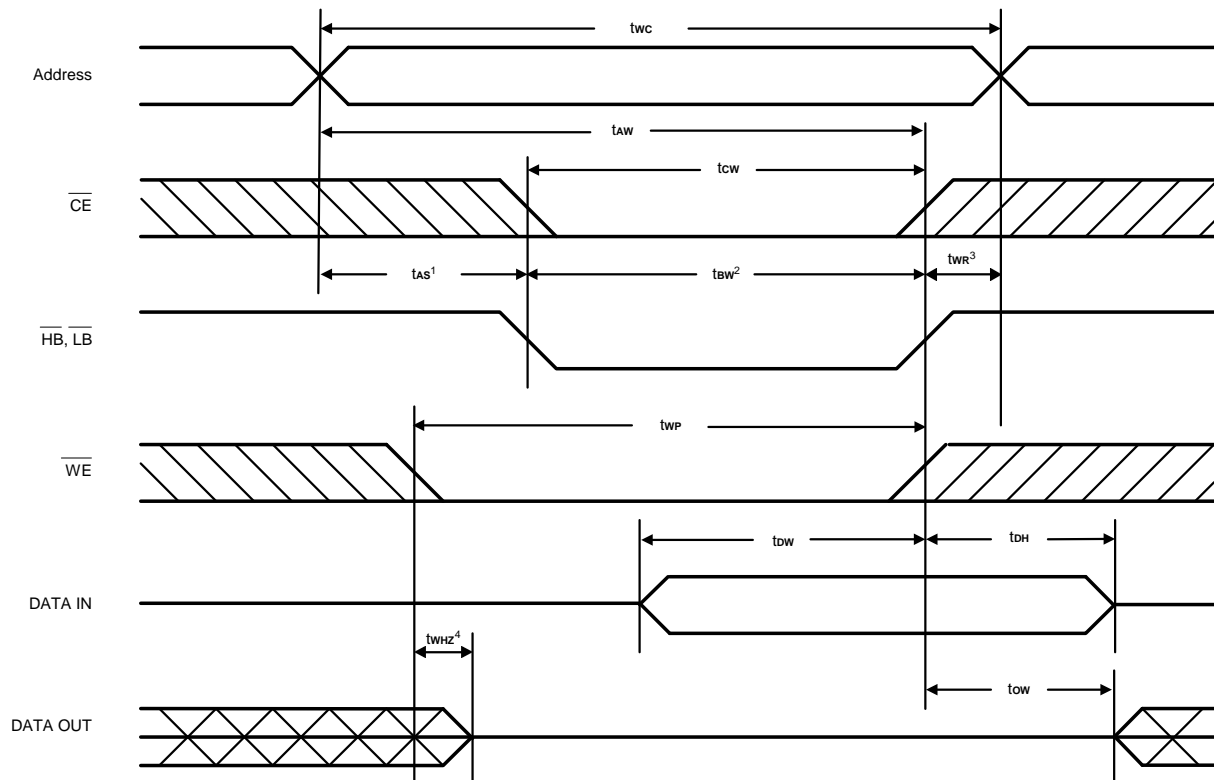
**Timing Waveforms**
**Read Cycle 1<sup>(1, 2, 4)</sup>**

**Read Cycle 2<sup>(1, 2, 3)</sup>**


- Notes:
1.  $\overline{WE}$  is high for Read Cycle.
  2. Device is continuously enabled  $\overline{CE} = V_{IL}$ ,  $\overline{HB} = V_{IL}$  and, or  $\overline{LB} = V_{IL}$ .
  3. Address valid prior to or coincident with  $\overline{CE}$  and ( $\overline{HB}$  and, or  $\overline{LB}$ ) transition low.
  4.  $\overline{OE} = V_{IL}$ .
  5. Transition is measured  $\pm 500\text{mV}$  from steady state. This parameter is sampled and not 100% tested.



**Timing Waveforms (continued)**
**Write Cycle 1  
(Write Enable Controlled)**


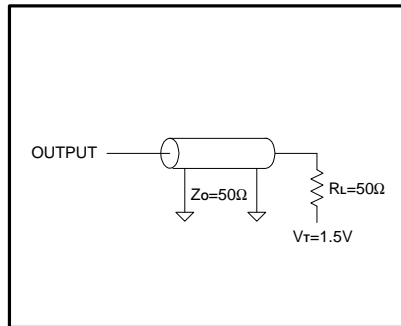
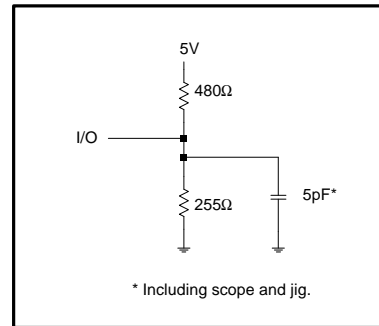
**Timing Waveforms (continued)**
**Write Cycle 2  
(Chip Enable Controlled)**


**Timing Waveforms (continued)**
**Write Cycle 3  
(Byte Enable Controlled)**


- Notes:
1.  $t_{AS}$  is measured from the address valid to the beginning of Write.
  2. A Write occurs during the overlap ( $t_{WP}$ ,  $t_{BW}$ ) of a low  $\overline{CE}$ ,  $\overline{WE}$  and ( $\overline{HB}$  and, or  $\overline{LB}$ ).
  3.  $t_{WR}$  is measured from the earliest of  $\overline{CE}$  or  $\overline{WE}$  or ( $\overline{HB}$  and, or  $\overline{LB}$ ) going high to the end of the Write cycle.
  4.  $\overline{OE}$  level is high or low.
  5. Transition is measured  $\pm 500\text{mV}$  from steady state. This parameter is sampled and not 100% tested.

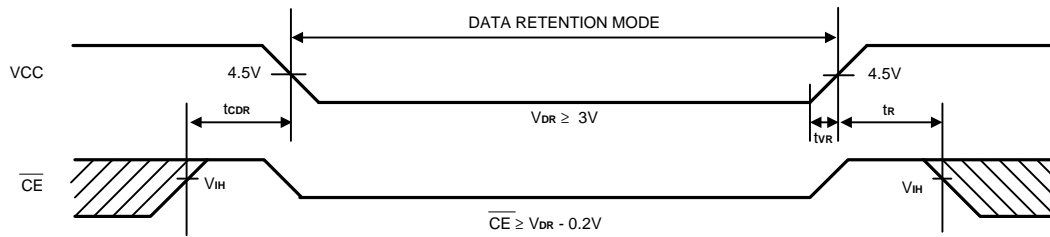
**AC Test Conditions**

Input Pulse Levels	0V to 3.0V
Input Rise And Fall Time	3 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	See Figures 1 and 2


**Figure 1. Output Load**

**Figure 2. Output Load for  $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$ ,  $t_{OHZ}$ ,  $t_{WHZ}$ , and  $t_{OW}$** 
**Data Retention Characteristics** ( $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ )

Symbol	Parameter	Min.	Max.	Unit	Conditions
$V_{DR}$	VCC for Data Retention	3	5.5	V	$\overline{CE} \geq VCC - 0.2V$
$I_{CCDR}$	Data Retention Current	-	1	mA	$VCC = 3.0V$ $\overline{CE} \geq VCC - 0.2V$ $V_{IN} \geq VCC - 0.2V$ or $V_{IN} \leq 0.2V$
$t_{CDR}$	Chip Disable to Data Retention Time	0	-	ns	See Retention Waveform
$t_R$	Operation Recovery Time	$TRC^*$	-	ms	

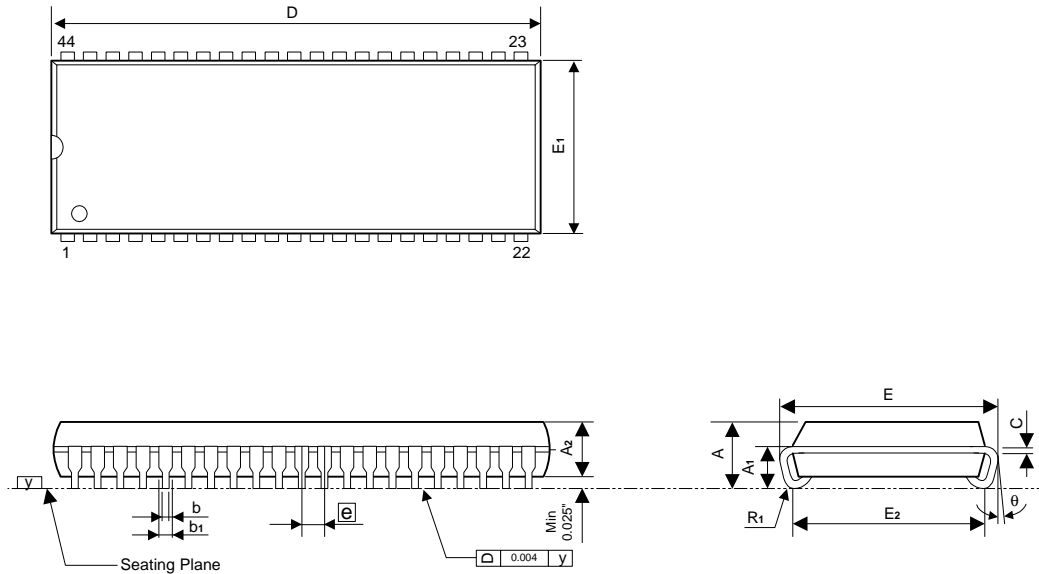
 $trc$  = Read Cycle Time

**Low VCC Data Retention Waveform**

**Ordering Information**

Part No.	Access Time (ns)	Operating Current Max. (mA)	CMOS Standby Max. (mA)	Package
A616316S-12	12	120	8	44L SOJ
A616316V-12				44L TSOP(II)
A616316S-15	15	100	8	44L SOJ
A616316V-15				44L TSOP(II)

**Package Information**
**SOJ 44L Outline Dimensions**

unit: inches/mm



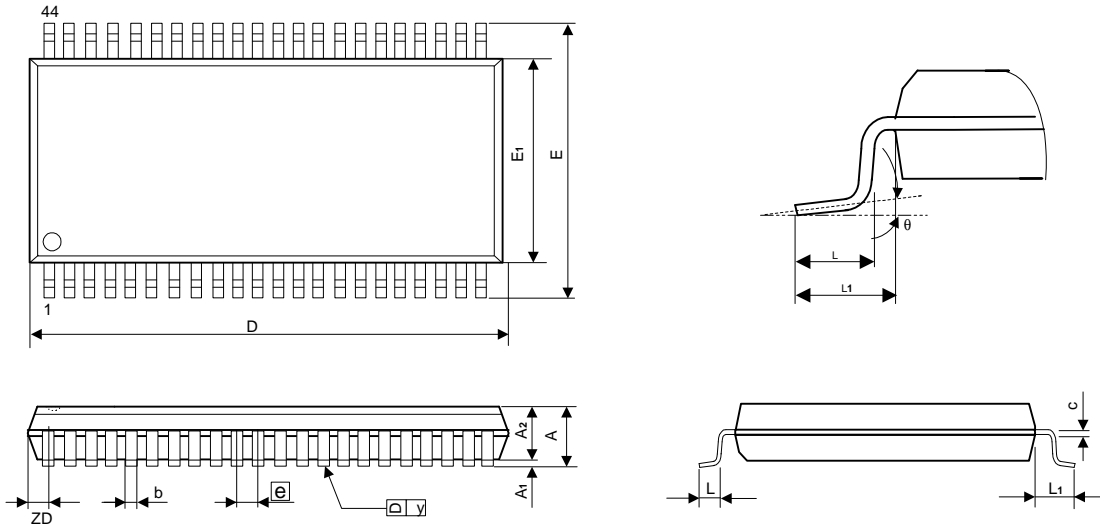
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.128	0.138	0.148	3.25	3.51	3.76
A1	0.082	-	-	2.08	-	-
A2	0.105	0.110	0.115	2.67	2.79	2.92
b	0.015	-	0.020	0.38	-	0.51
b1	0.026	0.028	0.032	0.66	0.71	0.81
C	0.007	-	0.013	0.18	-	0.21
D	1.120	1.125	1.130	28.45	28.58	28.70
E	0.435	0.440	0.445	11.05	11.18	11.30
E1	0.394	0.400	0.405	10.01	10.16	10.29
E2	0.370 BSC			9.40 BSC		
$\square e$	0.050 BSC			1.27 BSC		
R1	0.030	0.035	0.040	0.76	0.89	1.02
$\theta$	0°	-	10°	0°	-	10°

**Notes:**

1. The maximum value of dimension  $D$  includes end flash.
2. Dimension  $E$  does not include resin fins.
3. Dimension  $E_1$  is for PC Board surface mount pad pitch design reference only.

**Package Information**
**TSOP 44L (Type II) Outline Dimensions**

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.047	-	-	1.20
A1	0.002	-	0.006	0.05	-	0.15
A2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.012	-	0.018	0.30	-	0.45
c	0.005	-	0.008	0.12	-	0.21
D	0.720	0.725	0.730	18.28	18.41	18.54
ZD	0.032 REF			0.805 REF		
E	0.455	0.463	0.471	11.56	11.76	11.96
E1	0.395	0.400	0.405	10.03	10.16	10.29
L	0.019	0.023	0.027	0.49	0.59	0.69
L1	0.031 REF			0.80 REF		
[e]	0.031 BSC			0.80 BSC		
y	-	-	0.004	-	-	0.10
θ	0°	-	5°	0°	-	5°

**Notes:**

1. The maximum value of dimension D includes end flash.
2. Dimension E1 does not include resin fins.
3. Dimension ZD includes end flash.