
Standard Features

- 5.0V low-leakage CMOS transistors
- 17V and 40V high-voltage LDMOS transistors
- High-density, double-poly memory cell
- Isolated NMOS and LDMOS transistors
- Analog Resistors
- Dual Poly Capacitor
- Mono-silicon capacitors
- 3 layer metal
- Isolated and folded bond pads

Applications

- Power management integrated circuits
- High performance mixed-signal with embedded memory
- Motor/motion control
- Automotive monitor and control circuitry

Description

Atmel's AT35700, 0.35um, high-voltage CMOS foundry technology process was developed for mixed-signal and power management applications. The technology has LDMOS transistors capable of 17V and 40V operation and has 5.0V low-leakage CMOS transistors. The low-leakage CMOS has been engineered to minimize sub-threshold leakage currents making this technology ideal for portable electronic devices. Isolated NMOS and LDMOS transistors are included to minimize circuit noise. A large selection of on-chip analog resistors and capacitors are included to reduce off-chip component requirements. The technology supports placement of ESD and I/O transistors under the bond pads, thus minimizing the die size.

Included is Atmel's reliable double-poly, high-density memory cell. The cell can be used to create parallel EEPROM, serial EEPROM or Pseudo FLASH memory designs. Having embedded EEPROM provides large data storage capability as required in monitor and control applications and eliminates the need for additional memory chips.



**0.35um, 40.0V
HV CMOS
Foundry
Technology**

AT35700

Preliminary





Atmel's AT35700 0.35um HV CMOS Foundry Process Specifications

Table 1. CMOS Specifications

CMOS	Drawn Size (um)	V _t (V)	BV _{dss} (V)	Max Op (V)	Tox (angstrom)
LV NMOS	0.49	0.85	>6	6	110
LV PMOS	0.49	-0.9	<-6	-6	110
HV NMOS in Substrate/No Vt II	1.68	0.05	>15	10	275
HV NMOS in Substrate/Vt II	1.33	0.6	>12	10	275
HV NMOS in HV P-Well/No Vt II	1.54	0.3	>14	10	275
HV PMOS in HV N-Well/Vt II	1.12	-0.85	<-12	-12	275
HV PMOS in LV P-Well	1.505	-0.85	<-16	-12	275
HV BN+ NMOS in Substrate/No Vt II	2.765	-0.15	>16	16	275
HV BN+ NMOS in Substrate/Vt II	2.66	0.55	>16	12	275
HV BN+ NMOS in HV P-Well/No Vt II	2.765	0.3	>16	16	275
Isolated NMOS (NMOS in SVNWELL)	0.49	0.85	>6	6	110
LDNMOS	Note 1	Note 1	>40	40	275
LDPMOS	Note 1	Note 1	<-40	40	275

Note: 1. See DRM

Table 2. Resistor Specifications

Resistor	N-Well	N-LDD	Poly 2	BN+ in Poly 1	N+ in Poly 2	P+ in Poly 2
$\rho(\Omega/\blacksquare)$	3200	1500	135	300	100	170

Table 3. Capacitor Specifications

Capacitor	Capacitance (fF/um ²)	Equivalent Thickness (A)	Max Op (V)
Poly2 to Poly1 (ONO)	1.55	215	16
Poly2 to BN+ (SiO ₂)	1.15	290	16
Poly2 to BN+ (SiO ₂)	2.5	130	6
Poly2 to Poly1			40
Poly2 to LV N-Well	3	110	6



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