Features

- **High-speed ADC Family Companion Chip**
- **Selectable 1:2 or 1:4 DMUX Ratio**
- **Power Consumption: 2.6W**
- **LVDS Compatible Differential Data and Clock Inputs (100Ω Terminated)**
- **LVDS Compatible Differential Data and Data Ready Outputs**
- **Staggered or Simultaneous Data Outputs**
  - **11^{th} Bit = Ports A, B, C and D Clock in Staggered Mode**
- **Selectable Active Edge for Input and Output Clocks:**
  - **Only Rising: CLK and DR Mode**
  - **Rising and Falling: CLK/2 and DR/2 Mode**
- **Fine Tuning of Input Clock Path Delay**
  - **Compensation of External Data and Clock Path Misalignment and Skews**
  - **Once Tuned, Setting is Valid over Full Operating Frequency and Over Full Specified Temperature Range**
- **Additional 11^{th} Bit (Example: for Out-of-range Bit)**
- **Built-in Self Test (BIST)**
- **Stand-alone Tunable Delay Cell**
- **Power Supplies: V_{CCD} = 3.3V (Digital), V_{PLUSD} = 2.5V (Outputs)**
- **Power Consumption Reduction Mode: 1.1W**
- **EBGA240 Package**

Screening

- **Temperature Range:**
  - **$-40^{\circ}C < T_C; T_J < 110^{\circ}C$ (Industrial Grade)**

Applications

This DMUX enables users to process high-speed output data streams from fast analog-to-digital converters down to standard FPGA processor speed.

Description

The AT84CS001 is a monolithic high-speed demultiplexer, used to lower a 10-bit data stream of up to 2.2 Gsps guaranteed rate by a selectable 4 or 2 ratio (a 1:8 ratio may be achieved by interleaving two DMUXes).

The DMUX is a companion chip designed to fit perfectly with all of Atmel's high-speed ADCs and is capable of tracking the ADC's output sampling rate over all operating frequency and temperature ranges.

Thanks to its LVDS buffers, this DMUX can easily be interfaced with standard high-speed FPGAs (100Ω differentially terminated).

The AT84CS001 has the same footprint as Atmel's TS81102G0 DMUX, with a very similar pinout. Minimum re-design efforts are required to use this low-power DMUX. An application note "Replacing Atmel's TS81102G0 DMUX with Atmel's AT84CS001 LVDS DMUX" reference 5413, is available to assist in migrating from the TS81102G0 to the AT84CS001.

10-bit 1:2/4 2.2 GHz LVDS DMUX

AT84CS001

Summary

5402AS–BDC–11/04

Description

The AT84CS001 is a monolithic high-speed demultiplexer (DMUX) using high-speed Atmel technology.

It enables the user to lower a 10-bit stream of 2.2 Gsps maximum by a factor of two or four. One can obtain a 1:8 ratio by using two interleaved AT84CS001 devices. The maximum input data rate is 2.2 Gsps in both 1:2 and 1:4 ratios.

The AT84CS001 DMUX is capable of processing an 11-bit data flow. The additional 11th bit (IOR/IORN) may be connected for example to the out-of-range bit of a 10-bit ADC.

The input and output clocks as well as the input and output data are LVDS-compatible. Digital inputs are 100Ω differentially terminated on chip. Digital output buffers shall be terminated by a 100Ω differential ASIC load.

The improved architecture of the DMUX facilitates interfacing with high-speed ADCs operating at up to 2.2 Gsps. No tuning of the delay between the data and clock paths should be necessary since the data and clock paths are internally matched over the frequency and specified temperature range.

However, in the case of misalignment or skews between the external clock path and the data path, a fine delay tuning cell has been provided. Tuning may be requested for rates exceeding 2 GHz, where the data skews are more sensitive. This tunable delay cell is integrated in serial with the clock input. The delay is controlled by means of the CLKDACTRL analog control input. The tunable delay ranges from -250 ps to 250 ps for CLKDACTRL varying from $V_{CCD}/3$ to $(2 \times V_{CCD})/3$.

Two modes can be selected for the clock input (CLK and CLK/2) and the clock output (DR and DR/2):

- CLK and DR mode: only the rising edges of the input (CLK,CLKN) and output (DR, DRN) clocks are active. The input (or output) clock rate remains the same as the input or output data rate.
- CLK/2 and DR/2 mode: both the rising and falling edges of the input (CLK,CLKN) and output (DR, DRN) clocks are active. The input (or output) clock rate is half the input or output data rate.

The data outputs can be received at the DMUX output in two different modes:

- Staggered: even and odd bits are output with half a data period delay
- Simultaneous: even and odd bits are output at the same time

The AT84CS001 DMUX is started by the ASYNCRST control input that acts as a master asynchronous reset for the device. Once resetted, there is no loss of synchronization over an indefinite time period, therefore no additional incoming synchronous reset signal is required.

The power consumption of the AT84CS001 is 2.6W and can be reduced by approximately 60% of its nominal value by means of the SLEEP control input.

A standalone delay cell is provided. It features a typical 500 ps tuning range (± 250 ps around the center value of DACTRL analog control input).

A Built-in Self Test (BIST) is implemented for rapid debugging of the DMUX.

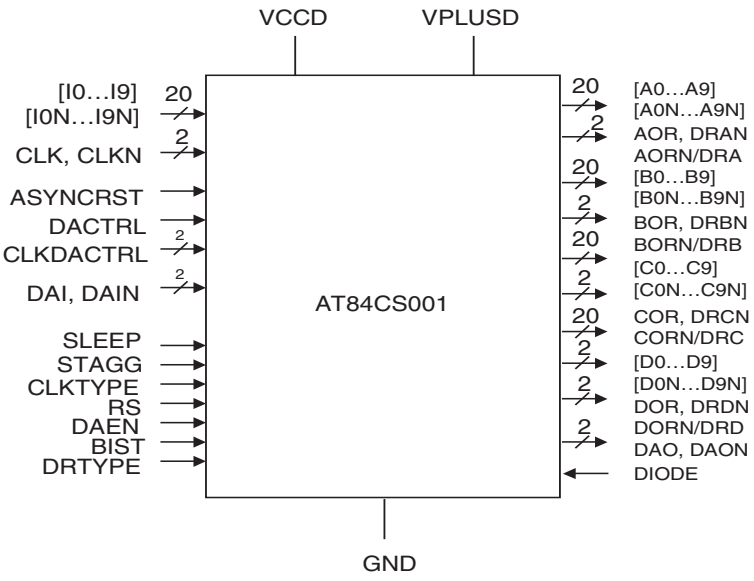
Die junction temperature monitoring is possible by sensing the voltage drop across a diode implemented close to the die's hot point after forcing a 1 mA bias current.

The AT84CS001 DMUX is a companion chip designed to fit perfectly with all of Atmel's high-speed ADCs.

Table 1. Description of Main Functions

Name	Function	Name	Function
V_{CCD}	Digital 3.3V power supply	D0…D9	In-phase output data port D
V_{PLUSD}	Output 2.5V power supply	D0N…D9N	Inverted phase output data port D
GND	Ground	DOR/DRDN DORN/DRD	Additional output bit port D or port D output clock in staggered mode
CLK, CLKN	Input clock signals	DAO, DAON	Output signals for stand-alone delay cell
I0…I9	In-phase input data (true)	DAI, DAIN	Input signals for stand-alone delay cell
I0N…I9N	Inverted phase input data (false)	DACTRL	Control signal for standalone delay cell
IOR, IORN	Additional input bit	CLKDACTRL	Control signal for clock delay cell
DR/DRN	Output clock signals	DAEN	Enable signal for standalone delay cell
A0…A9	In-phase output data port A	ASYNCRST	Asynchronous reset signal
A0N…A9N	Inverted phase output data port A	SLEEP	Sleep mode selection signal
AOR/DRAN AORN/DRA	Additional output bit port A or port A output clock in staggered mode	RS	DMUX ratio selection signal
B0…B9	In-phase output data port B	CLKTYPE	Input clock type selection signal
B0N…B9N	Inverted phase output data port B	DRTYPE	Output clock type selection signal
BOR/DRBN BORN/DRB	Additional output bit port B or port B output clock in staggered mode	STAGG	Staggered mode selection for data outputs
C0…C9	In-phase output data port C	BIST	Built-in self test enable
C0N…C9N	Inverted phase output data port C	DIODE	Diode for die junction temperature monitoring
COR/DRCN CORN/DRC	Additional output bit port C or port C output clock in staggered mode		

Figure 1. Device Pinout



Pin Description

Table 2. Pin Description

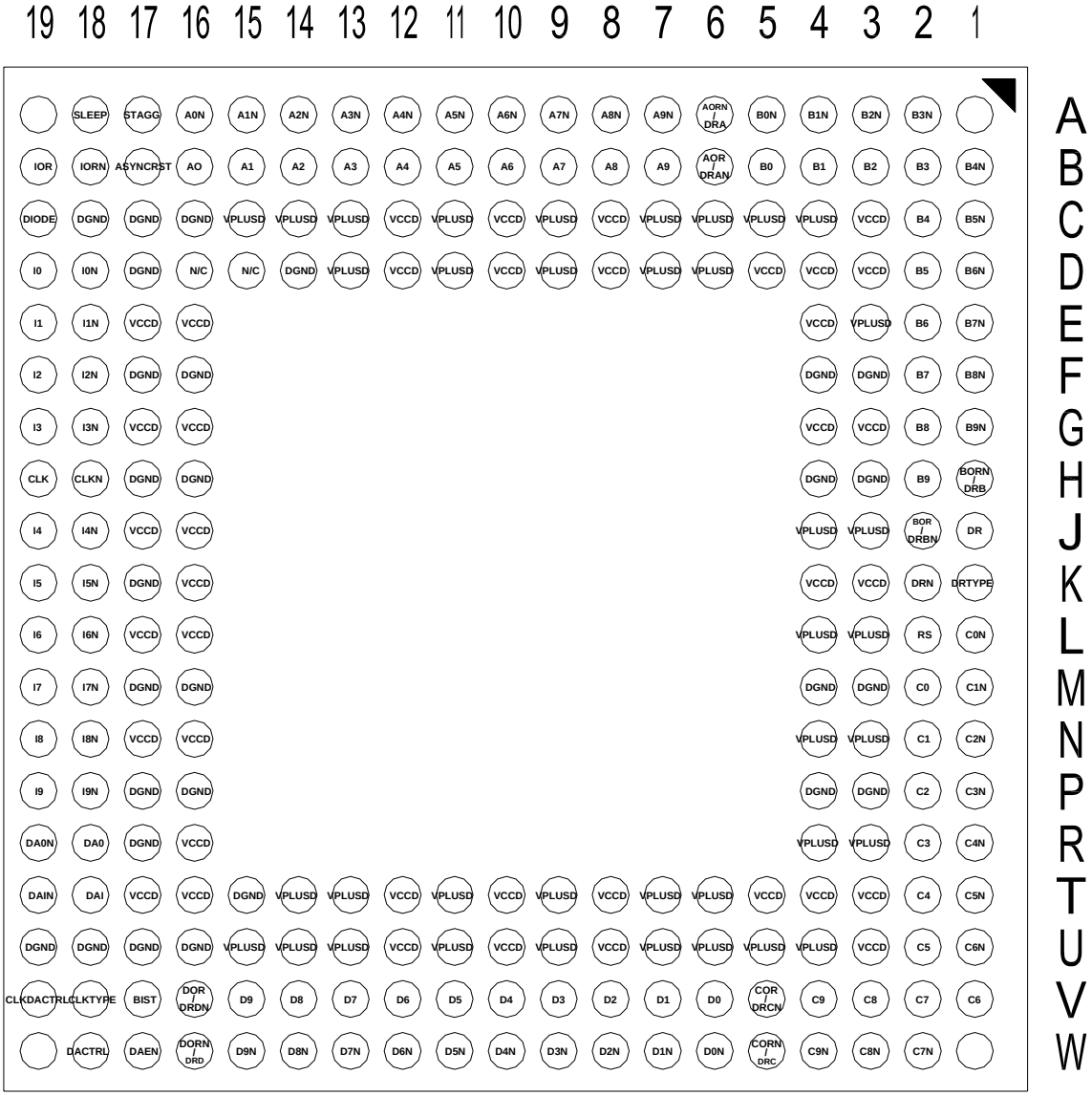
Symbol	Pin Number	Function
Power Supplies		
V_{CCD}	C12, C10, C8, C3, D12, D10, D8, D5, D4, D3, E4, E17, E16, G17, G16, G4, G3, J17, J16, K16, K4, K3, L17, L16, N17, N16, R16, T17, T16, T12, T10, T8, T5, T4, T3, U12, U1, U8, U3	Digital 3.3V supply
V_{PLUSD}	C15, C14, C13, C11 C9, C7, C6, C5, C4, D13, D11, D9, D7, D6, E3, J4, J3, L4, L3, N4, N3, R4, R3, T14, T13, T11, T9, T7, T6, U15, U14, 13, U11, U9, U7, U6, U5, U4	Output 2.5V supply
DGND	C18, C17, C16, D17, D14, F17, F16, F4, F3, H17, H16, H4, H3, K17, M17, M16, M4, M3, P17, P16, P4, P3, R17, T15, U19, U18, U17, U16	Ground
Digital Inputs		
I0, I1, I2, I3, I4, I5, I6, I7, I8, I9	D19, E19, F19, G19, J19, K19, L19, M19, N19, P19	In-phase (+) digital input signal
I0N, I1N, I2N, I3N, I4N, I5N, I6N, I7N, I8N, I9N	D18, E18, F18, G18, J18, K18, L18, M18, N18, P18	Inverted phase (-) digital input signal
IORN	B18	In-phase (+) digital input signal additional bit
IOR	B19	Inverted phase (-) digital input signal for additional bit
DAI	T18	In-phase (+) input signal for standalone delay cell
DAIN	T19	Inverted phase (-) input signal for standalone delay cell
Clock Inputs		
CLK	H19	In-phase (+) clock input
CLKN	H18	Inverted phase (-) clock input
Digital Outputs		
A0, A1, A2, A3, A4, A5, A6, A7, A8, A9	B16, B15, B14, B13, B12, B11, B10, B9, B8, B7	In-phase (+) digital outputs for port A A0 is the LSB, A9 is the MSB
A0N, A1N, A2N, A3N, A4N, A5N, A6N, A7N, A8N, A9N	A16, A15, A14, A13, A12, A11, A10, A9, A8, A7	Inverted phase (-) digital outputs for port A
AOR/DRAN	B6	In-phase (+) additional bit output for port A or inverted phase (-) output clock in staggered mode for port A
AORN/DRA	A6	Inverted phase (-) additional bit output for port A or in-phase (+) output clock in staggered mode for port A
B0, B1, B2, B3, B4, B5, B6, B7, B8, B9	B5, B4, B3, B2, C2, D2, E2, F2, G2, H2	In-phase (+) digital outputs for port B B0 is the LSB, B9 is the MSB

Table 2. Pin Description (Continued)

Symbol	Pin Number	Function
B0N, B1N, B2N, B3N, B4N, B5N, B6N, B7N, B8N, B9N	A5, A4, A3, A2, B1, C1, D1, E1, F1, G1	Inverted phase (-) digital outputs for port B
BOR/DRBN	J2	In-phase (+) additional bit output for port B or inverted phase (-) output clock in staggered mode for port B
BORN/DRB	H1	Inverted phase (-) additional bit output for port B or in-phase (+) output clock in staggered mode for port B
C0, C1, C2, C3, C4, C5, C6, C7, C8, C9	M2, N2, P2, R2, T2, U2, V2, W2, V3, V4	In-phase (+) digital outputs for port C C0 is the LSB, C9 is the MSB
C0N, C1N, C2N, C3N, C4N, C5N, C6N, C7N, C8N, C9N	L1, M1, N1, P1, R1, T1, U1, V1, W3, W4	Inverted phase (-) digital outputs for port C
COR/DRCN	V5	In-phase (+) additional bit output for port C or inverted phase (-) output clock in staggered mode for port C
CORN/DRC	W5	Inverted phase (-) additional bit output for port C or in-phase (+) output clock in staggered mode for port C
D0, D1, D2, D3, D4, D5, D6, D7, D8, D9	V6, V7, V8, V9, V10, V11, V12, V13, V14, V15	In-phase (+) digital outputs for port D D0 is the LSB, D9 is the MSB
D0N, D1N, D2N, D3N, D4N, D5N, D6N, D7N, D8N, D9N	W6, W7, W8, W9, W10, W11, W12, W13, W14, W15	Inverted phase (-) digital outputs for port D
DOR/DRDN	V16	In-phase (+) additional bit output for port D or inverted phase (-) output clock in staggered mode for port D
DORN/DRD	W16	Inverted phase (-) additional bit output for port D or in-phase (+) output clock in staggered mode for port D
DR	J1	In-phase (+) data ready signal output
DRN	K2	Inverted phase (-) data ready signal output
DAO	R18	In-phase (+) output signal for standalone delay cell
DAON	R19	Inverted phase (-) output signal for standalone delay cell
Additional Functions		
ASYNCRST	B17	Asynchronous reset signal
CLKTYPE	V18	Input clock type selection signal
DRTYPE	K1	Output clock type selection signal
CLKDACTRL	V19	Clock delay cell control signal
DACTRL	W18	Standalone delay cell control signal
DAEN	W17	Standalone delay cell enable signal
RS	L2	Ratio selection signal
SLEEP	A18	Sleep mode enable
STAGG	A17	Staggered output mode selection signal
BIST	V17	Built-in self test enable
DIODE	C19	Diode for die junction temperature monitoring

AT84CS001 Pinout

Figure 2. EBGA 240 (Bottom View)



Ordering Information

Part Number	Package	Temperature Range	Screening	Comments
AT84XCS001TP	EBGA 240	Ambient	Prototype	Please contact your local Atmel sales office
AT84CS001VTP	EBGA 240	Industrial grade -40°C < T_C; T_J < 110°C	Standard	
AT84CS001TP-EB	EBGA 240	Ambient	Prototype	Evaluation kit

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