Features

- **22.8 SPECint95 (estimated), 17SPECfp95 at 500 MHz (estimated)**
- **917MIPS at 500 MHz**
- **Selectable Bus Clock (14 CPU Bus Dividers Up To 9x)**
- **Seven Selectable Core-to-L2 Frequency Divisors**
- **Selectable 603 Interface Voltage Below 3.3V (1.8V, 2.5V)**
- **Selectable L2 interface of 1.8V or 2.5V**
- **P_D Typical 5.3W at 500 MHz, Full Operating Conditions**
- **Nap, Doze and Sleep Modes for Power Saving**
- **Superscalar (Four Instructions fetched per Clock Cycle)**
- **4 GB Direct Addressing Range**
- **Virtual Memory: 4 hexabytes (2^{52})**
- **64-bit Data and 32-bit Address Bus Interface**
- **32 KB Instruction and Data Cache**
- **Eight Independent Execution Units and Three Register Files**
- **Write-back and Write-through Operations**
- **f_{INT} Max = 450 MHz 500 MHz**
- **f_{BUS} Max = 133 MHz**

Description

The PC7410 is the second microprocessor that uses the fourth (G4) full implementation of the PowerPC™ Reduced Instruction Set Computer (RISC) architecture. It is fully JTAG-compliant.

The PC7410 maintains some of the characteristics of G3 microprocessors:

- The design is superscalar, capable of issuing three instructions per clock cycle into eight independent execution units
- The microprocessor provides four software controllable power-saving modes and a thermal assist unit management
- The microprocessor has separate 32-Kbyte, physically-addressed instruction and data caches with dedicated L2 cache interface with on-chip L2 tags

In addition, the PC7410 integrates full hardware-based multiprocessing capability, including a 5-state cache coherency protocol (4 MESI states plus a fifth state for shared intervention) and an implementation of the new AltiVec™ technology instruction set.

New features have been developed to make latency equal for double-precision and single-precision floating-point operations involving multiplication. Additionally, in memory subsystem (MSS) bandwidth, the PC7410 offers an optional, high-bandwidth MPX bus interface.

Unlike the PC7400, the PC7410 does not support the 3.3V I/O on the L2 cache interface.

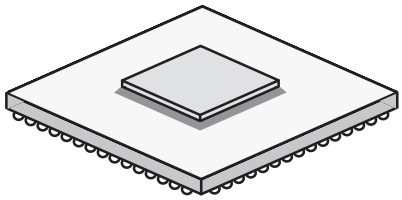
PowerPC 7410 RISC Microprocessor Product Specification

PC7410

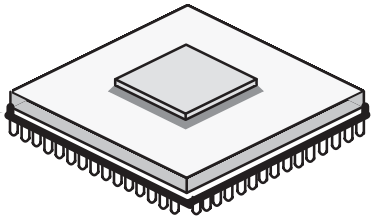
Rev. 2141D–HIREL–02/04

Screening

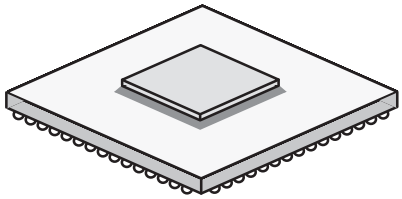
- CBGA Upscreenings Based on Atmel Standards
- Full Military Temperature Range (T_j = -55°C, +125°C), Industrial Temperature Range (T_j = -40°C, +110°C)
- CI-CGA Package Version, HiTCE Package Version



G suffix
CBGA 360
Ceramic Ball Grid Array



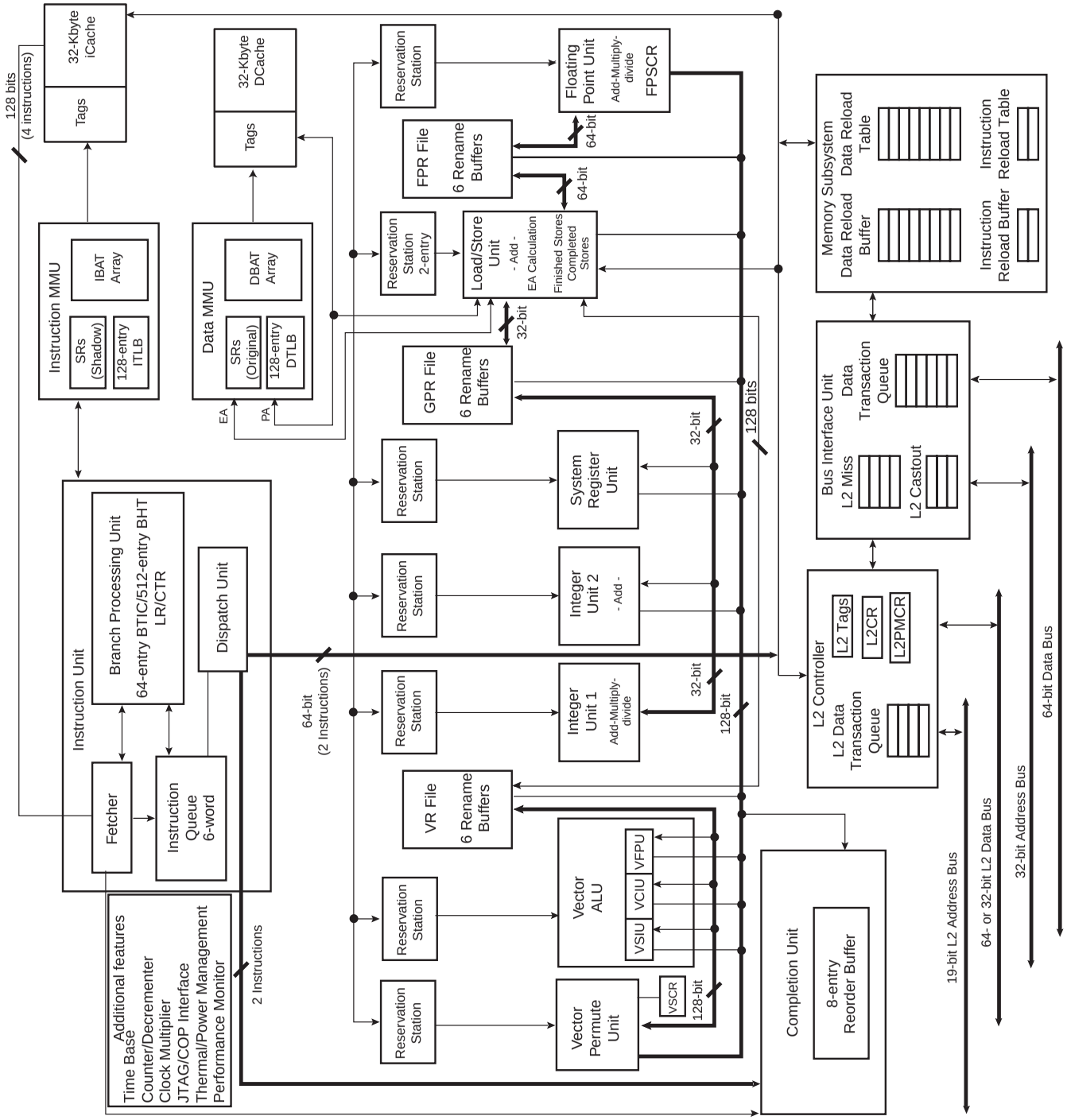
GS suffix
CI±CGA 360
Ceramic Ball Grid Array
with Solder Column Interposer (SCI)



GH suffix
HITCE 360
Ceramic Ball Grid Array

Block Diagram

Figure 1. PC7410 Microprocessor Block Diagram



General Parameters

Table 1 provides a summary of the general parameters of the PC7410.

Table 1. Device Parameters

Parameter	Description
Technology	0.18 µm CMOS, six-layer metal
Die size	6.32 mm × 8.26 mm (52 mm^2)
Transistor count	10.5 million
Logic design	Fully-static
Packages	Surface-mount 360 ceramic ball grid array (CBGA) Surface mount 360 high coefficient of thermal expansion ceramic ball grid array (HiTCE) Surface mount 360-column Ci-CGA Package
Core power supply	1.8V ± 100 mV dc or 1.5V ± 50 mV dc (nominal; see Table 4 for Recommended Operating Conditions)
I/O power supply	1.8V ± 100 mV dc or 2.5V ± 100 mV 3.3V ± 165 mV (603 bus only) (1) (input thresholds are configuration pin selectable) or

Note: 1. 3.3V I/O bus not supported for 1.5V core power supply processor version.

Features

This section summarizes features of the PC7410's implementation of the PowerPC architecture. Major features of the PC7410 are as follows:

- Branch Processing Unit
  - Four instructions fetched per clock
  - One branch processed per cycle (plus resolving two speculations)
  - Up to one speculative stream in execution, one additional speculative stream in fetch
  - 512-entry branch history table (BHT) for dynamic prediction
  - 64-entry, 4-way set associative branch target instruction cache (BTIC) for eliminating branch delay slots
- Dispatch Unit
  - Full hardware detection of dependencies (resolved in the execution units)
  - Dispatch two instructions to eight independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, floating-point, AltiVec permute, AltiVec ALU)
  - Serialization control (predispatch, postdispatch, execution serialization)
- Decode
  - Register file access
  - Forwarding control
  - Partial instruction decode
- Completion
  - 8-entry completion buffer
  - Instruction tracking and peak completion of two instructions per cycle

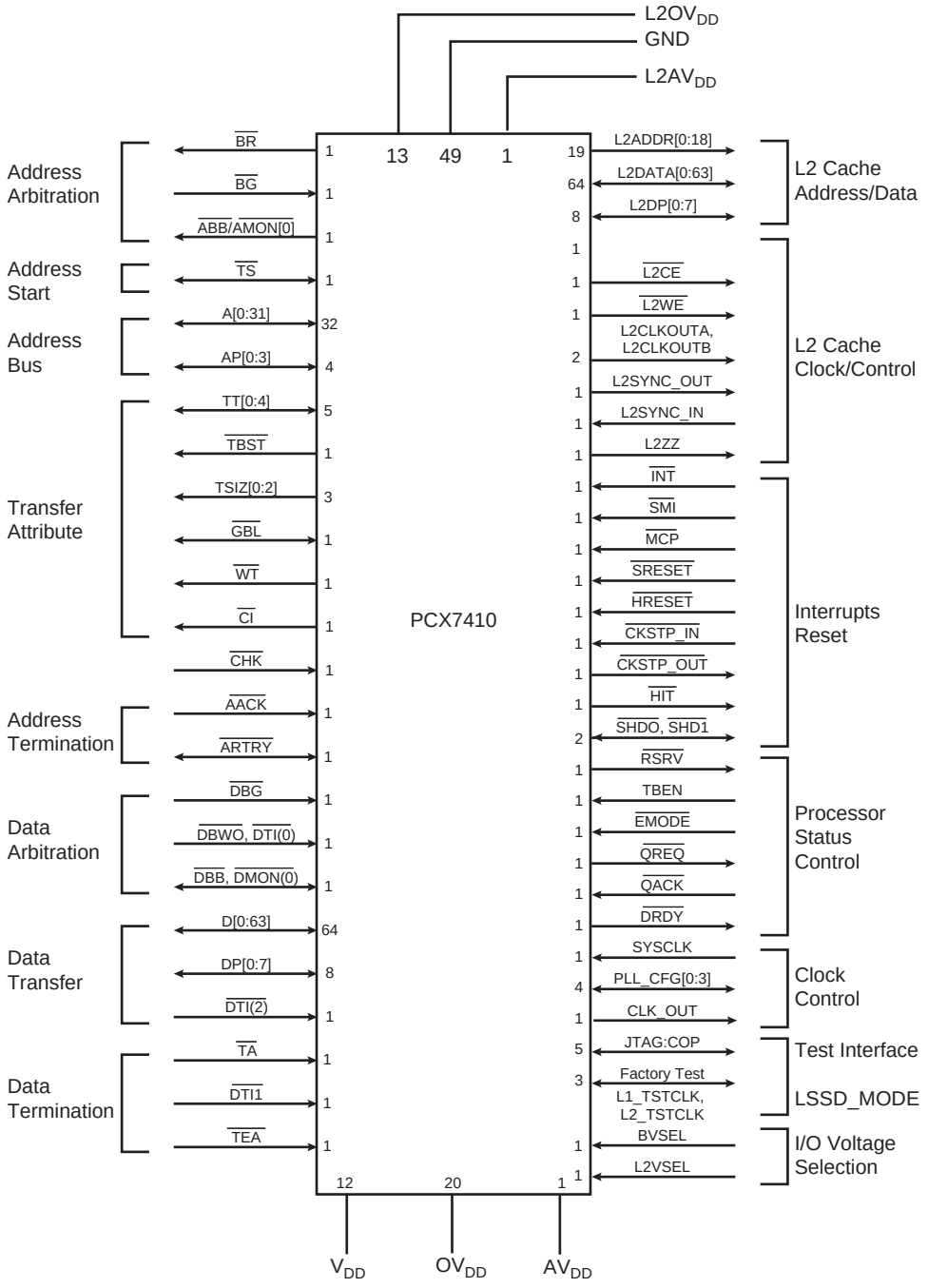
  - Completion of instructions in program order while supporting out-of-order instruction execution, completion serialization and all instruction flow changes
- Fixed-point Units (FXUs) that Share 32 GPRs for Integer Operands
  - Fixed-point unit 1 (FXU1)—multiply, divide, shift, rotate, arithmetic, logical
  - Fixed-point unit 2 (FXU2)—shift, rotate, arithmetic, logical
  - Single-cycle arithmetic, shifts, rotates, logical
  - Multiply and divide support (multi-cycle)
  - Early out multiply
- Three-stage Floating-point Unit and a 32-entry FPR File
  - Support for IEEE-754 standard single- and double-precision floating-point arithmetic
  - Three-cycle latency, one-cycle throughput (single or double precision)
  - Hardware support for divide
  - Hardware support for denormalized numbers
  - Time deterministic non-IEEE mode
- System Unit
  - Executes CR logical instructions and miscellaneous system instructions
  - Special register transfer instructions
- AltiVec Unit
  - Full 128-bit data paths
  - Two dispatchable units: vector permute unit and vector ALU unit
  - Contains its own 32-entry 128-bit vector register file (VRF) with six renames
  - The vector ALU unit is further sub-divided into the vector simple integer unit (VSIU), the vector complex integer unit (VCIU) and the vector floating-point unit (VFPU).
  - Fully pipelined
- Load/Store Unit
  - One-cycle load or store cache access (byte, half-word, word, double-word)
  - Two-cycle load latency with one-cycle throughput
  - Effective address generation
  - Hits under misses (multiple outstanding misses)
  - Single-cycle unaligned access within double-word boundary
  - Alignment, zero padding, sign extend for integer register file
  - Floating-point internal format conversion (alignment, normalization)
  - Sequencing for load/store multiples and string operations
  - Store gathering
  - Executes the cache and TLB instructions
  - Big- and little-endian byte addressing supported
  - Misaligned little-endian supported
  - Supports FXU, FPU, and AltiVec load/store traffic
  - Complete support for all four architecture AltiVec DST streams
- Level 1 (L1) Cache Structure
  - 32K 32-byte line, 8-way set associative instruction cache (iL1)

  - 32K 32-byte line, 8-way set associative data cache (dL1)
  - Single-cycle cache access
  - Pseudo least-recently-used (LRU) replacement
  - Data cache supports AltiVec LRU and transient instructions algorithm
  - Copy-back or write-through data cache (on a page-per-page basis)
  - Supports all PowerPC memory coherency modes
  - Non-blocking instruction and data cache
  - Separate copy of data cache tags for efficient snooping
  - No snooping of instruction cache except for ICBI instruction
- Level 2 (L2) Cache Interface
  - Internal L2 cache controller and tags; external data SRAMs
  - 512K, 1M and 2-Mbyte 2-way set associative L2 cache support
  - Copyback or write-through data cache (on a page basis or for all L2)
  - 32-byte (512K), 64-byte (1M), or 128-byte (2M) sectored line size
  - Supports pipelined (register-register) synchronous burst SRAMs and pipelined (register-register) late-write synchronous burst SRAMs
  - Supports direct mapped mode for 256K, 512K, 1M or 2 Mbytes of SRAM (either all, half or none of L2 SRAM must be configured as direct mapped.
  - Core-to-L2 frequency divisors of ÷1, ÷1.5, ÷2, ÷2.5, ÷3, ÷3.5, and ÷4 supported
  - 64-bit data bus which also support 32-bits bus mode
  - Selectable interface voltages of 1.8V and 2.5V
- Memory Management Unit
  - 128 entry, 2-way set associative instruction TLB
  - 128 entry, 2-way set associative data TLB
  - Hardware reload for TLBs
  - Four instruction BATs and four data BATs
  - Virtual memory support for up to four petabytes (2^{52}) of virtual memory
  - Real memory support for up to four gigabytes (2^{32}) of physical memory
  - Snooped and invalidated for TLBI instructions
- Efficient Data Flow
  - All data buses between VRF, load/store unit, dL1, iL1, L2 and the bus are 128 bits wide
  - dL1 is fully pipelined to provide 128 bits per cycle to/from the VRF
  - L2 is fully pipelined to provide 128 bits per L2 clock cycle to the L1s
  - Up to eight outstanding out-of-order cache misses between dL1 and L2/bus
  - Up to seven outstanding out-of-order transactions on the bus
  - Load folding to fold new dL1 misses into older outstanding load and store misses to the same line
  - Store miss merging for multiple store misses to the same line. Only coherency action taken (i.e., address only) for store misses merged to all 32 bytes of a cache line (no data tenure needed).
  - Two-entry finished store queue and four-entry completed store queue between load/store unit and dL1

  - Separate additional queues for efficient buffering of outbound data (castouts, write throughs, etc.) from dL1 and L2
- Bus Interface
  - MPX bus extension to 60X processor interface
  - Mode-compatible with 60x processor interface
  - 32-bit address bus
  - 64-bit data bus
  - Bus-to-core frequency multipliers of 2x, 2.5x, 3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x, 7.5x, 8x, 9x supported
  - Selectable interface voltages of 1.8V, 2.5V and 3.3V
- Power Management
  - Low-power design with thermal requirements very similar to PC740 and PC750
  - Low voltage 1.8V or 1.5V processor core
  - Selectable interface voltages of 1.8V can reduce power in output buffers
  - Three static power saving modes: doze, nap, and sleep
  - Dynamic power management
- Testability
  - LSSD scan design
  - IEEE 1149.1 JTAG interface
  - Array built-in self test (ABIST) – factory test only
  - Redundancy on L1 data arrays and L2 tag arrays
- Reliability and Serviceability
  - Parity checking on 60x and L2 cache buses

Signal Description

Figure 2. PC7410 Microprocessor Signal Groups



Detailed Specification

Scope

This drawing describes the specific requirements for the microprocessor PC7410 in compliance with Atmel-Grenoble standard screening.

Applicable Documents

1. MIL-STD-883: Test methods and procedures for electronics
2. MIL-PRF-38535: Appendix A: General specifications for microcircuits

Requirements

General

The microcircuits are in accordance with the applicable documents and as specified herein.

Design and Construction

Terminal Connections

Depending on the package, the terminal connections are as shown in Table 16, Table 4 and Figure 2.

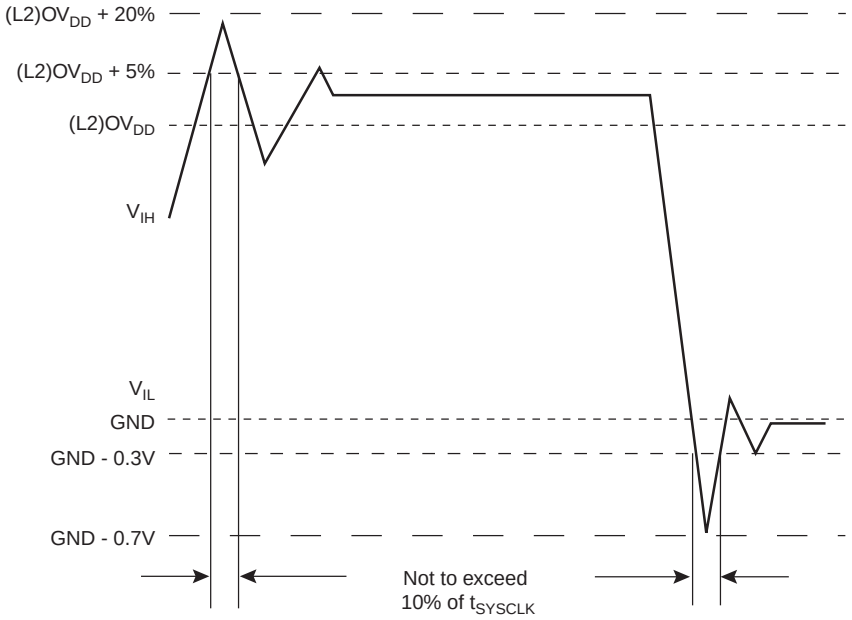
Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings(1)

Symbol	Characteristic	Value	Unit
V_{DD}	Core supply voltage	-0.3 to 2.1(4)	V
AV_{DD}	PLL supply voltage	-0.3 to 2.1(4)	V
$L2AV_{DD}$	L2 DLL supply voltage	-0.3 to 2.1(4)	V
OV_{DD}	60x bus supply voltage	-0.3 to 3.465(3)(6)	V
$L2OV_{DD}$	L2 bus supply voltage	-0.3 to 2.6(3)	V
V_{IN}	Processor bus input voltage	-0.3 to OVDD + 0,2V(2)(5)	V
V_{IN}	L2 bus input voltage	-0.3 to L2OVDD + 0,2V(2)(5)	V
V_{IN}	JTAG signal input voltage	-0.3 to OVDD + 0,2V	V
T_{STG}	Storage temperature range	-55 to 150	°C
	Rework temperature	260	°C

Notes:
1. Functional and tested operating conditions are given in Table 4. Absolute maximum ratings are stress ratings only. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. Caution: V_{IN} must not exceed OV_{DD} or $L2OV_{DD}$ by more than 0.2V at any time including during power-on reset.
3. Caution: $L2OV_{DD}/OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by more than 2.0V at any time including during power-on reset; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. Caution: $V_{DD}/AV_{DD}/L2AV_{DD}$ must not exceed $L2OV_{DD}/OV_{DD}$ by more than 0.4V at any time including during power-on reset; this limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. V_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 3.
6. PC7410RXnnnLE (Rev 1.4) and later only. Previous revisions do not support 3.3V OV_{DD} and have a maximum value OV_{DD} of -0.3 to 2.6V.

Figure 3. Overshoot/Undershoot Voltage



The PC7410 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The PC7410 “core” voltage must always be provided at nominal voltage (see Table 4 for actual recommended core voltage). Voltage to the L2 I/Os and processor interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in Table 3. The input voltage threshold for each bus is selected by sampling the state of the voltage select pins at the negation of the signal $\overline{\text{HRESET}}$. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} or $L2OV_{DD}$ power pins.

Table 3. Input Threshold Voltage Setting

BVSEL Signal	Processor Bus Input Threshold is Relative to:	L2VSEL Signal(3)	L2 Bus Input Threshold is Relative to:
0(1)	1.8V	0	1.8
$\overline{\text{HRESET}}$(1)(2)	2.5V	$\overline{\text{HRESET}}$	2.5
1(1)(4)(5)	3.3V(7)	1	2.5
HRESET(6)	3.3V(7)	HRESET	Not supported

Notes:
1. Caution: The input threshold selection must agree with the OV_{DD}/$L2OV_{DD}$ voltages supplied.
2. To select the 2.5V threshold option, L2VSEL/BVSEL should be tied to $\overline{\text{HRESET}}$ so that the two signals change state together. This is the preferred method for selecting this mode operation.
3. To overcome the internal pull-up resistance, a pull-down resistance less than 250Ω should be used.
4. Default voltage setting if left unconnected (internal pulled-up). Parts Rev 1.4 and later only. Previous revisions do not support 3.3V OV_{DD}, the default voltage setting if left unconnected is 2.5V.
5. Parts Rev 1.4 and later only. Previous revisions do not support 3.3V OV_{DD}, having BVSEL = 1 selects the 2.5V threshold.
6. Parts Rev 1.4 and later only. Previous revisions do not support BVSEL = HRESET.
7. NSpec does not support the default OV_{DD} setting of 3.3V. The BVSEL input must be tie either low or $\overline{\text{HRESET}}$.

Recommended Operating Conditions

Table 4. Recommended Operating Conditions[1]

Symbol	Characteristic		Recommended Value	Unit
V_{DD}	Core supply voltage		1.8 ± 100 mV or 1.5 ± 50 mV	V
AV_{DD}	PLL supply voltage		1.8 ± 100 mV or 1.5 ± 50 mV	V
$L2AV_{DD}$	L2 DLL supply voltage		1.8 ± 100 mV or 1.5 ± 50 mV	V
OV_{DD}	Processor bus supply voltage see note [3]	BVSEL = 0	1.8 ± 100 mV	V
OV_{DD}		BVSEL = $\overline{\text{HRESET}}$	2.5 ± 100 mV	V
OV_{DD}[2][3]		BVSEL = 1 or = HRESET[4]	3.3 ± 165 mV	V
$L2OV_{DD}$	L2 bus supply voltage	L2VSEL = 0	1.8 ± 100 mV	V
$L2OV_{DD}$		L2VSEL = 1[2] or L2VSEL = HRESET	2.5 ± 100 mV	V
V_{IN}	Input voltage	Processor bus	GND to OV_{DD}	V
V_{IN}		L2 Bus	GND to $L2OV_{DD}$	V
V_{IN}		JTAG Signals	GND to OV_{DD}	V
T_j	Die-junction temperature		-55 to 125	°C

Notes:
1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. PC7410RXnnnLE (Rev 1.4) and later only. Previous revisions do not support 3.3V OV_{DD} and have a recommended OV_{DD} value of 2.5V ±100 mV for BVSEL = 1.
3. PC7410RXnnnLE (Rev 1.4) and later only. Previous revisions do not support BVSEL = HRESET.
4. Not supported for N spec with V_{DD} = 1.5V

Thermal Characteristics

Package Characteristics

Table 5. Package Thermal Characteristics CBGA

Symbol	Characteristic	Value PC7410 CBGA	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance, natural convection, single-layer (1s) board(1)(2)	24	°C/W
$R_{\theta JMA}$	Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board(1)(3)	17	°C/W
$R_{\theta JMA}$	Junction-to-ambient thermal resistance, 200 ft/min airflow, single-layer (1s) board(1)(3)	18	°C/W
$R_{\theta JMA}$	Junction-to-ambient thermal resistance, 400 ft/min airflow, single-layer (1s) board	16	°C/W
$R_{\theta JMA}$	Junction-to-ambient thermal resistance, 200 ft/min airflow, four-layer (2s2p) board(1)(3)	14	°C/W
$R_{\theta JMA}$	Junction-to-ambient thermal resistance, 400 ft/min airflow, four-layer (2s2p) board	13	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance(4)	8	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance(5)	< 0.1	°C/W

Notes:
1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. The actual value of $R_{\theta JC}$ for the part is less than 0.1°C/W.

See “Thermal Management Information” on page 13 for more details about thermal management.

The board designer can choose between several commercially available heat sink types to place on the PC7410. For exposed-die packaging technology as in Table 5, the intrinsic conduction thermal resistance paths are shown in Figure 4.

Package Thermal Characteristics for HiTCE

Table 6 provides the package thermal characteristics for the PC7410, HiTCE.

Table 6. Package Thermal Characteristics for HiTCE Package

Characteristic	Symbol	Value PC7410 HiTCE	Unit
Junction-to-bottom of balls(1)	$R\theta_J$	6.8	°C/W
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board(1)(2)	$R\theta_{JMA}$	20.7	°C/W
Junction to board thermal resistance	$R\theta_{JB}$	11.0	°C/W

Notes:
1. Simulation, no convection air flow.
2. Per JEDEC JESD51-6 with the board horizontal.

Package Thermal Characteristics for CI-CGA

Table 7. Package Thermal Characteristics for CI-CGA

Characteristic	Symbol	Value PC7410 CI-CGA	Unit
Junction to board thermal resistance	$R\theta_{JB}$	8.42	°C/W

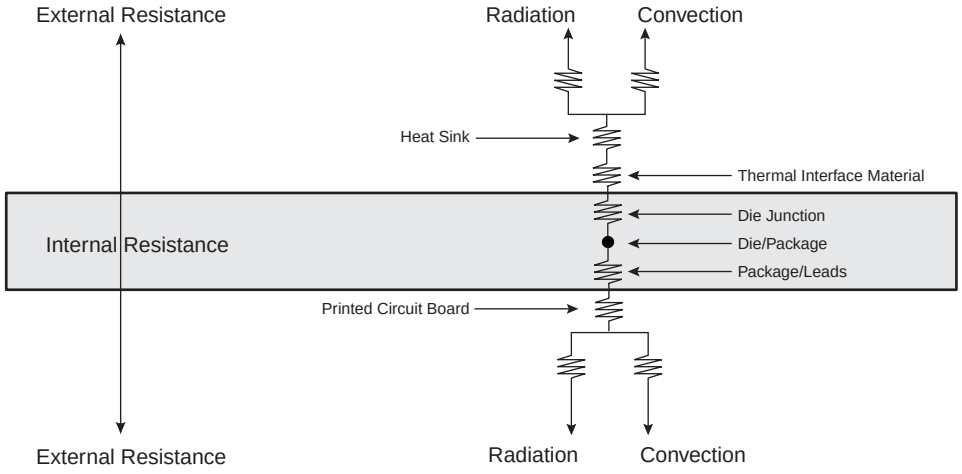
Internal Package Conduction Resistance

Figure 4 depicts the primary heat transfer path for a package with an attached heat sink mounted on a printed circuit board.

Heat generated on the active side of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material) and finally to the heat sink where it is removed by forced-air convection.

Since the silicon thermal resistance is quite small, for a first-order analysis the temperature drop in the silicon may be neglected. Thus, the heat sink attach material and the heat sink conduction/convective thermal resistances are the dominant terms.

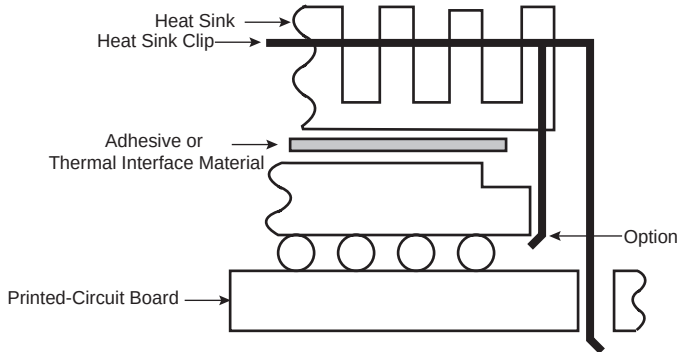
Figure 4. C4 Package with Heat Sink Mounted on a Printed Circuit Board



Thermal Management Information

This section provides thermal management information for the ceramic ball grid array (CBGA) package for air-cooled applications. Proper thermal control design is primarily dependent upon the system-level design – the heat sink, airflow and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods: adhesive, spring clip to holes in the printed-circuit board or package and mounting clip and screw assembly; see Figure 5. This spring force should not exceed 5.5 pounds of force. Ultimately, the final selection of an appropriate heat sink depends on many factors such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly and cost.

Figure 5. CBGA Package Cross-section with Heat Sink Options



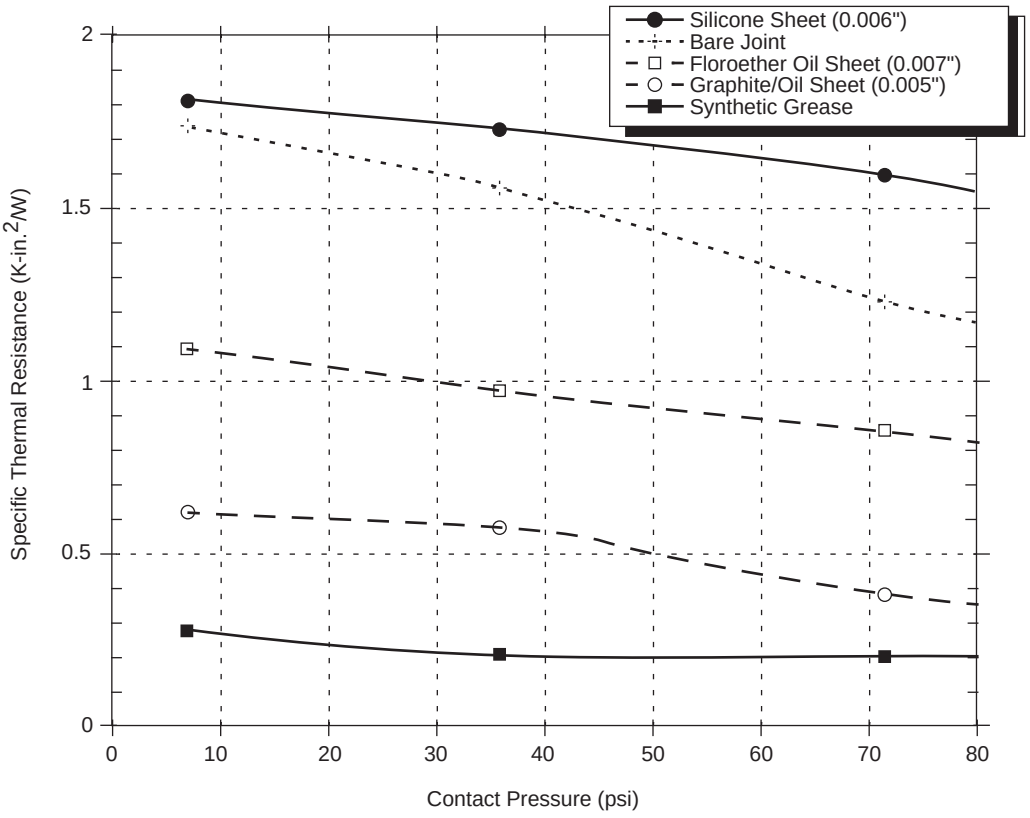
Adhesives and Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 6 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 5). This spring force should not exceed 5.5 pounds of force. Therefore, synthetic grease offers the best thermal performance, considering the low interface pressure.

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based upon high conductivity, yet must have adequate mechanical strength to meet equipment shock/vibration requirements.

Figure 6. Thermal Performance of Different Thermal Interface Materials



Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_a + T_r + (\theta_{jc} + \theta_{int} + \theta_{sa}) \times P_d$$

where:

T_j = die-junction temperature

T_a = inlet cabinet ambient temperature

T_r = air temperature rise within the computer cabinet

θ_{jc} = junction-to-case thermal resistance

θ_{int} = adhesive or interface material thermal resistance

θ_{sa} = heat sink base-to-ambient thermal resistance

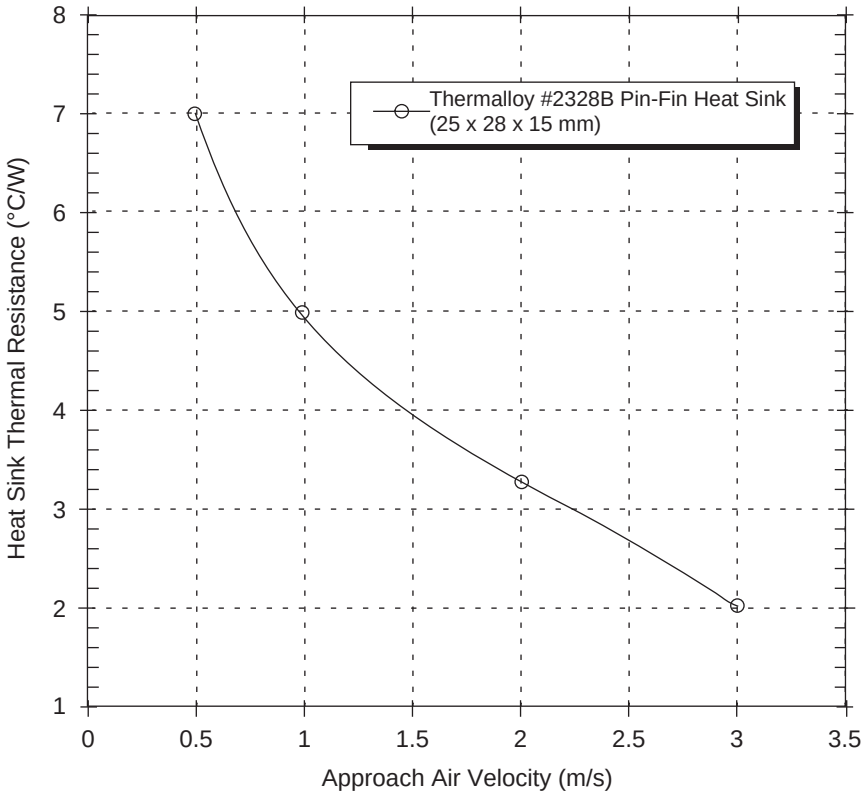
P_d = power dissipated by the device

During operation, the die-junction temperatures (T_j) should be maintained less than the value specified in Table 4. The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_a) may range from 30°C to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5°C to 10°C. The thermal resistance of the thermal interface material (θ_{int}) is typically about 1°C/W. Assuming a T_a of 30°C, a T_r of 5°C, a CBGA package θ_{jc} = 0.03, and a power consumption (P_d) of 5.0 watts, the following expression for T_j is obtained:

$$T_j = 30°C + 5°C + (0{,}03°C/W + 1{,}0°C/W + \theta_{sa}) \times 5W$$

For a Thermally heat sink #2328B, the heat sink-to-ambient thermal resistance (θ_{sa}) versus airflow velocity is shown in Figure 7.

Figure 7. Thermalloy #2328B Heat Sink-to-ambient Thermal Resistance vs. Airflow Velocity



Assuming an air velocity of 0.5 m/s, the effective R_{sa} is 7°C/W, thus

$$T_j = 30°C + 5°C + (0{,}03°C/W + 1{,}0°C/W + 7°C/W) \times 5W,$$

resulting in a die-junction temperature of approximately 75°C which is well within the maximum operating temperature of the component.

Other heat sinks offered by Chip Coolers, IERC, Thermalloy, Wakefield Engineering and Aavid Engineering offer different heat sink-to-ambient thermal resistances and may or may not need air flow.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure of merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but of the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature – airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection and conduction) may vary widely. For these reasons, it is recommended to use conjugate heat transfer models for the board, as well as system-level designs.

To expedite system-level thermal analysis, several “compact” thermal-package models are available within FLOTHERM®. These are available upon request.

Power Consideration

Power Management

The PC7410 provides four power modes, selectable by setting the appropriate control bits in the MSR and HIDO registers. The four power modes are:

- Full-power: This is the default power state of the PC7410. The PC7410 is fully powered and the internal functional units are operating at the full processor clock speed. If the dynamic power management mode is enabled, functional units that are idle will automatically enter a low-power state without affecting performance, software execution or external hardware.
- Doze: All the functional units of the PC7410 are disabled except for the time base/decrementer registers and the bus snooping logic. When the processor is in doze mode, an external asynchronous interrupt, a system management interrupt, a decrementer exception, a hard or soft reset or machine check brings the PC7410 into the full-power state. The PC7410 in doze mode maintains the PLL in a fully powered state and locked to the system external clock input (SYSCLK) so a transition to the full-power state takes only a few processor clock cycles.
- Nap: The nap mode further reduces power consumption by disabling bus snooping, leaving only the time base register and the PLL in a powered state. The PC7410 returns to the full-power state upon receipt of an external asynchronous interrupt, a system management interrupt, a decrementer exception, a hard or soft reset or a machine check input ($\overline{\text{MCP}}$). A return to full-power state from a nap state takes only a few processor clock cycles. When the processor is in nap mode, if $\overline{\text{QACK}}$ is negated, the processor is put in doze mode to support snooping.
- Sleep: Sleep mode minimizes power consumption by disabling all internal functional units, after which external system logic may disable the PLL and SYSCLK. Returning the PC7410 to the full-power state requires the enabling of the PLL and SYSCLK, followed by the assertion of an external asynchronous interrupt, a system management interrupt, a hard or soft reset or a machine check input ($\overline{\text{MCP}}$) signal after the time required to relock the PLL.

Power Dissipation

Table 8. Power Consumption for PC7410 (1.8V)

	Processor (CPU) Frequency					Unit
Power Mode	**400 MHz**		**450 MHz**		**500 MHz**	
Core power supply	**1.5V**	**1.8V**	**1.5V**	**1.8V**	**1.8 V**	
Full-On Mode						
Typical(1)(3)	2.92	4.2	3.29	4.7	5.3	W
Maximum(1)(2)(4)(5)	6.6	9.5	7.43	10.7	11.9	W
Doze Mode						
Maximum(1)(2)(5)	3.6	4.3	4.1	4.8	5.3	W
Nap Mode						
Maximum(1)(2)(5)	1.35	1.35	1.5	1.5	1.65	W
Sleep Mode						
Maximum(1)(2)(5)	1.3	1.3	1.45	1.45	1.6	W
Sleep Mode - PLL and DLL Disabled						
Typical(1)(3)	600	600	600	600	600	mW
Maximum(1)(2)(5)	1.1	1.1	1.1	1.1	1.1	W

Notes:
1. These values apply for all valid processor bus and L2 bus ratios. The values do not include I/O supply power (OV_{DD} and $L2OV_{DD}$) or PLL/DLL supply power (AV_{DD} and $L2AV_{DD}$). OV_{DD} and $L2OV_{DD}$ power is system dependent, but is typically <10% of V_{DD} power. Worst case power consumption for AV_{DD} = 15 mW and $L2AV_{DD}$ = 15 mW.
2. Maximum power is measured at 105°C, at V_{DD} = 1.8V or 1.5Vwhile running an entirely cache-resident, contrived sequence of instructions which keep the execution units, including AltiVec, maximally busy.
3. Typical power is an average value measured at 65°C, V_{DD} = 1.8V or 1.5V, OV_{DD} = $L2OV_{DD}$ = 2.5V in a system while running a codec application that is AltiVec intensive.
4. These values include the use of AltiVec. Without AltiVec operation, estimate a 25% decrease.
5. Power consumption derating at low temperatures to be defined after device characterization.

Electrical Characteristics

Static Characteristics

Table 9. DC Electrical Specifications (see Table 4 for Recommended Operating Conditions)

Symbol	Characteristic	Nominal Bus Voltage[1]	Min	Max	Unit
V_{IH}	Input high voltage (all inputs except SYSCLK)[2][3][8]	1.8	0.65 x (L2)OV_{DD}	(L2)OV_{DD} + 0.2	V
V_{IH}		2.5	1.7	(L2)OV_{DD} + 0.2	
V_{IH}		3.3	2.0	OV_{DD} + 0.3	
V_{IL}	Input low voltage (all inputs except SYSCLK)[8]	1.8	-0.3	0.35 x (L2)OV_{DD}	V
V_{IL}		2.5	-0.3	0.2 x (L2)OV_{DD}	
V_{IL}		3.3	-0.3	0.8	
CV_{IH}	SYSCLK input high voltage[2][8]	1.8	1.5	OV_{DD} + 0.2	V
CV_{IH}		2.5	2.0	OV_{DD} + 0.2	
CV_{IH}		3.3	2.4	OV_{DD} + 0.3	
CV_{IL}	SYSCLK input low voltage[8]	1.8	-0.3	0.2	V
CV_{IL}		2.5	-0.3	0.4	
CV_{IL}		3.3	-0.3	0.4	
I_{IN}	Input leakage current, V_{IN} = L2OV_{DD}/OV_{DD}[2][3][6][7]	1.8	–	20	µA
I_{IN}		2.5	–	35	
I_{IN}		3.3	–	70	
I_{TSI}	High-Z (off-state) leakage current, V_{IN} = L2OV_{DD}/OV_{DD}[2][3][5][7]	1.8	–	20	µA
I_{TSI}		2.5	–	35	
I_{TSI}		3.3	–	70	
V_{OH}	Output high voltage, I_{OH} = -6 mA[8]	1.8	(L2)OV_{DD} - 0.45	–	V
V_{OH}		2.5	1.7	–	
V_{OH}		3.3	2.4	–	
V_{OL}	Output low voltage, I_{OL} = 6 mA[8]	1.8	–	0.45	V
V_{OL}		2.5	–	0.4	
V_{OL}		3.3	–	0.4	
C_{IN}	Capacitance, V_{IN} = 0V, f = 1 MHz[3][4][7]		–	6.0	pF

Notes:
1. Nominal voltages; see Table 4 for recommended operating conditions.
2. For processor bus signals, the reference is OV_{DD} while L2OV_{DD} is the reference for the L2 bus signals.
3. Excludes factory test signals.
4. Capacitance is periodically sampled rather than 100% tested.
5. The leakage is measured for nominal OV_{DD} and L2OV_{DD}, or both OV_{DD} and L2OV_{DD} must vary in the same direction (for example, both OV_{DD} and L2OV_{DD} vary by either +5% or –5%).
6. Measured at max OV_{DD}/L2OV_{DD}
7. Excludes IEEE 1149.1 boundary scan (JTAG) signals.

8. For JTAG support: all signals controlled by BVSEL and L2VSEL will see $V_{IL}/V_{IH}/V_{OL}/V_{OH}/CV_{IH}/CV_{IL}$ DC limits of 1.8V mode while either the EXTEST or CLAMP instruction is loaded into the IEEE 1149.1 instruction register by the UpdateIR TAP state until a different instruction is loaded into the instruction register by either another UpdateIR or a Test-Logic-Reset TAP state. If only $\overline{\text{TSRT}}$ is asserted to the part, and then a SAMPLE instruction is executed, there is no way to control or predict what the DC voltage limits are. If $\overline{\text{HRESET}}$ is asserted before executing a SAMPLE instruction, the DC voltage limits will be controlled by the BVSEL/L2VSEL settings during $\overline{\text{HRESET}}$. Anytime $\overline{\text{HRESET}}$ is not asserted (i.e., just asserting $\overline{\text{TRST}}$), the voltage mode is not known until either EXTEST or CLAMP is executed, at which time the voltage level will be at the DC limits of 1.8V.

Dynamic Characteristics

After fabrication, parts are sorted by maximum processor core frequency as shown in "Clock AC Specifications" and tested for conformance to the AC specifications for that frequency. These specifications are for valid processor core frequencies. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0:3] signals. Parts are sold by maximum processor core frequency.

Clock AC Specifications

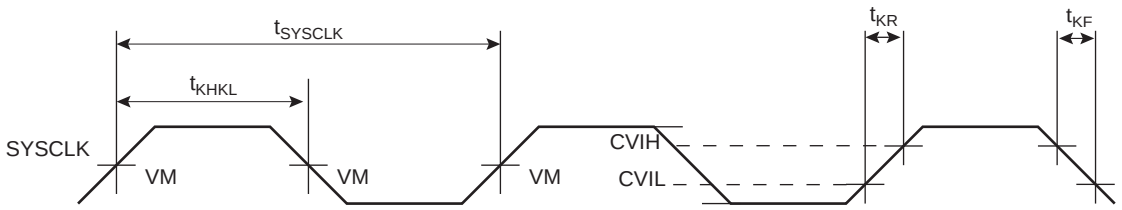
Table 10 provides the clock AC timing specifications as defined in Figure 8.

Table 10. Clock AC Timing Specifications (See Table 4 for Recommended Operating Conditions)

		Maximum Processor Core Frequency						
		400 MHz		450 MHz		500 MHz		
Symbol	**Characteristic**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{CORE}(1)	Processor frequency	350	400	350	450	350	500	MHz
f_{VCO}(1)	VCO frequency	700	800	700	900	700	1000	MHz
f_{SYSCLK}(1)	SYSCLK frequency	33	133	33	133	33	133	MHz
t_{SYSCLK}	SYSCLK cycle time	7.5	30	7.5	30	7.5	30	ns
t_{KR} & t_{KF}(2)	SYSCLK rise and fall time		1.0		1.0		1	ns
t_{KR} & t_{KF}(3)			0.5		0.5		0.5	ns
t_{KHKL}/t_{SYSCLK}(4)	SYSCLK duty cycle measured at $OV_{DD}/2$	40	60	40	60	40	60	%
	SYSCLK jitter(5)		±150		±150		±150	ps
	Internal PLL relock time(6)		100		100		100	µs

Notes:
1. Caution: The SYSCLK frequency and PLL_CFG[0:3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:3] signal description in "Clock Selection" on page 39 for valid PLL_CFG[0:3] settings
2. Rise and fall times for the SYSCLK input measured from 0.4V to 2.4V when OV_{DD} = 3.3V nominal.
3. Rise and fall times for the SYSCLK input measured from 0.2V to 1.2V when OV_{DD} = 1.8V or 2.5V nominal.
4. Timing is guaranteed by design and characterization.
5. This represents total input jitter, short-term and long-term combined, and is guaranteed by design.
6. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

Figure 8. SYSCLK Input Timing Diagram



Note: VM = Midpoint Voltage (OV_{DD}/2)

Processor Bus AC Specifications

Table 11 provides the processor AC timing specifications for the PC7410 as defined in Figure 10 and Figure 11. Timing specifications for the L2 bus are provided in "L2 Bus AC Specifications" on page 26.

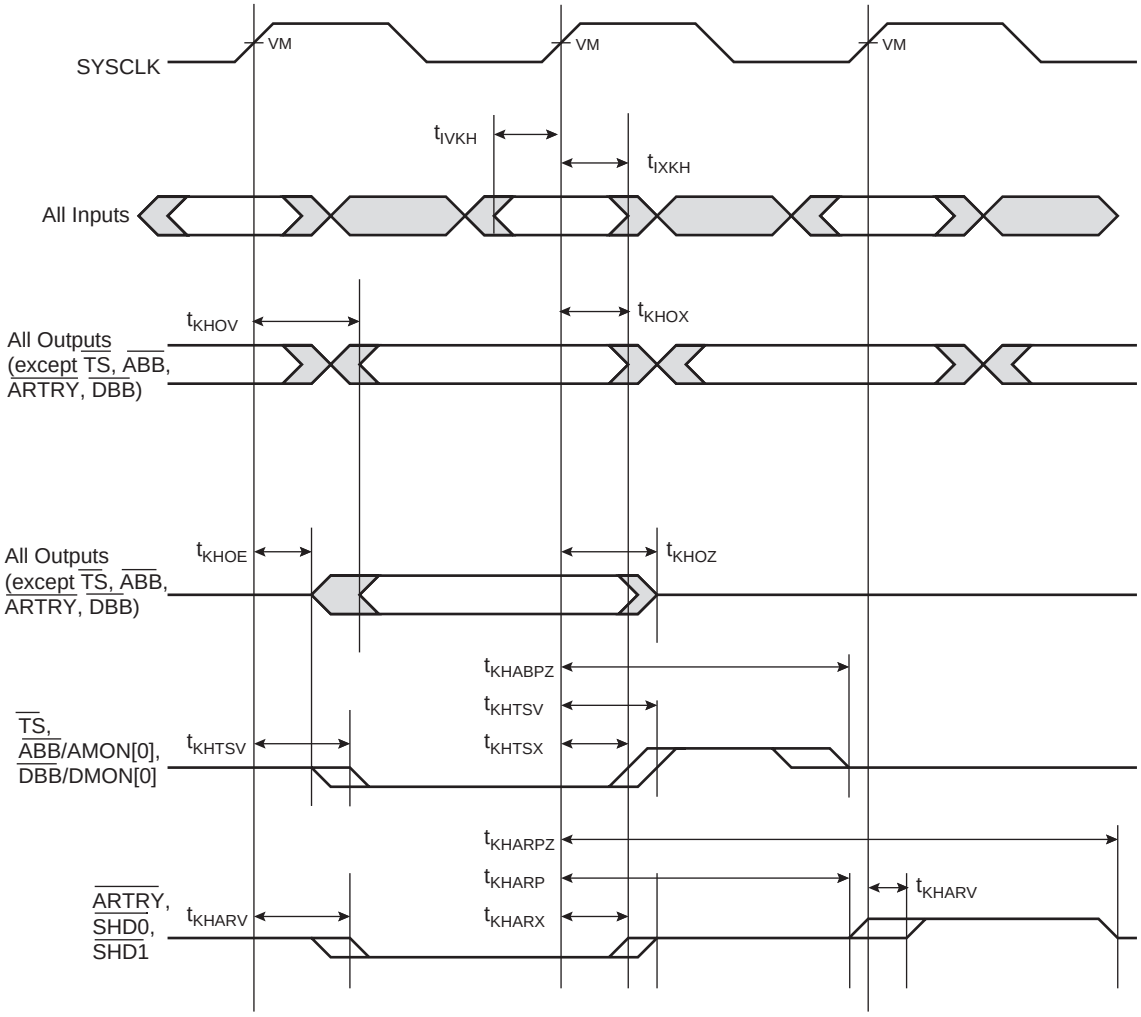
Table 11. Processor Bus AC Timing Specifications[1] at $V_{DD} = AV_{DD} = 1.8V \pm 100$ mV; $-55°C \le T_j \le 125°C$, $OV_{DD} = 1.8V \pm 100$ mV

Symbol[2]	Parameter	400, 450, 500 MHz		Unit
		Min	Max	
t_{IVKH}	Input Setup	1.0	–	ns
t_{IXKH}	Input Hold	0	–	ns
	Output Valid Times:[7][8]			ns
t_{KHTSV}	TS	–	3.0	
t_{KHARV}	$\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$	–	2.3	
t_{KHOV}	All Other Outputs	–	3.0	
	Output Hold Times:[7][12]			ns
t_{KHTSX}	TS	0.5	–	
t_{KHARX}	$\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$	0.5	–	
t_{KHOX}	All Other Outputs	0.5	–	
t_{KHOE}[11]	SYSCLK to Output Enable	0.5	–	ns
t_{KHOZ}	SYSCLK to Output High Impedance (all except $\overline{ABB}$/$\overline{AMON}$[0], $\overline{ARTRY}$/$\overline{SHD}$, $\overline{DBB}$/$\overline{DMON}$[0]), $\overline{SHD0}$, $\overline{SHD1}$)	–	3.5	ns
t_{KHABPZ}[5][9][11]	SYSCLK to $\overline{ABB}$/$\overline{AMON}$[0], $\overline{DBB}$/$\overline{DMON}$[0] High Impedance after precharge	–	1	t_{SYSCLK}
t_{KHARP}[5][10][11]	Maximum Delay to $\overline{ARTRY}$/$\overline{SHD0}$/$\overline{SHD1}$ Precharge	–	1	t_{SYSCLK}

Notes:
1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50Ω load (see Figure 10). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{(signal)(state)(reference)(state)}$ for inputs and $t_{(reference)(state)(signal)(state)}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK (K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) - note the position of the reference and its state for inputs -and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. The setup and hold time is with respect to the rising edge of $\overline{HRESET}$ (see Figure 11).
4. This specification is for configuration mode select only. Also note that the $\overline{HRESET}$ must be held asserted for a minimum of 255 bus clocks after the PLL re-lock time during the power-on reset sequence.
5. t_{SYSCLK} is the period of the external clock (SYSCLK) in nanoseconds(ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
6. Mode select signals are BVSEL, EMODE, L2VSEL, PLL_CFG[0:3]

7. All other output signals are composed of the following - A[0:31], AP[0:3], TT[0:4], $\overline{\text{TBST}}$, TSIZ[0:2], $\overline{\text{GBL}}$, $\overline{\text{WT}}$, $\overline{\text{CI}}$, DH[0:31], DL[0:31], DP[0:7], $\overline{\text{BR}}$, $\overline{\text{CKSTP\_OUT}}$, $\overline{\text{DRDY}}$, $\overline{\text{HIT}}$, $\overline{\text{QREQ}}$, $\overline{\text{RSRV}}$.
8. Output valid time is measured from 2.4V to 0.8V which may be longer than the time required to discharge from Vdd to 0.8V.
9. According to the 60x bus protocol, $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ are driven only by the currently active bus master. They are asserted low then precharged high before returning to high-Z as shown in Figure 9. The nominal precharge width for $\overline{\text{ABB}}$ or $\overline{\text{DBB}}$ is 0.5 x t_{SYSCLK}, i.e., less than the minimum t_{SYSCLK} period, to ensure that another master asserting $\overline{\text{ABB}}$, or $\overline{\text{DBB}}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge.The high-Z behavior is guaranteed by design.
10. According to the 60x bus protocol, $\overline{\text{ARTRY}}$ can be driven by multiple bus masters through the clock period immediately following $\overline{\text{AACK}}$. Bus contention is not an issue since any master asserting $\overline{\text{ARTRY}}$ will be driving it low. Any master asserting it low in the first clock following $\overline{\text{AACK}}$ will then go to high-Z for one clock before precharging it high during the second cycle after the assertion of $\overline{\text{AACK}}$. The nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 t_{SYSCLK} ; i.e., it should be high-Z as shown in Figure 9 before the first opportunity for another master to assert $\overline{\text{ARTRY}}$. Output valid and output hold timing are tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
11. Guaranteed by design and not tested.
12. Output hold time characteristics can be altered by the use of the L2_TSTCK pin during system reset, similar to L2 output hold being altered by the use of bits [14-15] in the L2CR register. Information on the operation of the L2_TSTCLK will be included in future revisions of this specification.

Figure 9. Input/Output Timing Diagram



VM = Midpont Voltage (OV_{DD}/2)

Figure 10. AC Test Load for the 60x Interface

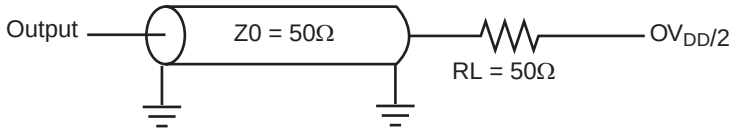
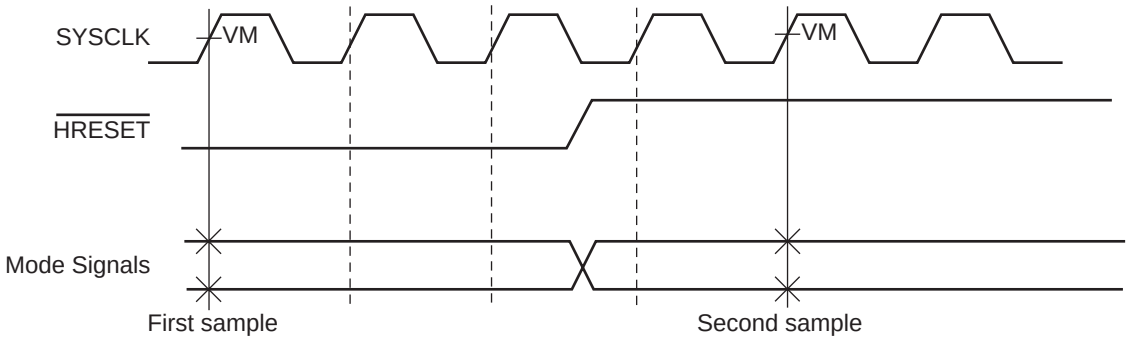


Figure 11 provides the mode select input timing diagram for the PC7410. The mode select inputs are sampled twice, once before and once after $\overline{\text{HRESET}}$ negation.

Figure 11. Mode Input Timing Diagram



where VM = Midpoint Voltage ($OV_{DD}/2$)

L2 Clock AC Specifications

The L2CLK frequency is programmed by the L2 configuration register (L2CR[4:6]) core-to-L2 divisor ratio. See Table 18 for example core and L2 frequencies at various divisors. Table 12 provides the potential range of L2CLK output AC timing specifications as defined in Figure 12.

The L2SYNC_OUT signal is intended to be routed halfway out to the SRAMs and then returned to the L2SYNC_IN input of the PC7410 to synchronize L2CLKOUT at the SRAM with the processor's internal clock. L2CLKOUT at the SRAM can be offset forward or backward in time by shortening or lengthening the routing of L2SYNC_OUT to L2SYNC_IN. See Motorola Application Note AN179/D "PowerPC Backside L2 Timing Analysis for the PCB Design Engineer."

The minimum L2CLK frequency of Table 12 is specified by the maximum delay of the internal DLL. The variable-tap DLL introduces up to a full clock period delay in the L2CLKOUTA, L2CLKOUTB and L2SYNC_OUT signals so that the returning L2SYNC_IN signal is phase aligned with the next core clock (divided by the L2 divisor ratio). Do not choose a core-to-L2 divisor which results in an L2 frequency below this minimum, or the L2CLKOUT signals provided for SRAM clocking will not be phase aligned with the PC7410 core clock at the SRAMs.

The maximum L2CLK frequency shown in Table 12 is the core frequency divided by one. Very few L2 SRAM designs will be able to operate in this mode. Most designs will select a greater core-to-L2 divisor to provide a longer L2CLK period for read and write access to the L2 SRAMs. The maximum L2CLK frequency for any application of the PC7410 will be a function of the AC timings of the PC7410, the AC timings for the SRAM, bus loading and printed circuit board trace length.

Atmel is similarly limited by system constraints and cannot perform tests of the L2 interface on a socketed part on a functional tester at the maximum frequencies of Table 12. Therefore, functional operation and AC timing information are tested at core-to-L2 divisors of 2 or greater.

L2 input and output signals are latched or enabled respectively by the internal L2CLK (which is SYSCLK multiplied up to the core frequency and divided down to the L2CLK frequency). In other words, the AC timings of Table 13 are entirely independent of L2SYNC_IN. In a closed loop system, where L2SYNC_IN is driven through the board trace by L2SYNC_OUT, L2SYNC_IN only controls the output phase of L2CLKOUTA and L2CLKOUTB which are used to latch or enable data at the SRAMs. However, since in a closed loop system L2SYNC_IN is held in phase alignment with the internal L2CLK, the signals of Table 13 are referenced to this signal rather than the not-externally-visible internal L2CLK. During manufacturing test, these times are actually measured relative to SYSCLK.

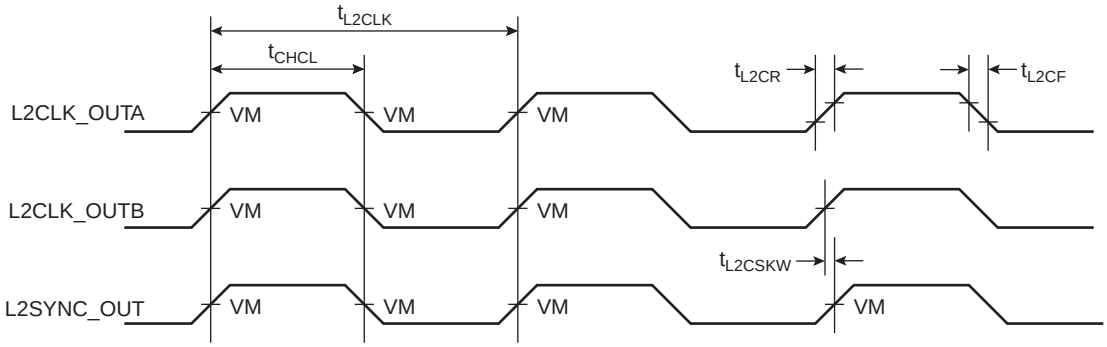
Table 12. L2CLK Output AC Timing Specifications at Recommended Operating Conditions (See Table 4)

		400 MHz		450 MHz		500 MHz		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{L2CLK} (1)(4)	L2CLK frequency	133	400	133	400	133	400	MHz
t_{L2CLK}	L2CLK cycle time	2.5	7.5	2.5	7.5	2.5	7.5	ns
t_{CHCL}/t_{L2CLK} (2)	L2CLK duty cycle	50		50		50		%
	Internal DLL-relock time (3)	640		640		640	-	L2CLK
	DLL capture window (5)	0	10	0	10	0	10	ns
t_{L2CSKW}	L2CLKOUT output-to-output skew (6)	-	50	-	50	-	50	ps
	L2CLKOUT output jitter (6)	-	±150	-	±150	-	±150	ps

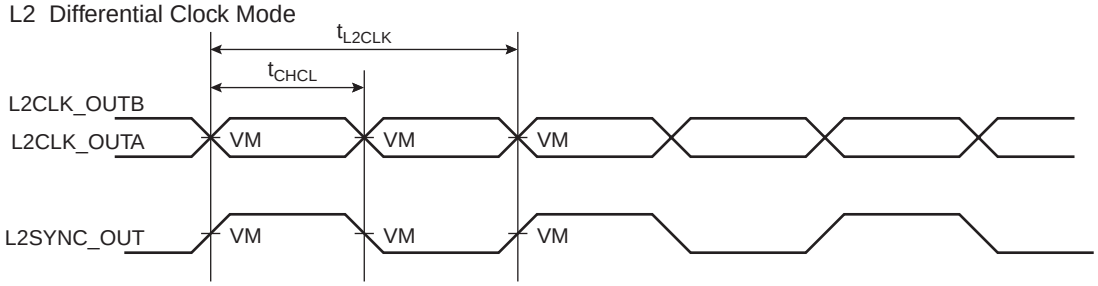
Notes:
1. L2CLK outputs are L2CLK_OUTA, L2CLK_OUTB, and L2SYNC_OUT pins. The L2CLK frequency to core frequency settings must be chosen such that the resulting L2CLK frequency and core frequency do not exceed their respective maximum or minimum operating frequencies. The maximum L2LCK frequency will be system-dependent. L2CLK_OUTA and L2CLK_OUTB must have equal loading.
2. The nominal duty cycle of the L2CLK is 50% measured at midpoint voltage.
3. The DLL re-lock time is specified in terms of L2CLKs. The number in the table must be multiplied by the period of L2CLK to compute the actual time duration in nanoseconds. Re-lock timing is guaranteed by design and characterization.
4. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 110 MHz. This adds more delay to each tap of the DLL.
5. Allowable skew between L2SYNC_OUT and L2SYNC_IN.
6. Guaranteed by design and not tested. This output jitter number represents the maximum delay of one tap forward or one tap back from the current DLL tap as the phase comparator seeks to minimize the phase difference between L2SYNC_IN and the internal L2CLK. This number must be comprehended in the L2 timing analysis. The input jitter on SYSCLK affects L2CLKOUT and the L2 address/data/control signals equally and therefore is already comprehended in the AC timing and does not have to be considered in the L2 timing analysis.

Figure 12. L2CLK_OUT Output Timing Diagram

L2 Single-Ended Clock Mode



L2 Differential Clock Mode



Note: VM = Midpoint Voltage ($L2OV_{DD}/2$)

L2 Bus AC Specifications

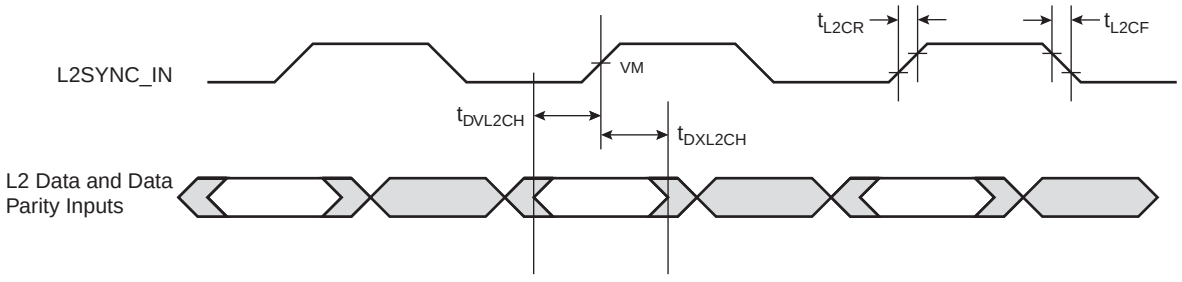
Table 13 provides the L2 bus interface AC timing specifications for the PC7410 as defined in Figure 13 and Figure 14 for the loading conditions described in Figure 15.

Table 13. L2 Bus Interface AC Timing Specifications at $V_{DD} = AV_{DD} = L2AV_{DD} = 1.8V \pm 100mV$ or $1.5V \pm 50mV$; $-55°C \le T_j \le 125°C$, $L2OV_{DD} = 2.5V \pm 100mV$ or $L2OV_{DD} = 1.8V \pm 100mV$

Symbol	Parameter	400, 450, 500 MHz		Unit
		Min	Max	
t_{L2CR} & t_{L2CF}(1)	L2SYNC_IN rise and fall time		1.0	ns
	Setup Times			ns
t_{DVL2CH}(2)	Data and parity	1.5		
	Input Hold Times			ns
t_{DXL2CH}(2)	Data and parity		0.0	
t_{L2CHOV}(3)(4)	Valid Times			ns
	All outputs when L2CR[14:15] = 00		2.5	
	All outputs when L2CR[14:15] = 01		2.5	
	All outputs when L2CR[14:15] = 10		2.9	
	All outputs when L2CR[14:15] = 11		3.5	
t_{L2CHOX}(3)	Output Hold Times			ns
	All outputs when L2CR[14:15] = 00	0.4		
	All outputs when L2CR[14:15] = 01	0.8		
	All outputs when L2CR[14:15] = 10	1.2		
	All outputs when L2CR[14:15] = 11	1.6		
t_{L2CHOZ}	L2SYNC_IN to high impedance			ns
	All outputs when L2CR[14:15] = 00		2.0	
	All outputs when L2CR[14:15] = 01		2.5	
	All outputs when L2CR[14:15] = 10		3.0	
	All outputs when L2CR[14:15] = 11		3.5	

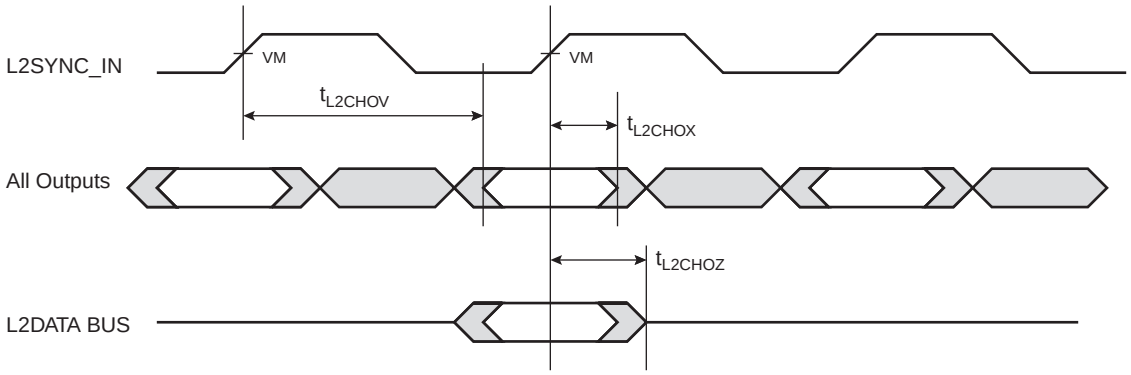
Notes:
1. Rise and fall times for the L2SYNC_IN input are measured from 20% to 80% of $L2OV_{DD}$.
2. All input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising edge of the input L2SYNC_IN (see Figure 13). Input timings are measured at the pins.
3. All output specifications are measured from the midpoint voltage of the rising edge of L2SYNC_IN to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50 Ω load (see Figure 15).
4. The outputs are valid for both single-ended and differential L2CLK modes. For pipelined registered synchronous burst RAMs, L2CR[14:15] = 00 is recommended. For pipelined late-write synchronous burst SRAMs, L2CR[14:15] = 10 is recommended.

Figure 13. L2 Bus Input Timing Diagram



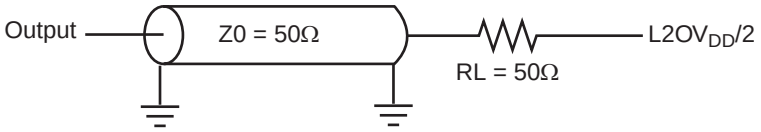
Note: VM = Midpoint Voltage ($L2OV_{DD}/2$)

Figure 14. L2 Bus Output Timing Diagram



Note: VM = Midpoint Voltage ($L2OV_{DD}/2$)

Figure 15. AC Test Load for the L2 Interface



IEEE 1149.1 AC Timing Specifications

Table 14 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 16, Figure 17, Figure 18 and Figure 19.

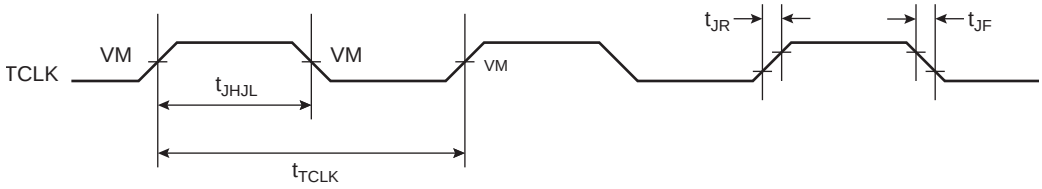
Table 14. JTAG AC Timing Specifications (Independent of SYSCLK) [1] at Recommended Operating Conditions (see Table 4)

Symbol	Parameter	Min	Max	Unit
f_{TCLK}	TCK frequency of operation	0	33.3	MHz
t_{TCLK}	TCK cycle time	30		ns
t_{JHJL}	TCK clock pulse width measured at OVDD/2	15		ns
t_{JR} & t_{JF}	TCK rise and fall times	0	2	ns
t_{TRST} [2]	$\overline{TRST}$ assert time	25		ns
	Input Setup Times:			ns
t_{DVJH} [3]	Boundary-scan data	4		
t_{IVJH}	TMS, TDI	0		
	Input Hold Times:			ns
t_{DXJH} [3]	Boundary-scan data	20		
t_{IXJH}	TMS, TDI	25		
	Valid Times:			ns
t_{JLDV} [4]	Boundary-scan data	4	20	
t_{JLOV}	TDO	4	25	
	TCK to output high impedance:			ns
t_{JLDZ} [4][5]	Boundary-scan data	3	19	
t_{JLOZ} [5]	TDO	3	9	

Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50 Ω load (see Figure 16). Time-of-flight delays must be added for trace lengths, vias and connectors in the system.
2. $\overline{TRST}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization

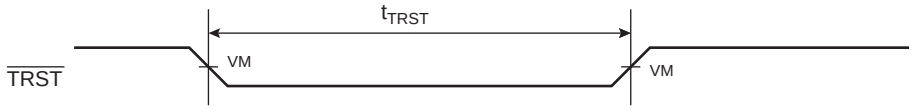
Figure 16. Alternate AC Test Load for the JTAG Interface

Figure 17. JTAG Clock Input Timing Diagram



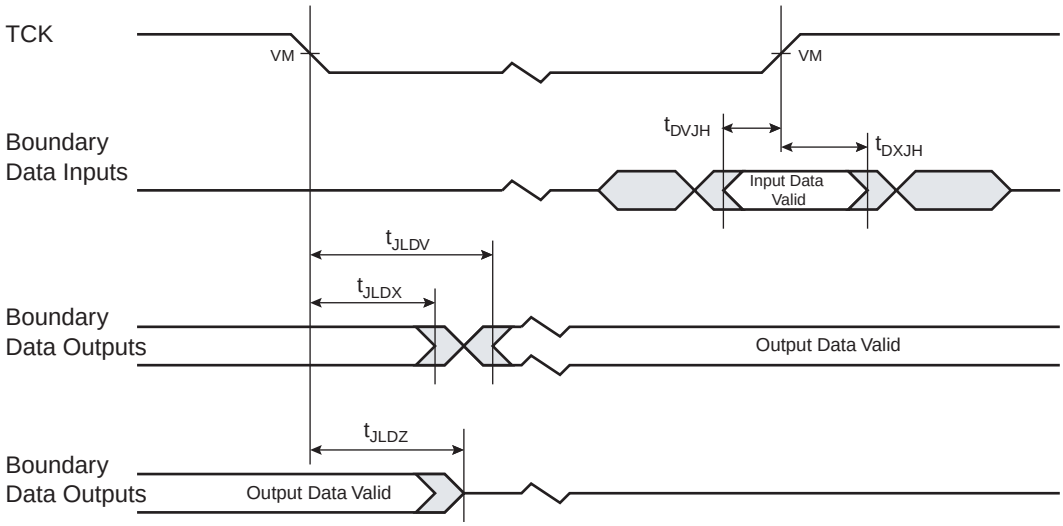
Note: VM = Midpoint Voltage (OV_{DD}/2)

Figure 18. $\overline{\text{TRST}}$ Timing Diagram



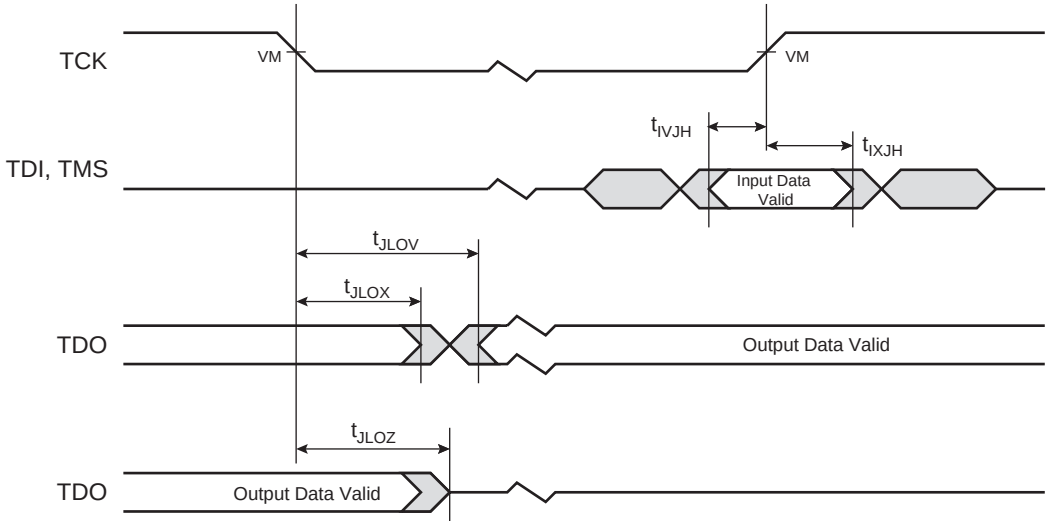
Note: VM = Midpoint Voltage ($OV_{DD}/2$)

Figure 19. Boundary-scan Timing Diagram



Note: VM = Midpoint Voltage ($OV_{DD}/2$)

Figure 20. Test Access Port Timing Diagram



Note: VM = Midpoint Voltage ($OV_{DD}/2$)

Preparation for Delivery

Handling

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of static buildup. However, the following handling practices are recommended:

- Devices should be handled on benches with conductive and grounded surfaces.
- Ground test equipment, tools and operator.
- Do not handle devices by the leads.
- Store devices in conductive foam or carriers.
- Avoid use of plastic, rubber or silk in MOS areas.
- Maintain relative humidity above 50% if practical.
- For CI-CGA packages, use specific tray to take care of the highest height of the package compared with the normal CBGA.

Package Mechanical Data

Parameters

The package parameters are as provided in the following list. The package type is 25x25 mm, 360-lead CBGA, HiTCE and CI-CGA.

Table 15. Package Parameters

Parameter	
Package outline	25 mm x 25 mm
Interconnects	360 (19 x 19 ball array minus one)
Pitch	1.27 mm (50 mil)
Minimum module height	2.65 mm (CBGA, HiTCE), 3.65 mm (CI-CGA)
Maximum module height	3.20 mm (CBGA), 3.24 mm (HiTCE), 4.20 mm (CI-CGA)
Ball or column diameter	0.89 mm (35 mil)

The following remarks apply to Figure 26 and Figure 27:

- Dimensions and tolerancing are as per ASME Y14.5M-1994.
- All dimensions are in millimeters.
- Top side A1 corner index is a metallized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array.
- Dimension B is the maximum solder ball diameter measured parallel to datum A.
- D2 and E2 define the area occupied by the die and underfill. Actual size of this area may be smaller than shown. D3 and E3 are the minimum clearance from the package edge to the chip capacitors.

Pin Assignment

BGA360 Package

Figure 21, Figure 22, Figure 23 and Figure 24 show top views of the packages available for the PC7410. Note that these drawings are not to scale.

Figure 21. Top View of 360-Ball CBGA and 360-Pin CI-CGA Packages

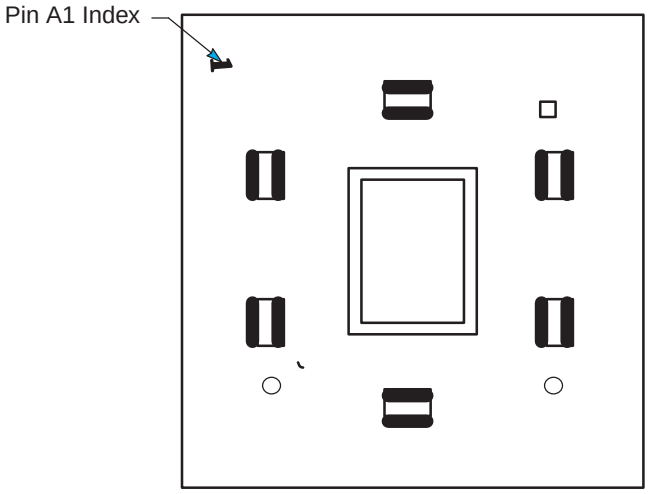


Figure 22. Top View of 360-pin CBGA and CI-CGA Packages

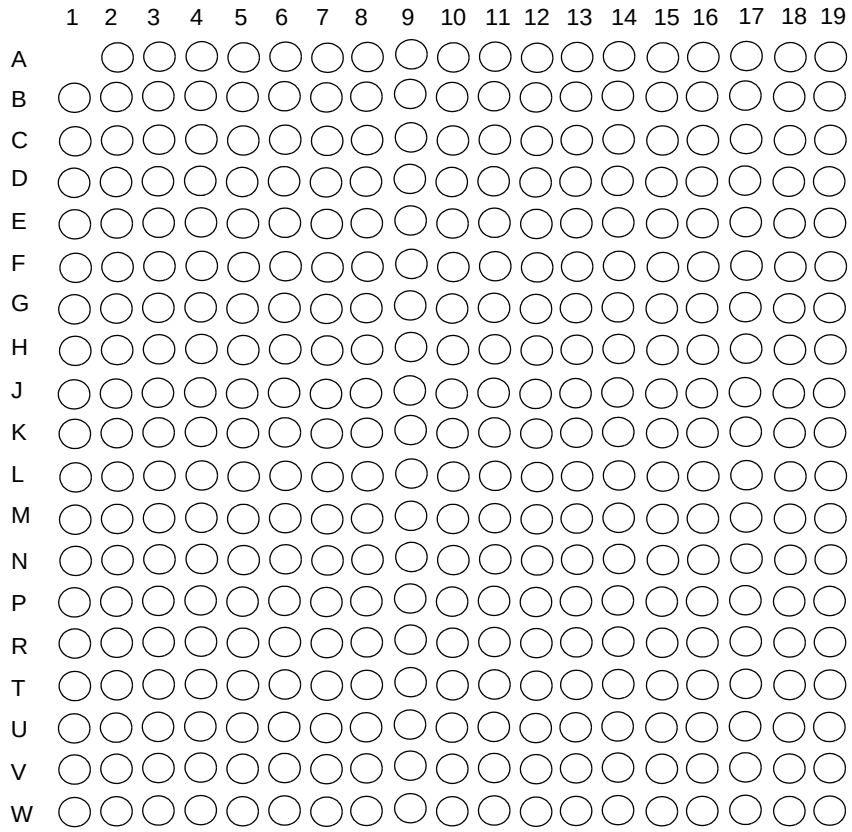


Figure 23. Cross-section of 360-ball CBGA and HiTCE Package

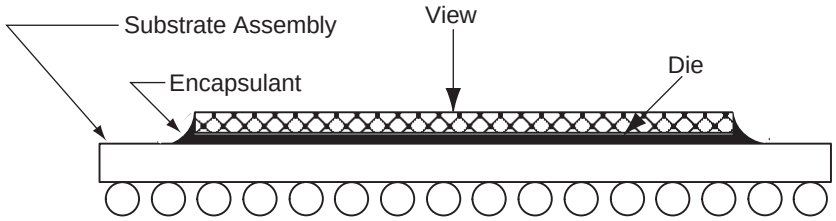


Figure 24. Cross-section of 360-column CI-CGA Package

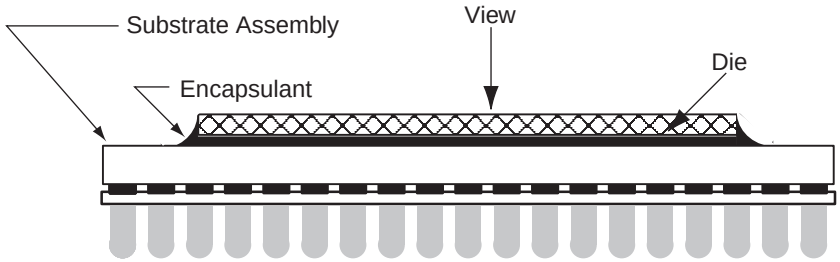


Table 16. Pinout Listing for the PC7410, 360-ball CBGA and CI-CGA packages

Signal Name	Pin Number	Active	I/O	I/F Select[1]
A[0:31]	A13, D2, H11, C1, B13, F2, C13, E5, D13, G7, F12, G3, G6, H2, E2, L3, G5, L4, G4, J4, H7, E1, G2, F3, J7, M3, H3, J2, J6, K3, K2, L2	High	I/O	BVSEL
$\overline{\text{AACK}}$	N3	Low	Input	BVSEL
$\overline{\text{ABB}}$[12] $\overline{\text{AMON[0]}}$[12]	L7	Low	Output	BVSEL
AP[0:3]	C4, C5, C6, C7	High	I/O	BVSEL
$\overline{\text{ARTRY}}$	L6	Low	I/O	BVSEL
AV_{DD}	A8			Vdd
$\overline{\text{BG}}$	H1	Low	Input	BVSEL
$\overline{\text{BR}}$	E7	Low	Output	BVSEL
BVSEL[1][3][8][9][14]	W1	High	Input	N/A
$\overline{\text{CHK}}$[4][8][9]	K11	Low	Input	BVSEL
$\overline{\text{CI}}$	C2	Low	I/O	BVSEL
$\overline{\text{CKSTP\_IN}}$	B8	Low	Input	BVSEL
$\overline{\text{CKSTP\_OUT}}$	D7	Low	Output	BVSEL
CLK_OUT	E3	High	Output	BVSEL
DBB[12] $\overline{\text{DMON[0]}}$[12]	K5	Low	Output	BVSEL
$\overline{\text{DBG}}$	K1	Low	Input	BVSEL

Table 16. Pinout Listing for the PC7410, 360-ball CBGA and CI-CGA packages (Continued)

Signal Name	Pin Number	Active	I/O	I/F Select(1)
DH[0:31]	W12, W11, V11, T9, W10, U9, U10, M11, M9, P8, W7, P9, W9, R10, W6, V7, V6, U8, V9, T7, U7, R7, U6, W5, U5, W4, P7, V5, V4, W3, U4, R5	High	I/O	BVSEL
DL[0:31]	M6, P3, N4, N5, R3, M7, T2, N6, U2, N7, P11, V13, U12, P12, T13, W13, U13, V10, W8, T11, U11, V12, V8, T1, P1, V1, U1, N1, R2, V3, U3, W2	High	I/O	BVSEL
DP[0:7]	L1, P2, M2, V2, M1, N2, T3, R1	High	I/O	BVSEL
$\overline{\text{DRDY}}$(6)(8)(13)	K9	Low	Output	BVSEL
$\overline{\text{DBWO}}$ DTI[0]	D1	Low	Input	BVSEL
DTI[1:2](10)(13)	H6, G1	High	Input	BVSEL
$\overline{\text{EMODE}}$(7)(10)	A3	Low	Input	BVSEL
$\overline{\text{GBL}}$	B1	Low	I/O	BVSEL
GND	D10, D14, D16, D4, D6, E12, E8, F4, F6, F10, F14, F16, G9, G11, H5, H8, H10, H12, H15, J9, J11, K4, K6, K8, K10, K12, K14, K16, L9, L11, M5, M8, M10, M12, M15, N9, N11, P4, P6, P10, P14, P16, R8, R12, T4, T6, T10, T14, T16			N/A
$\overline{\text{HIT}}$(6)(8)	B5	Low	Output	BVSEL
$\overline{\text{HRESET}}$	B6	Low	Input	BVSEL
$\overline{\text{INT}}$	C11	Low	Input	BVSEL
L1_TSTCLK(2)	F8	High	Input	BVSEL
L2ADDR[0:16]	L17, L18, L19, M19, K18, K17, K15, J19, J18, J17, J16, H18, H17, J14, J13, H19, G18	High	Output	L2VSEL
L2ADDR[17:18](8)	K19, W19	High	Output	L2VSEL
$L2AV_{DD}$	L13			Vdd
$\overline{\text{L2CE}}$	P17	Low	Output	L2VSEL
L2CLKOUTA	N15	High	Output	L2VSEL
L2CLKOUTB	L16	High	Output	L2VSEL
L2DATA[0:63]	U14, R13, W14, W15, V15, U15, W16, V16, W17, V17, U17, W18, V18, U18, V19, U19, T18, T17, R19, R18, R17, R15, P19, P18, P13, N14, N13, N19, N17, M17, M13, M18, H13, G19, G16, G15, G14, G13, F19, F18, F13, E19, E18, E17, E15, D19, D18, D17, C18, C17, B19, B18, B17, A18, A17, A16, B16, C16, A14, A15, C15, B14, C14, E13	High	I/O	L2VSEL
L2DP[0:7]	V14, U16, T19, N18, H14, F17, C19, B15	High	I/O	L2VSEL
$L2OV_{DD}$(11)	D15, E14, E16, H16, J15, L15, M16, K13, P15, R14, R16, T15, F15			N/A
L2SYNC_IN	L14	High	Input	L2VSEL
L2SYNC_OUT	M14	High	Output	L2VSEL
L2_TSTCLK(2)	F7	High	Input	BVSEL
L2VSEL(1)(3)(8)(9)(14)	A19	High	Input	$\overline{\text{N/A}}$

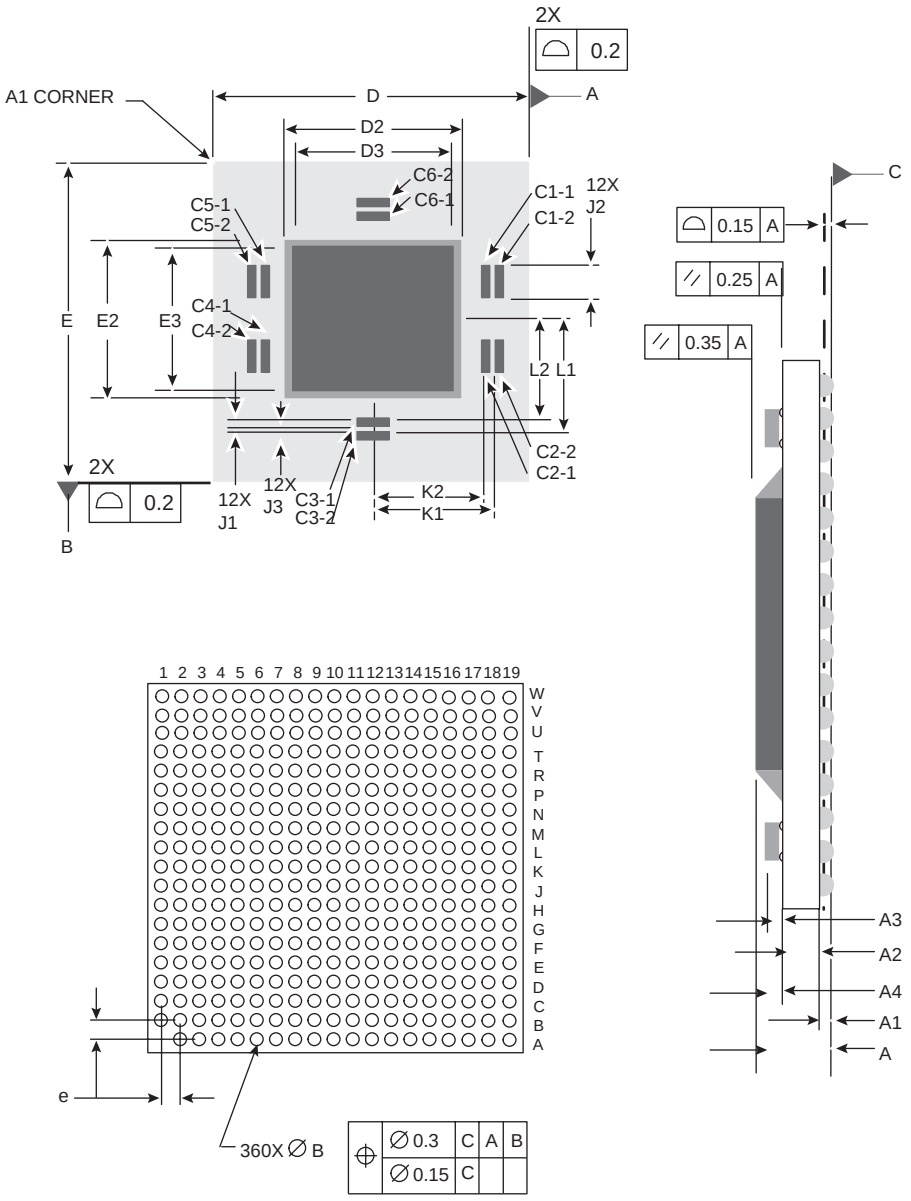
Table 16. Pinout Listing for the PC7410, 360-ball CBGA and CI-CGA packages (Continued)

Signal Name	Pin Number	Active	I/O	I/F Select(1)
$\overline{\text{L2WE}}$	N16	Low	Output	L2VSEL
L2ZZ	G17	High	Output	L2VSEL
$\overline{\text{LSSD\_MODE}}$(2)	F9	Low	Input	BVSEL
$\overline{\text{MCP}}$	B11	Low	Input	BVSEL
OV_{DD}	D5, D8, D12, E4, E6, E9, E11, F5, H4, J5, L5, M4, P5, R4, R6, R9, R11, T5, T8, T12			N/A
PLL_CFG[0:3]	A4, A5, A6, A7	High	Input	BVSEL
$\overline{\text{QACK}}$	B2	Low	Input	BVSEL
$\overline{\text{QREQ}}$	J3	Low	Output	BVSEL
$\overline{\text{RSRV}}$	D3	Low	Output	BVSEL
$\overline{\text{SHD0}}$(8)	B3	Low	I/O	BVSEL
$\overline{\text{SHD1}}$(5)(8)	B4	Low	I/O	BVSEL
$\overline{\text{SMI}}$	A12	Low	Input	BVSEL
$\overline{\text{SRESET}}$	E10	Low	Input	BVSEL
SYSCLK	H9		Input	BVSEL
$\overline{\text{TA}}$	F1	Low	Input	BVSEL
TBEN	A2	High	Input	BVSEL
$\overline{\text{TBST}}$	A11	Low	Output	BVSEL
TCK	B10	High	Input	BVSEL
TDI(9)	B7	High	Input	BVSEL
TDO	D9	High	Output	BVSEL
$\overline{\text{TEA}}$	J1	Low	Input	BVSEL
TMS(9)	C8	High	Input	BVSEL
$\overline{\text{TRST}}$(9)(14)	A10	Low	Input	BVSEL
$\overline{\text{TS}}$	K7	Low	I/O	BVSEL
TSIZ[0:2]	A9, B9, C9	High	Output	BVSEL
TT[0:4]	C10, D11, B12, C12, F11	High	I/O	BVSEL
$\overline{\text{WT}}$	C3	Low	I/O	BVSEL
V_{DD}	G8, G10, G12, J8, J10, J12, L8, L10, L12, N8, N10, N12			N/A

Notes:
1. OV_{DD} supplies power to the processor bus, JTAG and all control signals except the L2 cache controls ($\overline{\text{L2CE}}$, $\overline{\text{L2WE}}$, and $\overline{\text{L2ZZ}}$); $L2OV_{DD}$ supplies power to the L2 cache interface (L2ADDR[0:18], L2ASPARE, L2DATA[0:63], L2DP[0:7] and L2SYNC_OUT) and the L2 control signals and V_{DD} supplies power to the processor core and the PLL and DLL (after filtering to become AV_{DD} and $L2AV_{DD}$ respectively). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL/L2VSEL pin configurations of Table 3 and the voltage supplied. For actual recommended value of V_{IN} or supply voltages, see Table 4.
2. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
3. To allow for future I/O voltage changes, provide the option to connect BVSEL and L2VSEL independently to either OV_{DD} (selects 2.5V), GND (selects 1.8V), or to $\overline{\text{HRESET}}$ (selects 2.5V). The PC7410 Both the 60x processor bus and the L2 bus only support the 1.8 and 2.5 options (see Table 3). the default selection if BVSEL and/or L2VSEL is left unconnected is 2.5V
4. Connect to $\overline{\text{HRESET}}$ to trigger post power-on-reset (por) internal memory test.

5. Ignored in 60x bus mode.
6. Unused output in 60x bus mode.
7. Deasserted (pulled high) at $\overline{\text{HRESET}}$ for 60x bus mode.
8. Uses one of 9 existing no-connects in PC750's 360-ball BGA package.
9. Internal pull-up on die.
10. Reuses PC750's $\overline{\text{DRTRY}}$, $\overline{\text{DBDIS}}$ and TLBISYNC pins (DTI1, DTI2 and $\overline{\text{EMODE}}$ respectively).
11. The VOLTDET pin position on the PC750 360-ball CBGA package is now an $L2OV_{DD}$ pin on the PC7410 packages.
12. Output only for PC7410, was I/O for PC750.
13. Enhanced mode only.
14. To overcome the internal pull-up resistance and ensure this input will recognize a low signal, a pull-down resistance less than 250Ω should be used.

Figure 25. Mechanical Dimensions and Bottom Surface Nomenclature of the 360-ball CBGA Package

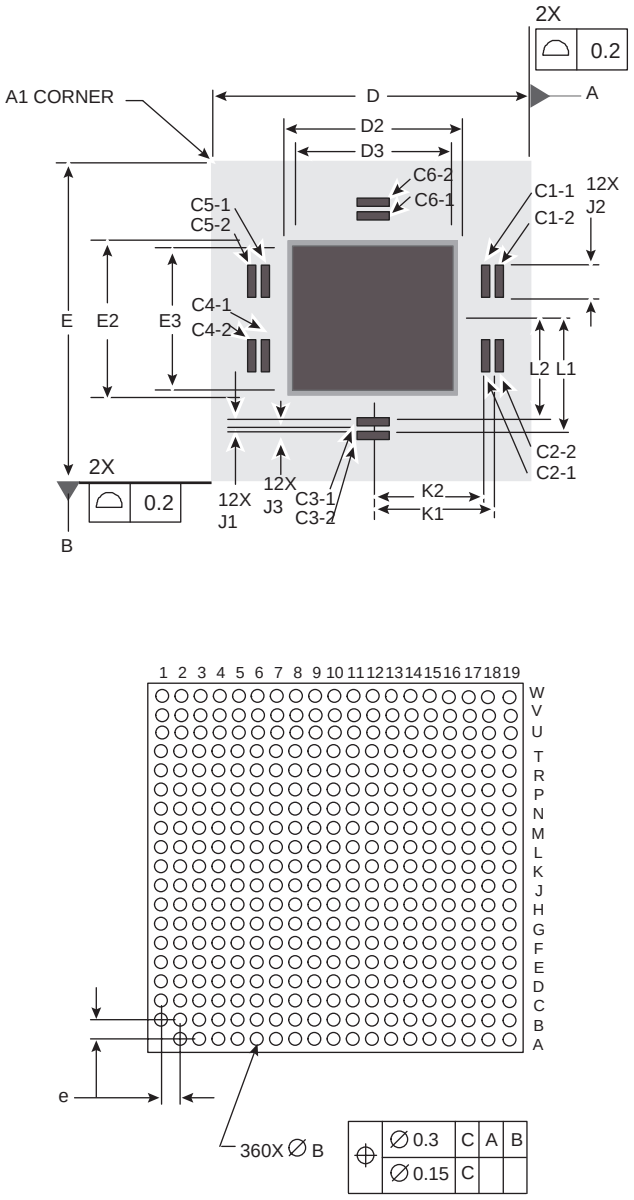


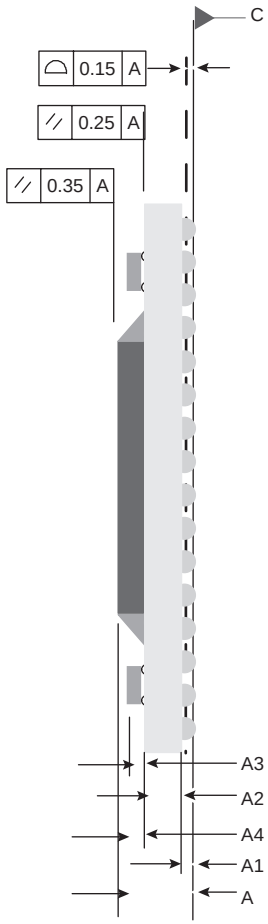
	Millimeters	
DIM	MIN	MAX
A	2,72	3,2
A1	0,8	1
A2	1,1	1,3
A3		0,6
A4	0,82	0,9
b	0,82	0,93
D	25 BSC	
D2	10 typ	
D3	6,32	
e	1,27 BSC	
E	25 BSC	
E2	12,6 typ	
E3	8,26	
J1	0,89 BSC	
J2	3,2 BSC	
J3	0,68 BSC	
K1	6,56	
K2	8,13	
L1	8,61	
L2	7,04	

Package Caps	Value µF	Voltage Reference
C1-1	0.01	$L2OV_{DD}$
C1-2		GND
C2-1	0.01	$L2OV_{DD}$
C2-2		GND
C3-1	0.01	V_{DD}
C3-2		GND
C4-1	0.01	OV_{DD}
C4-2		GND
C5-1	0.01	OV_{DD}
C5-2		GND
C6-1	0.01	V_{DD}
C6-2		GND

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters
3. Top side A1 corner index is a metallized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array

Figure 26. Mechanical Dimensions and Bottom Surface Nomenclature of the 360-ball HiTCE Package



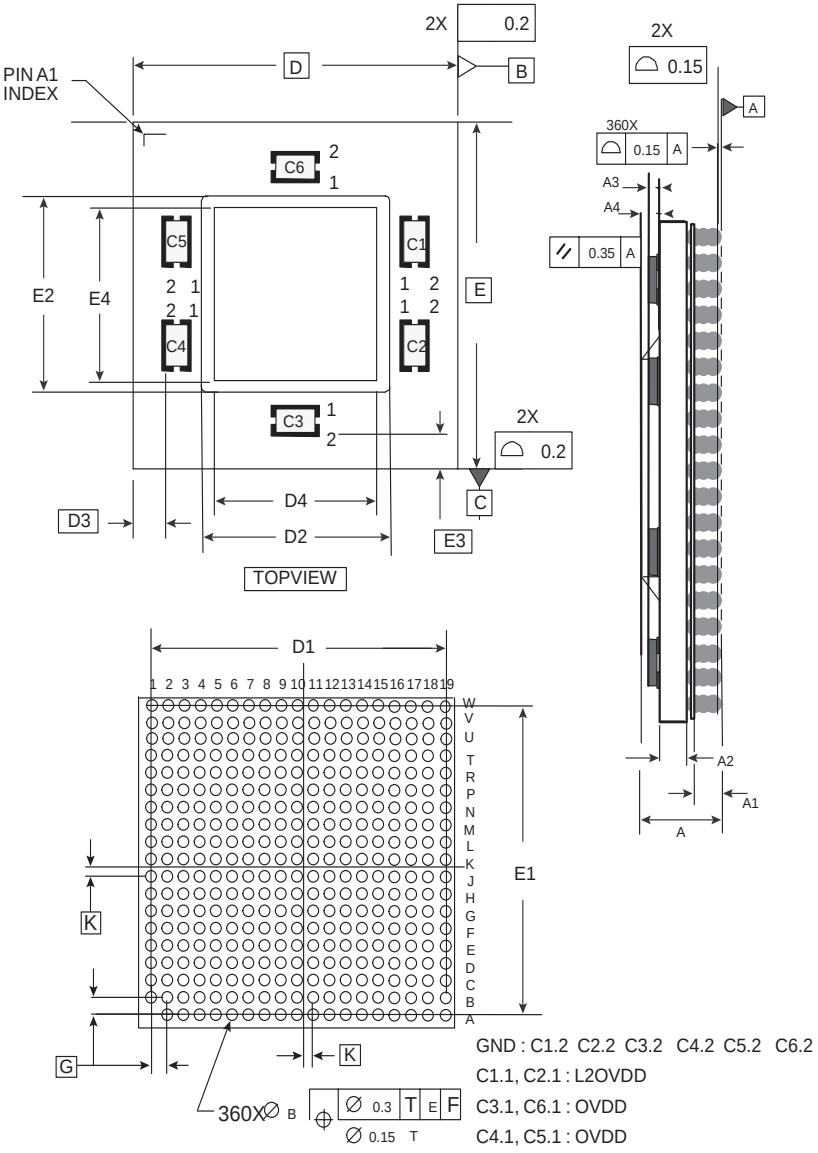


	Millimeters	
DIM	MIN	MAX
A	2,72	3,2
A1	0,8	1
A2	1,1	1,3
A3		0,6
A4	0,82	0,9
b	0,82	0,93
D	25 BSC	
D2	10 typ	
D3	6,32	
e	1,27 BSC	
E	25 BSC	
E2	12,6 typ	
E3	8,26	
J1	0,89 BSC	
J2	3,2 BSC	
J3	0,68 BSC	
K1	6,56	
K2	8,13	
L1	8,61	
L2	7,04	

Package Caps	Value µF	Voltage Reference
C1-1	0.01	$L2OV_{DD}$
C1-2		GND
C2-1	0.01	$L2OV_{DD}$
C2-2		GND
C3-1	0.01	V_{DD}
C3-2		GND
C4-1	0.01	OV_{DD}
C4-2		GND
C5-1	0.01	OV_{DD}
C5-2		GND
C6-1	0.01	V_{DD}
C6-2		GND

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M, 1994
2. Dimensions in millimeters
3. Top side A1 corner index is a metallized feature with various shapes. Bottom side A1 corner is designated with a ball missing from the array

Figure 27. Mechanical Dimensions and Bottom Surface Nomenclature of the 360-column CI-CGA Package



Parameter	Min	Max	Parameter	Min	Max
A	3.4	4.20	D3	2.75	–
A1	1.545	1.695	D4	6.32	
A2	1.10	1.30	E	25.00 BASIC	
A3	–	0.6	E1	22.86 BASIC	
A4	0.82	0.9	E2	–	15
B	0.82	0.93	E3	3.00	–
D	25.00 BASIC		E4	8.26	
D1	22.86 BASIC		G	1.27 BASIC	
D2	–	13			

Clock Selection

The PC7410's PLL is configured by the PLL_CFG[0:3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the PC7410 is shown in Table 17 for example frequencies. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with the minimum and maximum core frequencies listed in Table 11.

Table 17. PC7410 Microprocessor PLL Configuration(1)(2)(3)(4)(5)

PLL_CFG [0:3]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)								
	Bus-to-Core Multiplier	Core-to-VCO Multiplier	Bus 33.3 MHz	Bus 50 MHz	Bus 66.6 MHz	Bus 75 MHz	Bus 83.3 MHz	Bus 100 MHz	Bus 133 MHz
0100	2x	2x							
0110	2.5x	2x							
1000	3x	2x							400 (800)
1110	3.5x	2x						350 (700)	465 (930)
1010	4x	2x						400 (800)	
0111	4.5x	2x					375 (750)	450 (900)	
1011	5x	2x				375 (750)	416 (833)	500 (1000)	
1001	5.5x	2x			366 (733)	412 (825)	458 (916)		
1101	6x	2x			400 (800)	450 (900)	500 (1000)		
0101	6.5x	2x			433 (866)	488 (967)			
0010	7x	2x		350 (700)	466 (933)				
0001	7.5x	2x		375 (750)	500 (1000)				
1100	8x	2x		400 (800)					
0000	9x	2x		450 (900)					
0011	PLL off/bypass		PLL off, SYSCLK clocks core circuitry directly, 1x bus-to-core implied						
1111	PLL off		PLL off, no core clocking occurs						

Notes:
1. PLL_CFG[0:3] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the PC7410; see "Clock AC Specifications" on page 20 for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use and third- party emulator tool development only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL-off mode, no clocking occurs inside the PC7410 regardless of the SYSCLK input.
5. PLL-off mode should not be used during chip power-up sequencing.

The PC7410 generates the clock for the external L2 synchronous data SRAMs by dividing the core clock frequency of the PC7410. The divided-down clock is then phase-adjusted by an on-chip delay-lock-loop (DLL) circuit and should be routed from the PC74107410 to the external RAMs. A separate clock output, L2SYNC_OUT is sent out half the distance to the SRAMs and then returned as an input to the DLL on pin L2SYNC_IN so that the rising-edge of the clock as seen at the external RAMs can be aligned to the clocking of the internal latches in the L2 bus interface.

The core-to-L2 frequency divisor for the L2 PLL is selected through the L2CLK bits of the L2CR register. Generally, the divisor must be chosen according to the frequency supported by the external RAMs, the frequency of the PC7410 core, and the phase adjustment range that the L2 DLL supports. Table 18 shows various example L2 clock frequencies that can be obtained for a given set of core frequencies. The minimum L2 frequency target is 133 MHz. Sample core-to-L2 frequencies for the PC7410 is shown in Table 18. In this example, shaded cells represent settings that, for a given core frequency, result in L2 frequencies that do not comply with the minimum and maximum L2 frequencies listed in Table 14.

Table 18. Sample Core-to-L2 Frequencies

Core Frequency in MHz	÷1	÷1.5	÷2	÷2.5	÷3	÷3.5	÷4
350	350	233	175	140	–	–	–
366	366	244	183	147	–	–	–
400	400	266	200	160	133	–	–
433	–	288	216	173	144	–	–
450	–	300	225	180	150	–	–
466	–	311	233	186	155	133	–
500	–	333	250	200	166	143	–

Note: The core and L2 frequencies are for reference only. Some examples may represent core or L2 frequencies which are not useful, not supported or not tested for by the PC7410; see “L2 Clock AC Specifications” on page 23 for valid L2CLK frequencies. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 150 MHz.

System Design Information

PLL and DLL Power Supply Filtering

The AV_{DD} and $L2AV_{DD}$ power signals are provided on the PC7410 to supply power to the PLL and DLL, respectively.

On systems that use the PC7410 CBGA device, the $L2AV_{DD}$ filter should implement the circuit shown in Figure 28. The AV_{DD} filter on the PC7410 CBGA device should implement the circuit shown in Figure 29.

On systems that use the PC7410 HITCE device, the AV_{DD} and $L2AV_{DD}$ input signals should both implement the circuit shown in Figure 28.

The circuit shown below should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. A separate circuit should be placed as close as possible to the $L2AV_{DD}$ pin. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 360 CBGA footprint, without the inductance of vias. The $L2AV_{DD}$ pin may be more difficult to route, but is proportionately less critical.

It is the recommendation of Motorola, that systems that implement the AV_{DD} filter shown in Figure 29 design in the pads for the removed capacitors (shown in Figure 28), to provide for the possible reintroduction of the filter in Figure 28. This would be necessary in case there is a planned transition to the HCTE package of the PC7410.

Figure 28. PLL Power Supply Filter Circuit #1

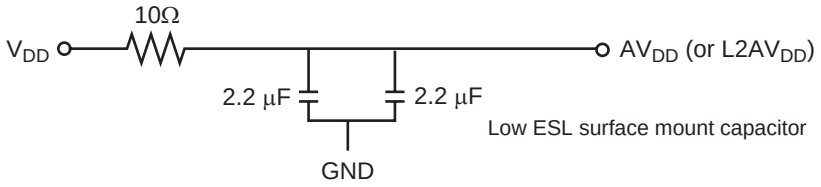
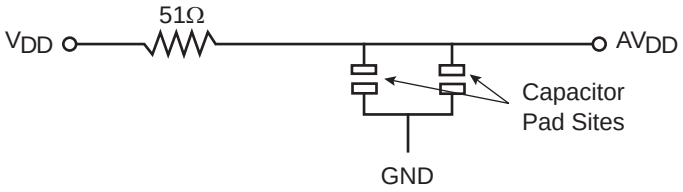


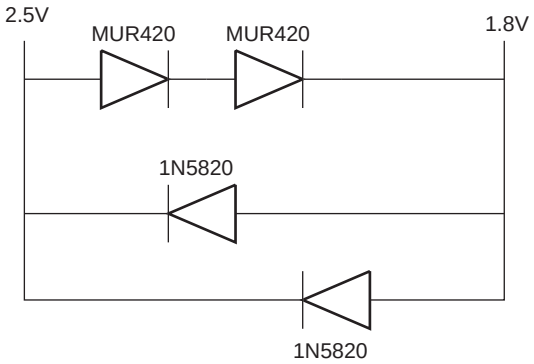
Figure 29. PLL Power Supply Filter Circuit #2



Power Supply Voltage Sequency

The notes in Table 2 contain cautions about the sequencing of the external bus voltages and core voltage of the PC7410 (when they are different). These cautions are necessary for the long term reliability of the part. If they are violated, the electrostatic discharge (ESD) protection diodes will be forward-biased and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, one or both of the circuits of Figure 30 can be added to meet these requirements. The MUR420 Schottky diodes of Figure 30 control the maximum potential difference between the external bus and core power supplies on power-up and the 1N5820 diodes regulate the maximum potential difference on power-down.

Figure 30. Example Voltage Sequencing Circuits



Decoupling Recommendations

Due to the PC7410's dynamic power management feature, large address and data buses and high operating frequencies, the PC7410 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the PC7410 system and the PC7410 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, and $L2OV_{DD}$ pin of the PC7410. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, (L2)OV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should have a value of 0.01 µF or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0508 or 0603 orientations where connections are made along the length of the part. Consistent with the recommendations of Dr. Howard Johnson in High Speed Digital Design: A Handbook of Black Magic (Prentice Hall, 1993) and contrary to previous recommendations for decoupling PowerPC microprocessors, multiple small capacitors of equal value are recommended over using multiple values of capacitance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, $L2OV_{DD}$, and OV_{DD} planes to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100 - 330 µF (AVX TPS tantalum or Sanyo OSCON).

Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, $L2OV_{DD}$, and GND pins of the PC7410.

See "L2 Clock AC Specifications" on page 23 for a discussion of the L2SYNC_OUT and L2SYNC_IN signals.

Output Buffer DC Impedance

The PC7410 60x and L2 I/O drivers are characterized over process, voltage and temperature. To measure Z_0, an external resistor is connected from the chip pad to OV_{DD} or GND. Then the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 31).

The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held low, SW2 is closed (SW1 is open), and R_N is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then $Z_0 = (R_P + R_N)/2$.

Figure 31. Driver Impedance Measurement

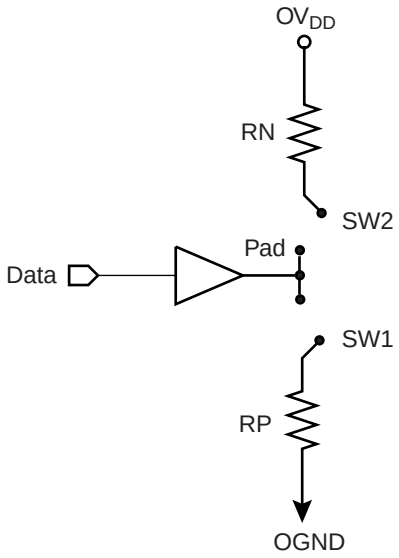


Table 19 summarizes the signal impedance results. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 19. Impedance Characteristics with V_{DD} = 1.8V, OV_{DD} = 1.8V or 2.5V, T_j = -55°C to 125°C

Impedance	Processor bus	L2 Bus	Symbol	Unit
R_N	41.5 - 54.3	42.7 - 54.1	Z_0	Ohms
R_P	37.3 - 55.3	39.3 - 50	Z_0	Ohms

Pull-up Resistor Requirements

The PC7410 requires pull-up resistors (1 kΩ–5 kΩ) on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the PC7410 or other bus masters. These pins are: $\overline{TS}$, $\overline{ARTRY}$, $\overline{SHDO}$, $\overline{SHD1}$.

Four test pins also require pull-up resistors (100Ω–1 kΩ). These pins are $\overline{CHK}$, L1_TSTCLK, L2_TSTCLK, and $\overline{LSSD\_MODE}$. These signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.

If pull-down resistors are used to configure BVSEL or L2VSEL, the resistors should be less than 250Ω. (see Table 12). Because PLL_CFG[0:3] must remain stable during normal operation, strong pull-up and pull-down resistors (1 kΩ or less) are recommended to configure these signals in order to protect against erroneous switching due to ground bounce, power supply noise or noise coupling.

In addition, $\overline{CKSTP\_OUT}$ is an open-drain style output that requires a pull-up resistor (1 kΩ–5 kΩ) if it is used by the system. The $\overline{CKSTP\_IN}$ signal should likewise be pulled up through a pull-up resistor (1 kΩ–5 kΩ) to prevent erroneous assertions of this signal.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Since the PC7410 must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on the PC7410 or by other receivers in the system. These signals can be pulled up through weak (10 kΩ) pull-up resistors by the system, address bus driven mode can be enabled (see the PC7410 RISC Microporcessor Family Users' Manual for more information on this mode), or these signals may be otherwise driven by the system during inactive periods of the bus to avoid this additional power draw. The snooped address and transfer attribute inputs are: A[0:31], AP[0:3], TT[0:4], $\overline{CI}$, $\overline{WT}$, and $\overline{GBL}$.

In systems where $\overline{GBL}$ is not connected and other devices may be asserting $\overline{TS}$ for a snoopable transaction while not driving $\overline{GBL}$ to the processor, we recommend that a strong (1 kΩ) pull-up resistor be used on $\overline{GBL}$. Note that the PC7410 will only snoop transactions when $\overline{GBL}$ is asserted.

The data bus input receivers are normally turned off when no read operation is in progress and, therefore, do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups, or that those signals be otherwise driven by the system during inactive periods by the system. The data bus signals are: DH[0:31], DL[0:31], and DP[0:7].

If address or data parity is not used by the system, and the respective parity checking is disabled through HID0, the input receivers for those pins are disabled, and those pins do not require pull-up resistors and should be left unconnected by the system. If parity checking is disabled through HID0, and parity generation is not required by the PC7410 (note that the PC7410 always generates parity), then all parity pins may be left unconnected by the system. The L2 interface does not normally require pull-up resistors.

JTAG Configuration Signals

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset.

Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 32 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted ensuring that the JTAG scan chain is initialized during power-on. While Motorola recommends that the COP header be designed into the system as shown in Figure 32, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

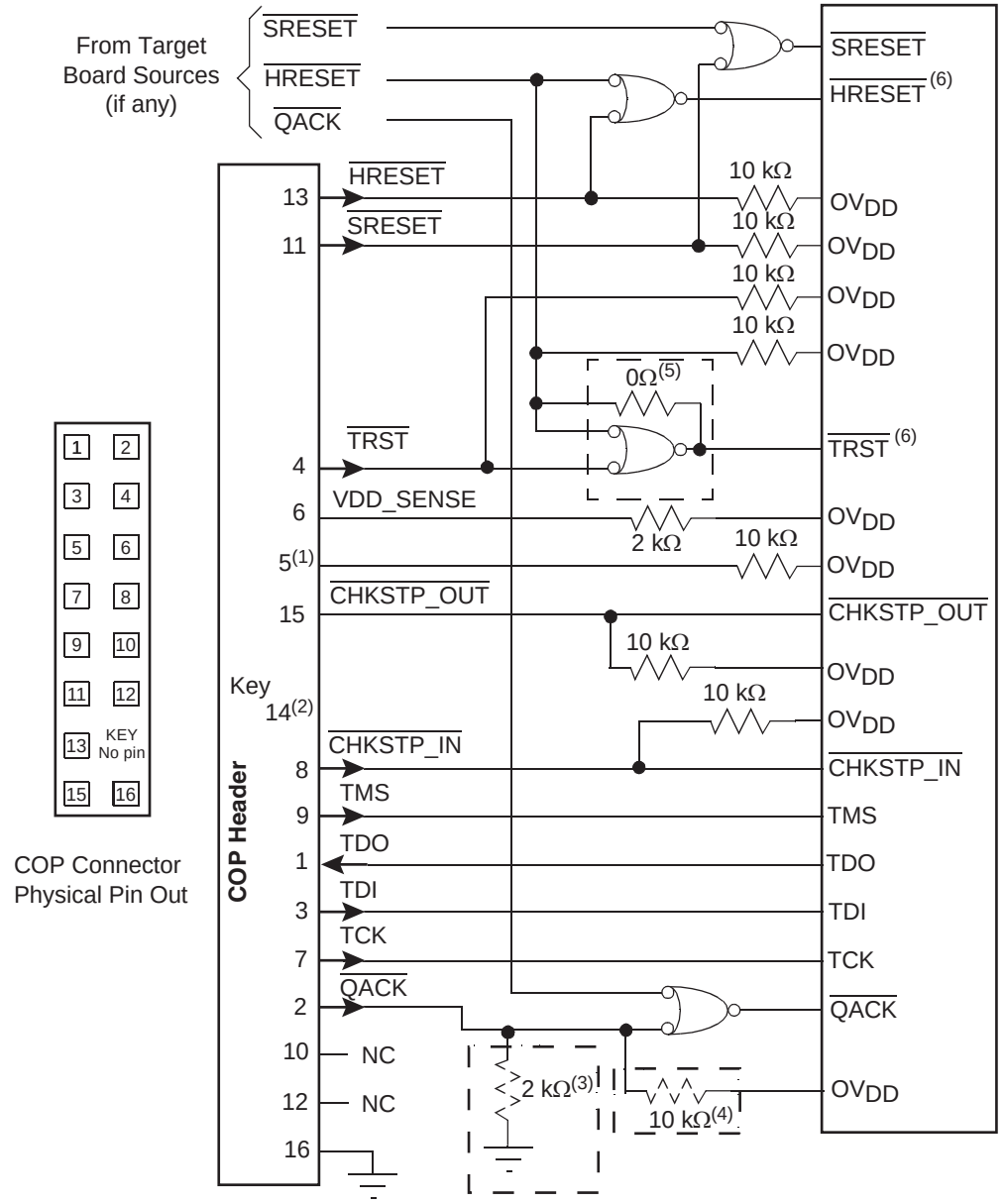
The COP header shown in Figure 32 adds many benefits — breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface — and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

There is no standardized way to number the COP header shown in Figure 32; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 32 is common to all known emulators.

The $\overline{\text{QACK}}$ signal shown in Figure 32 is usually connected to the PCI bridge chip in a system and is an input to the PC7410 informing it that it can go into the quiescent state. Under normal operation this occurs during a low-power mode selection. In order for COP to work, the PC7410 must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. If the product does not, a pull-down resistor can be populated to assert this signal. Additionally, some emulator products implement open-drain type outputs and can only drive $\overline{\text{QACK}}$ asserted; for these tools, a pull-up resistor can be implemented to ensure this signal is deasserted when it is not being driven by the tool. Note that the pull-up and pull-down resistors on the $\overline{\text{QACK}}$ signal are mutually exclusive and it is never necessary to populate both in a system. To preserve correct power-down operation, $\overline{\text{QACK}}$ should be merged via logic so that it also can be driven by the PCI bridge.

Figure 32. COP Connector Diagram



Notes:
1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented on the PC7410. Connect pin 5 of the COP header to OV_{DD} with a 10 kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Component not populated. Populate only if debug tool does not drive $\overline{\text{QACK}}$.
4. Populate only if debug tool uses an open-drain type output and does not actively deassert $\overline{\text{QACK}}$.
5. If the JTAG interface is implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ from the COP header though an AND gate to $\overline{\text{TRST}}$ of the part. If the JTAG interface is not implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ of the part through a 0Ω isolation resistor.
6. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown above.

Table 20. COP Pin Definitions

Pins	Signal	Connection	Special Notes
1	TDO	TDO	
2	$\overline{\text{QACK}}$	QACK	Add 2K pull-down to ground. Must be merged with on-board $\overline{\text{QACK}}$, if any.
3	TDI	TDI	
4	$\overline{\text{TRST}}$	TRST	Add 2K pull-down to ground. Must be merged with on-board $\overline{\text{TRST}}$ if any. See Figure 32.
5	RUN/$\overline{\text{STOP}}$	No Connect	Used on 604e; leave no-connect for all other processors.
6	VDD_SENSE	VDD	Add 2K pull-up to OV_{DD} (for short circuit limiting protection only).
7	TCK	TCK	
8	$\overline{\text{CKSTP\_IN}}$	CKSTP_IN	Optional. Add 10K pull-up to OV_{DD}. Used on several emulator products. Useful for checkstopping the processor from a logic analyzer of other external trigger.
9	TMS	TMS	
10	N/A		
11	$\overline{\text{SRESET}}$	SRESET	Merge with on-board $\overline{\text{SRESET}}$, if any.
12	N/A		
13	$\overline{\text{HRESET}}$	HRESET	Merge with on-board $\overline{\text{HRESET}}$.
14	N/A		Key location; pin should be removed.
15	$\overline{\text{CKSTP\_OUT}}$	CKSTP_OUT	Add 10K pull-up to OV_{DD}.
16	Ground	Digital Ground	

Boundary scan testing is enabled through the JTAG interface signals. (BSDL descriptions of the PC7410 are available on the Internet at www.mot.com/PowerPC/teksupport.) The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification but is provided on all PowerPC implementations. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Since the JTAG interface is also used for accessing the common on-chip processor (COP) function of PowerPC processors, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The common on-chip processor (COP) function of PowerPC processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 32 allows the COP to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. The pull-down resistor on $\overline{\text{TRST}}$ ensures that the JTAG scan chain is initialized during power-on if a JTAG interface cable is not attached; if it is attached, it is responsible for driving $\overline{\text{TRST}}$ when needed.

The COP header shown in Figure 32 adds many benefits – breakpoints, watchpoints, register and memory examination/modification and other standard debugger features are possible through this interface – and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025” square-post 0.100” centered header assembly (often called a “Berg” header). The connector typically has pin 14 removed as a connector key, as shown in Figure 32.

Definitions

Datasheet Status Description

Table 21. Datasheet Status

Datasheet Status		Validity
Objective specification	This datasheet contains target and goal specifications for discussion with customer and application validation.	Before design phase
Target specification	This datasheet contains target or goal specifications for product development.	Valid during the design phase
Preliminary specification α-site	This datasheet contains preliminary data. Additional data may be published later; could include simulation results.	Valid before characterization phase
Preliminary specification β-site	This datasheet also contains characterization results.	Valid before the industrialization phase
Product specification	This datasheet contains final product specification.	Valid for production purposes
Limiting Values		
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.		
Application Information		
Where application information is given, it is advisory and does not form part of the specification.		

Life Support Applications

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Atmel customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Atmel for any damages resulting from such improper use or sale.

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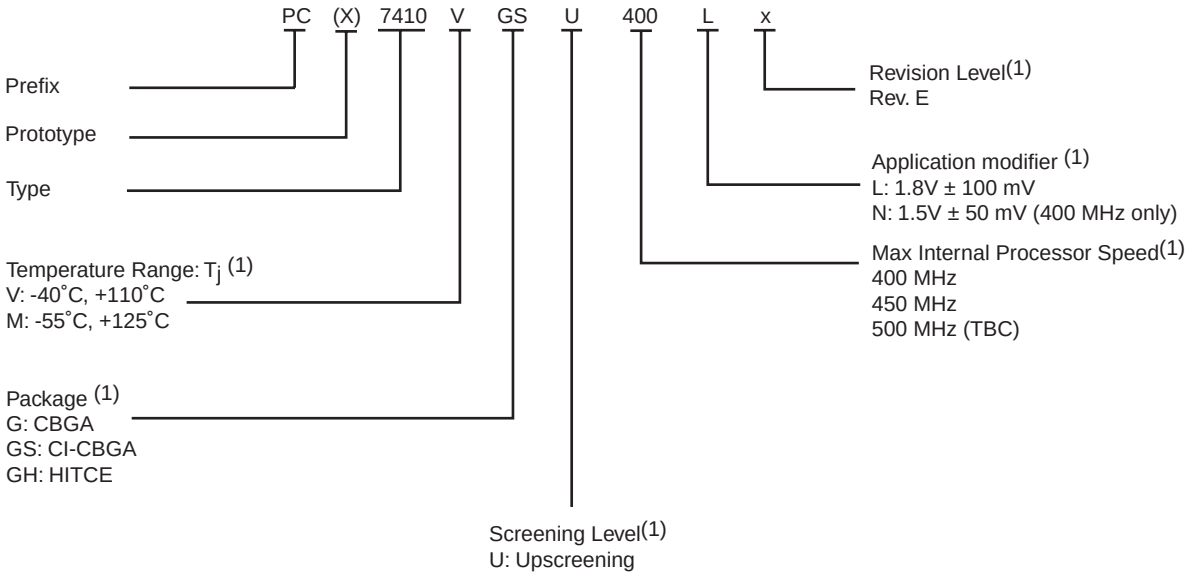

Note: 1. For availability of the different versions, contact your local Atmel sales office.

Document Revision History

Table 22 provides a revision history for this hardware specification.

Table 22. Document Revision History

Rev. No	Substantive Change(s)
D	Public release, includes Rev 1.1 changes.
	Section — added package capacitor values.
	Section "Thermal Management Assistant"— deleted
	Section “Pull-up Resistor Requirements” on page 43 — added recommendation that strong pull-up/down resistors be used on the PLL_CFG[0:3] signals.
	Table 11 on page 21— removed mode input setup and hold times. These inputs adhere to the general input setup and hold specifications.
	Figure 11 on page 23 — revised mode input diagram to show sample points around HRESET negation.
	Figure 32 on page 46 — added note 6 to emphasize that COP emulator and target board need to be able to drive $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ independently to the CPU.
	Section “PLL and DLL Power Supply Filtering” on page 40 — revised section for HCTE package. Added text and figure for AV_{DD} filter for the CBGA package.
	Section “Pull-up Resistor Requirements” on page 43 — removed $\overline{\text{AACK}}$, $\overline{\text{TEA}}$, and $\overline{\text{TS}}$ from control signals requiring pull-ups. Removed $\overline{\text{TBST}}$ from snooped transfer attribute list. $\overline{\text{TBST}}$ is an output and is not snooped.

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