Features

- **12.4 SPECint95, 8.4 SPECfp95 at 266 MHz (TSPC750A) with 1 MB L2 at 133 MHz**
- **11.5 SPECint95, 6.9 SPECfp95 at 266 MHz (TSPC740A)**
- **488 MIPS at 266 MHz**
- **Selectable Bus Clock (11 CPU Bus Dividers up to 8x)**
- **P_D Typical 4.2 W at 200 MHz, Full Operating Conditions**
- **Nap, Doze and Sleep Modes for Power Savings**
- **Superscalar (3 Instructions per Clock Cycle)**
- **4-GByte Direct Addressing Range**
- **64-bit Data and 32-bit Address Bus Interface**
- **32 KB Instruction and Data Cache**
- **Six Independent Execution Units and Two Register Files**
- **Write-back and Write-through Operations**
- **f_{int} max = 266 MHz**
- **f_{bus} max = 83.3 MHz**
- **Compatible CMOS Input / TTL Output**

Description

The TSPC750A and TSPC740A microprocessor (after named 750A/740A) are low-power implementations of the PowerPC Reduced Instruction Set Computer (RISC) architecture.

The 750A/740A microprocessors' designs are superscalar, capable of issuing three instructions per clock cycle into six independent execution units.

The 740A/750A microprocessors use a 2.6/3.3V CMOS process technology and maintain full interface compatibility with TTL devices.

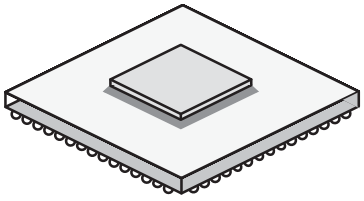
The 750A/740A provide four software controllable power-saving modes and a thermal assist unit management.

The 750A/740A microprocessors have separate 32K byte, physically-addressed instruction and data caches and differ only in that the 750A features a dedicated L2 cache interface with L2 on-chip tags.

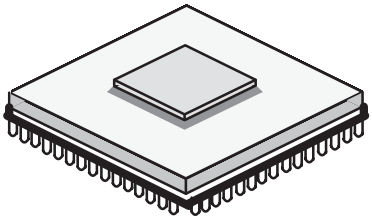
Both are software and bus-compatible with the PowerPC 603™ and PowerPC 604™ families, and are fully JTAG compliant.

The TSPC740A microprocessor is pin compatible with the TSPC603e family.

G suffix
CBGA255 and CBGA360
Ceramic Ball Grid Array



GS suffix
CI-CBGA255 and CI-CBGA360
Ceramic Ball Grid Array
with Solder Column Interposer (SCI)



PowerPC 750A/740A RISC Microprocessor Family PID8t-750A/740A Specification

TSPC750A/740A

Rev. 2128A–HIREL–01/02

Screening

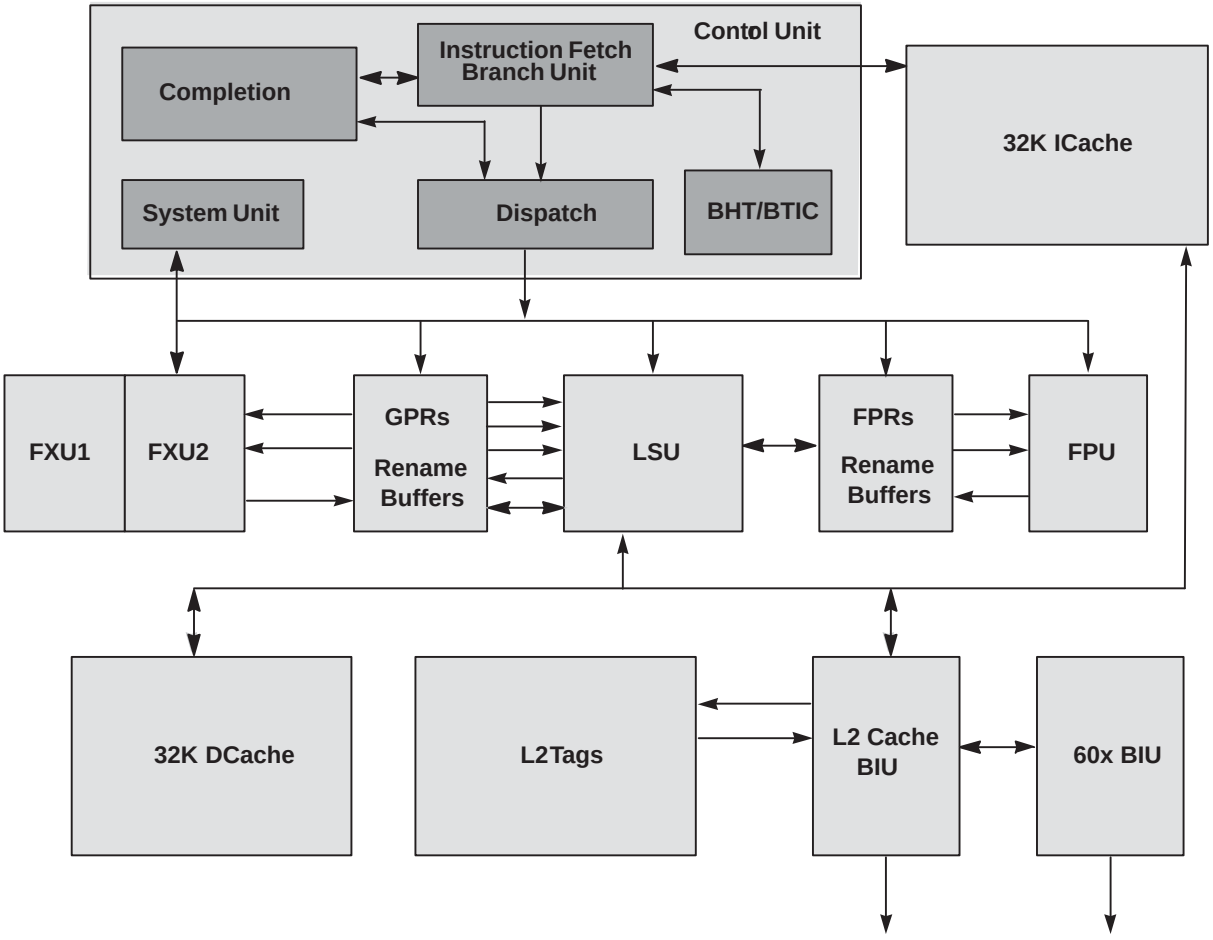
This product is manufactured in full compliance with:

- CBGA upscreenings based upon ATMEL-Grenoble standards
- Full military temperature range (Tc = -55°C,+125°C)
  Industrial temperature range (Tc = -40°C, +110°C)
- CI-CGA versions of TSPC740A and TSPC750A (planned)

Simplified Block Diagram

The TSPC750A is targeted for low power systems and supports the following power management features — doze, nap, sleep, and dynamic power management. The TSPC750A consists of a processor core and an internal L2 Tag combined with a dedicated L2 cache interface and a 60x bus.

Figure 1. TSPC750A Block Diagram



General Parameters

The general parameters of the 750A/740A are the following:

Technology	0.29 mm CMOS, five-layer metal
Die Size	7.56 mm x 8.79 mm (67 mm^2)
Transistor Count	6.35 million
Logic Design	Fully-static
Packages L2	740A: Surface mount 255 ceramic ball grid array (CBGA) and column interposer ceramic grid array CI-CGA without L2interface
	750A: Surface mount 360 ceramic ball grid array (CBGA) and column interposer ceramic grid array CI-CGA with L2 interface
Core Power Supply	2.6V ± 100 mV
I/O Power Supply	3.3V ± 5% V_{DC}

Features

Except L2 cache interface that is not supported by the PowerPC version, the major features implemented in the PowerPC 750A architecture are as follows:

Level 2 (L2) Cache Interface (not implemented on TSPC740A)

- Internal L2 cache controller and 4K-entry tags; external data SRAMs
- 256K, 512K, and 1-Mbyte 2-way set associative L2 cache support
- Copy-back or write-through data cache (on a page basis, or for all L2)
- 64-byte (256K/512K) and 128-byte (1-Mbyte) sectored line size
- Supports flow-through (reg-buf) synchronous burst SRAMs, pipelined (reg-reg) synchronous burst SRAMs, and pipelined (reg-reg) late-write synchronous burst SRAMs
- Core-to-L2 frequency divisors of ÷1, ÷1.5, ÷2, ÷2.5, and ÷3 supported

Branch Processing Unit

- Four instructions fetched per clock
- One branch processed per cycle (plus resolving 2 speculations)
- Up to 1 speculative stream in execution, 1 additional speculative stream in fetch
- 512-entry branch history table (BHT) for dynamic prediction
- 64-entry, 4-way set associative branch target instruction cache (BTIC) to minimize branch delay slots

Dispatch Unit

- Full hardware detection of dependencies (resolved in the execution units)
- Dispatch two instructions to six independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, or floating-point)
- Serialization control (predispatch, postdispatch, execution serialization)

Load/Store Unit

- One cycle load or store cache access (byte, half-word, word, double-word)
- Effective address generation
- Hits under misses (one outstanding miss)
- Single-cycle misaligned access within double word boundary
- Alignment, zero padding, sign extend for integer register file
- Floating-point internal format conversion (alignment, normalization)
- Sequencing for load/store multiples and string operations
- Store gathering
- Cache and TLB instructions

- Big- and little-endian byte addressing supported
- Misaligned little-endian support in hardware

Fixed-point Units

- Fixed-point unit 1 (FXU1)-multiply, divide, shift, rotate, arithmetic, logical
- Fixed-point unit 2 (FXU2)-shift, rotate, arithmetic, logical
- Single-cycle arithmetic, shift, rotate, logical
- Multiply and divide support (multi-cycle)
- Early out multiply

Bus Interface

- Compatible with 60x processor interface
- 32-bit address bus
- 64-bit data bus
- Bus-to-core frequency multipliers of 3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x, 7.5x, 8x supported

Decode

- Register file access
- Forwarding control
- Partial instruction decode

Floating-point Unit

- Support for IEEE-754 standard single- and double-precision floating-point arithmetic
- 3 cycle latency, 1 cycle throughput, single-precision multiply-add
- 3 cycle latency, 1 cycle throughput, double-precision add
- 4 cycle latency, 2 cycle throughput, double-precision multiply-add
- Hardware support for divide
- Hardware support for denormalized numbers
- Time deterministic non-IEEE mode

System Unit

- Executes CR logical instructions and miscellaneous system instructions
- Special register transfer instructions

Cache Structure

- 32K, 32-byte line, 8-way set associative instruction cache
- 32K, 32-byte line, 8-way set associative data cache
- Single-cycle cache access
- Pseudo-LRU replacement
- Copy-back or write-through data cache (on a page per page basis)
- Supports all PowerPC memory coherency modes
- Non-blocking instruction and data cache (one outstanding miss under hits)
- No snooping of instruction cache

Memory Management Unit

- 128 entry, 2-way set associative instruction TLB
- 128 entry, 2-way set associative data TLB
- Hardware reload for TLBs
- 4 instruction BATs and 4 data BATs
- Virtual memory support for up to 4 hexabytes (2^{52}) of virtual memory
- Real memory support for up to 4 gigabytes (2^{32}) of physical memory

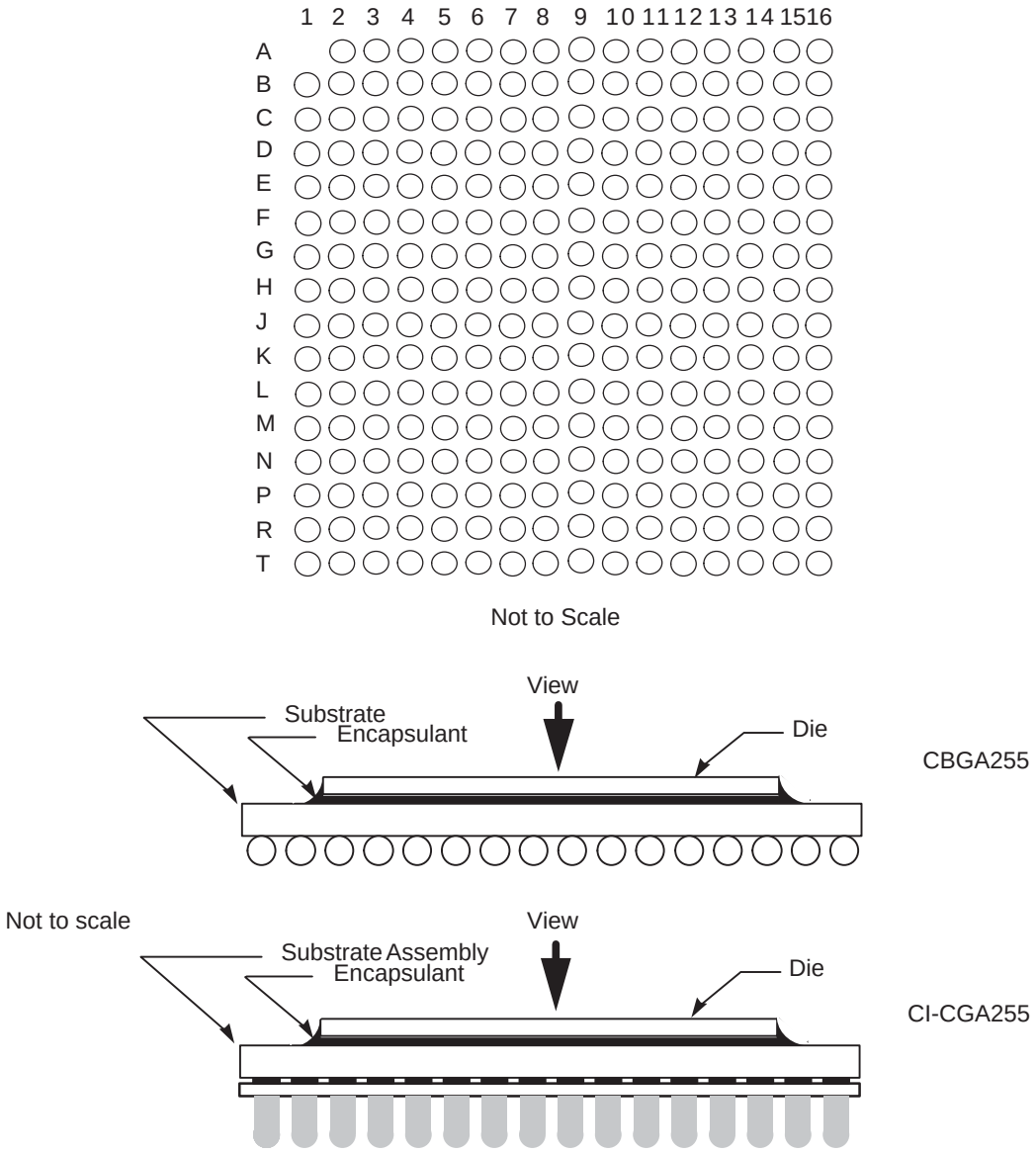
Testability	• LSSD scan design • JTAG interface
Integrated Power Management	• Low-power 2.6/3.3V design • Three static power saving modes: doze, nap, and sleep • Automatic dynamic power reduction when internal functional units are idle
Integrated Thermal Management Assist Unit	• On-chip thermal sensor and control logic • Thermal Management Interrupt for software regulation of junction temperature.
Reliability and Serviceability	• Parity checking on 60x and L2 cache buses

Pin Assignments

TSPC740A Package

The pinout of the TSPC740A, 255 CBGA and CI-CGA packages as viewed from the top surface.

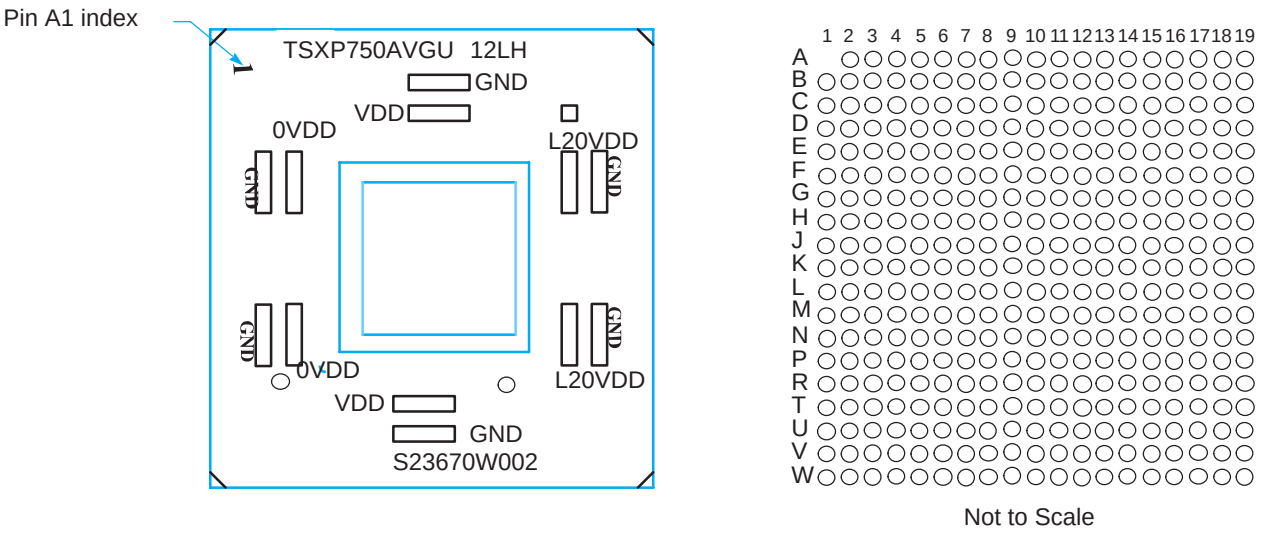
Figure 2. Pinout of TSPC740A, CBGA and CI-CGA Packages as Viewed from the Top Surface

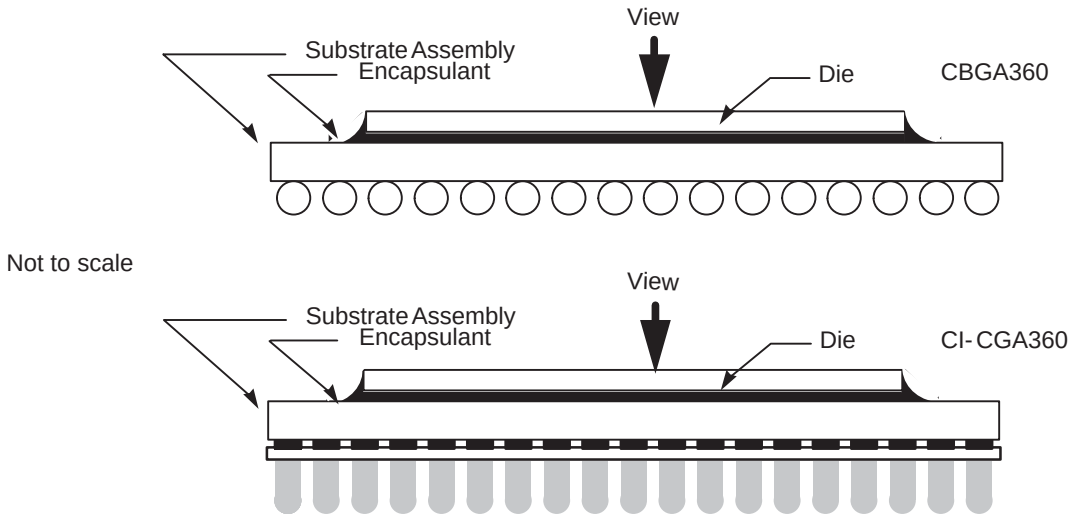


TSPC750A Package

The pinout of the TSPC750A, 360 CBGA and CI-CGA packages as viewed from the top surface.

Figure 3. Pinout of TSPC750A, CBGA and CI-BGA Packages as Viewed from the Top Surface





Pinout Listings

Table 1. Pinout Listing for the TSPC740A, 255 CBGA and CI-CGA Packages

Signal Name	Pin Number	Active	I/O
A[0-31]	C16, E4, D13, F2, D14, G1, D15, E2, D16, D4, E13, G2, E15, H1, E16, H2, F13, J1, F14, J2, F15, H3, F16, F4, G13, K1, G15, K2, H16, M1, J15, P1	High	I/O
$\overline{\text{AACK}}$	L2	Low	Input
$\overline{\text{ABB}}$	K4	Low	I/O
AP[0-3]	C1, B4, B3, B2	High	I/O
$\overline{\text{ARTRY}}$	J4	Low	I/O

Table 1. Pinout Listing for the TSPC740A, 255 CBGA and CI-CGA Packages (Continued)

Signal Name	Pin Number	Active	I/O
AVDD	A10	-	-
$\overline{BG}$	L1	Low	Input
$\overline{BR}$	B6	Low	Output
$\overline{CI}$	E1	Low	Output
$\overline{CKSTP\_IN}$	D8	Low	Input
$\overline{CKSTP\_OUT}$	A6	Low	Output
CLK_OUT	D7	-	Output
$\overline{DBB}$	J14	Low	I/O
$\overline{DBG}$	N1	Low	Input
$\overline{DBDIS}$	H15	Low	Input
$\overline{DBWO}$	G4	Low	Input
DH[0-31]	P14, T16, R15, T15, R13, R12, P11, N11, R11, T12, T11, R10, P9, N9, T10, R9, T9, P8, N8, R8, T8, N7, R7, T7, P6, N6, R6, T6, R5, N5, T5, T4	High	I/O
DL[0-31]	K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P3, N3, N4, R3, T1, T2, P4, T3, R4	High	I/O
DP[0-7]	M2, L3, N2, L4, R1, P2, M4, R2	High	I/O
$\overline{DRTRY}$	G16	Low	Input
$\overline{GBL}$	F1	Low	I/O
GND	C5, C12, E3, E6, E8, E9, E11, E14, F5, F7, F10, F12, G6, G8, G9, G11, H5, H7, H10, H12, J5, J7, J10, J12, K6, K8, K9, K11, L5, L7, L10, L12, M3, M6, M8, M9, M11, M14, P5, P12	-	-
$\overline{HRESET}$	A7	Low	Input
$\overline{INT}$	B15	Low	Input
L1_TSTCLK(1)	D11	High	Input
L2_TSTCLK(1)	D12	High	Input
LSSD_MODE(1)	B10	Low	Input
$\overline{MCP}$	C13	Low	Input
NC (No-Connect)	B7, B8, C3, C6, C8, D5, D6, H4, J16, A4, A5, A2, A3, B1, B5	-	-
OVDD	C7, E5, E7, E10, E12, G3, G5, G12, G14, K3, K5, K12, K14, M5, M7, M10, M12, P7, P10	-	-
PLL_CFG[0-3]	A8, B9, A9, D9	High	Input
$\overline{QACK}$	D3	Low	Input
$\overline{QREQ}$	J3	Low	Output
$\overline{RSRV}$	D1	Low	Output
$\overline{SMI}$	A16	Low	Input
$\overline{SRESET}$	B14	Low	Input
SYSCLK	C9	-	Input

Table 1. Pinout Listing for the TSPC740A, 255 CBGA and CI-CGA Packages (Continued)

Signal Name	Pin Number	Active	I/O
$\overline{TA}$	H14	Low	Input
TBEN	C2	High	Input
$\overline{TBST}$	A14	Low	I/O
TCK	C11	High	Input
TDI	A11	High	Input
TDO	A12	High	Output
$\overline{TEA}$	H13	Low	Input
$\overline{TLBISYNC}$	C4	Low	Input
TMS	B11	High	Input
$\overline{TRST}$	C10	Low	Input
$\overline{TS}$	J13	Low	I/O
TSIZ[0-2]	A13, D10, B12	High	Output
TT[0-4]	B13, A15, B16, C14, C15	High	I/O
$\overline{WT}$	D2	Low	Output
VDD 2	F6, F8, F9, F11, G7, G10, H6, H8, H9, H11, J6, J8, J9, J11, K7, K10, L6, L8, L9, L11	-	-
VOLTDET 3	F3	High	Output

Notes: 1. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
2. OV_{DD} inputs supply power to the I/O drivers and V_{DD} inputs supply power to the processor core.
3. Internally tied to GND in the TSPC740A CBGA package to indicate to the power supply that a low-voltage processor is present. This signal is not a power supply input.

Table 2. Pinout Listing for the TSPC750A, 360 CBGA and CI-CGA Packages

Signal Name	Pin Number	Active	I/O
A[0-31]	A13, D2, H11, C1, B13, F2, C13, E5, D13, G7, F12, G3, G6, H2, E2, L3, G5, L4, G4, J4, H7, E1, G2, F3, J7, M3, H3, J2, J6, K3, K2, L2	High	I/O
$\overline{AACK}$	N3	Low	Input
$\overline{ABB}$	L7	Low	I/O
AP[0-3]	C4, C5, C6, C7	High	I/O
$\overline{ARTRY}$	L6	Low	I/O
AVDD	A8	-	-
$\overline{BG}$	H1	Low	Input
$\overline{BR}$	E7	Low	Output
CKSTP_OUT	D7	High	Output
$\overline{CI}$	C2	Low	Output
CKSTP_IN	B8	High	Input
CLKOUT	E3	-	Output
$\overline{DBB}$	K5	Low	I/O

Table 2. Pinout Listing for the TSPC750A, 360 CBGA and CI-CGA Packages (Continued)

Signal Name	Pin Number	Active	I/O
$\overline{\text{DBDIS}}$	G1	Low	Input
$\overline{\text{DBG}}$	K1	Low	Input
$\overline{\text{DBWO}}$	D1	Low	Input
DH[0-31]	W12, W11, V11, T9, W10, U9, U10, M11, M9, P8, W7, P9, W9, R10, W6, V7, V6, U8, V9, T7, U7, R7, U6, W5, U5, W4, P7, V5, V4, W3, U4, R5	High	I/O
DL[0-31]	M6, P3, N4, N5, R3, M7, T2, N6, U2, N7, P11, V13, U12, P12, T13, W13, U13, V10, W8, T11, U11, V12, V8, T1, P1, V1, U1, N1, R2, V3, U3, W2	High	I/O
DP[0-7]	L1, P2, M2, V2, M1, N2, T3, R1	High	I/O
$\overline{\text{DRTRY}}$	H6	Low	Input
$\overline{\text{GBL}}$	B1	Low	I/O
GND	D10, D14, D16, D4, D6, E12, E8, F4, F6, F10, F14, F16, G9, G11, H5, H8, H10, H12, H15, J9, J11, K4, K6, K8, K10, K12, K14, K16, L9, L11, M5, M8, M10, M12, M15, N9, N11, P4, P6, P10, P14, P16, R8, R12, T4, T6, T10, T14, T16	-	-
$\overline{\text{HRESET}}$	B6	Low	Input
$\overline{\text{INT}}$	C11	Low	Input
L1_TSTCLK(1)	F8	High	Input
L2ADDR[0-16]	L17, L18, L19, M19, K18, K17, K15, J19, J18, J17, J16, H18, H17, J14, J13, H19, G18	High	Output
L2AVDD	L13	-	-
L2CE	P17	Low	Output
L2CLKOUTA	N15	Low	Output
L2CLKOUTB	L16	Low	Output
L2DATA[0-63]	U14, R13, W14, W15, V15, U15, W16, V16, W17, V17, U17, W18, V18, U18, V19, U19, T18, T17, R19, R18, R17, R15, P19, P18, P13, N14, N13, N19, N17, M17, M13, M18, H13, G19, G16, G15, G14, G13, F19, F18, F13, E19, E18, E17, E15, D19, D18, D17, C18, C17, B19, B18, B17, A18, A17, A16, B16, C16, A14, A15, C15, B14, C14, E13	High	I/O
L2DP[0-7]	V14, U16, T19, N18, H14, F17, C19, B15	High	I/O
L2OVDD	D15, E14, E16, H16, J15, L15, M16, P15, R14, R16, T15, F15	-	-
L2SYNC_IN	L14	High	Input
L2SYNC_OUT	M14	High	Output
L2_TSTCLK(1)	F7	High	Input
L2WE	N16	Low	Output
L2ZZ	G17	High	Output
LSSD_MODE(1)	F9	Low	Input
$\overline{\text{MCP}}$	B11	Low	Input
NC (No-Connect)	B3, B4, B5, A19, W19, W1, K9, K11(4), K19(4)	-	-
OVDD	D5, D8, D12, E4, E6, E9, E11, F5, H4, J5, L5, M4, P5, R4, R6, R9, R11, T5, T8, T12	-	-

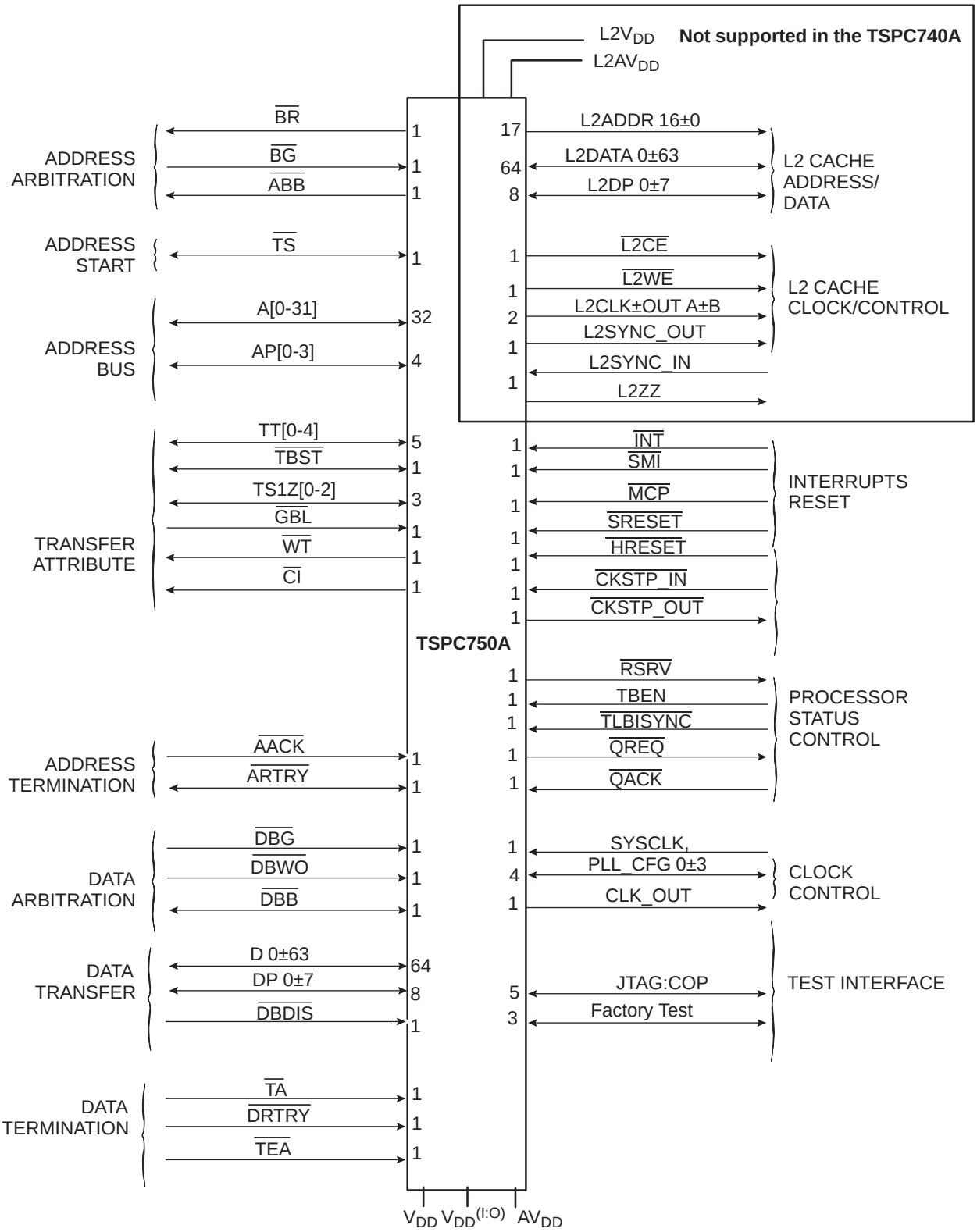
Table 2. Pinout Listing for the TSPC750A, 360 CBGA and CI-CGA Packages (Continued)

Signal Name	Pin Number	Active	I/O
PLL_CFG[0-3]	A4, A5, A6, A7	High	Input
$\overline{\text{QACK}}$	B2	Low	Input
$\overline{\text{QREQ}}$	J3	Low	Output
$\overline{\text{RSRV}}$	D3	Low	Output
$\overline{\text{SMI}}$	A12	Low	Input
$\overline{\text{SRESET}}$	E10	Low	Input
SYSCLK	H9	-	Input
$\overline{\text{TA}}$	F1	Low	Input
TBEN	A2	High	Input
$\overline{\text{TBST}}$	A11	Low	I/O
TCK	B10	High	Input
TDI	B7	High	Input
TDO	D9	High	Output
$\overline{\text{TEA}}$	J1	Low	Input
$\overline{\text{TLBISYNC}}$	A3	Low	Input
TMS	C8	High	Input
$\overline{\text{TRST}}$	A10	Low	Input
$\overline{\text{TS}}$	K7	Low	I/O
TSIZ[0-2]	A9, B9, C9	High	Output
TT[0-4]	C10, D11, B12, C12, F11	High	I/O
$\overline{\text{WT}}$	C3	Low	Output
VDD (2)	G8, G10, G12, J8, J10, J12, L8, L10, L12, N8, N10, N12	-	-
VOLTDET (3)	K13	High	Output

Notes:
1. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
2. OV_{DD} inputs supply power to the I/O drivers and V_{DD} inputs supply power to the processor core.
3. Internally tied to L2OVDD in the TSPC750A packages ATMEL-Grenoble to indicate the power present at the L2 cache interface. This signal is not a power supply input. Caution: this is different from the TSPC740A packages.
4. These pins are reserved for potential future use as additional L2 address pins.

Signal Description

Figure 4. TSPC750A Microprocessor Signal Groups



Scope

This drawing describes the specific requirements for the microprocessor TSPC750A, in compliance with ATMEL-Grenoble standard screening.

Applicable Documents

1. MIL-STD-883: Test methods and procedures for electronics.
2. MIL-PRF-38535 appendix A: General specifications for microcircuits.

Requirements

General

The microcircuits are in accordance with the applicable documents and as specified herein.

Design and Construction

Terminal Connections

Depending on the package, the terminal connections shall be is shown in Table 1, Table 2 and Figure 4.

Absolute Maximum Rating

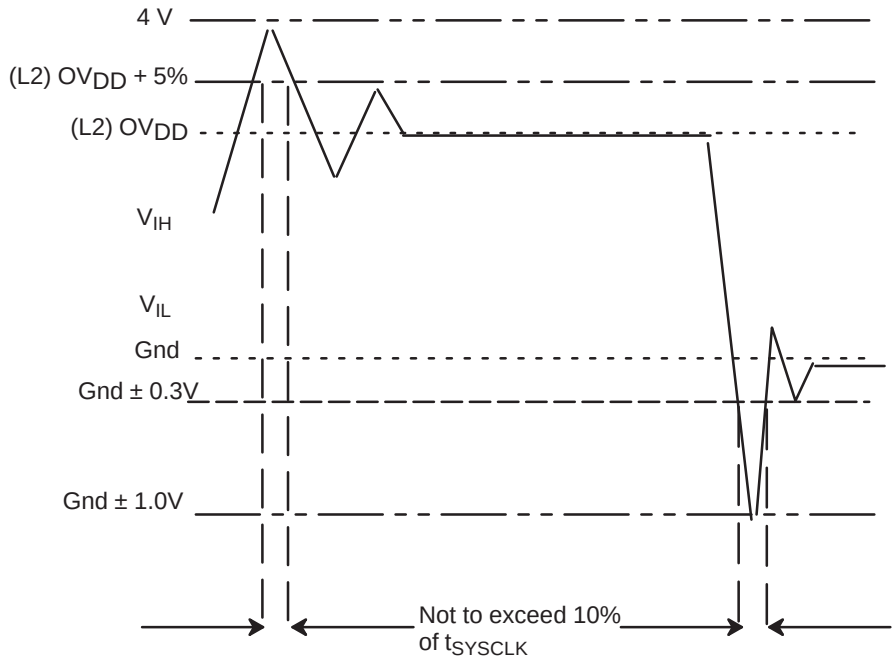
Table 3. Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	-0.3 to 2.75 (4)	V
PLL Supply Voltage	AV_{DD}	-0.3 to 2.75 (4)	V
L2 DLL Supply Voltage	$L2AV_{DD}$	-0.3 to 2.75 (4)	V
60x Bus Supply Voltage	OV_{DD}	-0.3 to 3.6 (3.5)	V
L2 Bus Supply Voltage	$L2OV_{DD}$	-0.3 to 3.6 (3.5)	V
Input Voltage	V_{IN}	-0.3 to 3.6 (2)	V
Storage Temperature Range	T_{STG}	-55 to 150	°C

Notes:
1. Functional and tested operating conditions are given in Table 4. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. Caution: V_{IN} must not exceed OV_{DD} by more than 0.3V at any time including during power-on reset.
3. Caution: OV_{DD} must not exceed V_{DD}/AV_{DD} by more than 1.2V at any time including during power-on reset.
4. Caution: V_{DD}/AV_{DD} must not exceed OV_{DD} by more than 0.4V at any time including during power-on reset.
5. Caution: V_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 5.

Figure 5 shows the allowable undershoot and overshoot voltage on the TSPC750A and TSPC 740A.

Figure 5. Overshoot/Undershoot Voltage



Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Characteristic	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	2.5 to 2.7	V
PLL Supply Voltage	AV_{DD}	2.5 to 2.7	V
L2 DLL Supply Voltage	$L2AV_{DD}$	2.5 to 2.7	V
60x Bus Supply Voltage	OV_{DD}	3.135 to 3.465	V
L2 Bus Supply Voltage	$L2OV_{DD}$	3.135 to 3.465	V
Input Voltage	V_{IN}	GND to OV_{DD}	V
Junction Temperature	T_j	-55 to +125	°C

Note: 1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Thermal Characteristics

Table 5. Package Thermal Characteristics

Characteristic	Symbol	Value	Rating
CBGA and CI-CGA packages thermal resistance, junction-to-case thermal resistance (typical)	θ_{JC}	0.03	°C/W
CBGA package thermal resistance, die junction-to-lead thermal resistance (typical)	θ_{JB}	3.8	°C/W
CI-CGA package thermal resistance, die junction-to-lead thermal resistance (typical)	θ_{JB}	4	°C/W

The board designer can choose between several types of heat sinks to place on the TSPC750A. There are several commercially-available heat sinks for the TSPC750A provided by the following vendors:

For the exposed-die packaging technology, shown in Table 5, the intrinsic conduction thermal resistance paths are as follows:

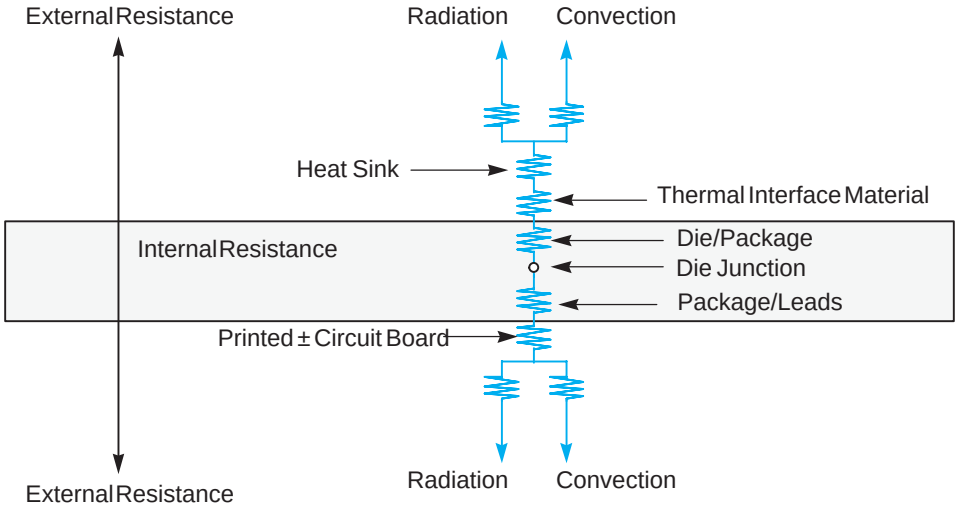
- The die junction-to-case (or top-of-die for exposed silicon) thermal resistance
- The die junction-to-ball thermal resistance

Figure 6 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Heat generated on the active side of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Since the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the heat sink attach material and the heat sink conduction/convective thermal resistances are the dominant terms.

Figure 6. C4 Package with Heat Sink Mounted to a Printed-Circuit Board



(Note the internal versus external package resistance)

Thermal Management Assistance

The TSPC750A incorporates a thermal management assist unit (TAU) composed of a thermal sensor, digital-to-analog converter, comparator, control logic, and dedicated special-purpose registers (SPRs). Specifications for the thermal sensor portion of the TAU are found in Table 6. More information on the use of this feature is given in the MPC750A RISC Microprocessor User's manual.

Table 6. Thermal Sensor Specifications

$V_{DD} = AV_{DD} = L2AV_{DD} = 2.6\ V_{DC} \pm 100$ mV, $OV_{DD} = L2OV_{DD} = 3.3 \pm 5\%\ V_{DC}$, GND = 0 V_{DC}, $0 \le T_j < +125°C$

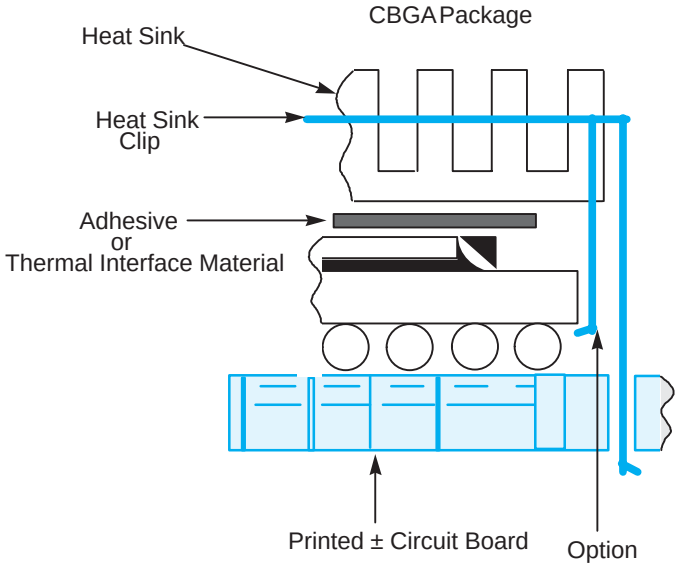
Num	Characteristic	Min	Max	Unit	Notes
1	Temperature Range	0	127	°C	1
2	Comparator Settling Time	20	-	µs	2
3	Resolution	4	-	°C	3

Notes:
1. The temperature is the junction temperature of the die. The thermal assist unit's raw output does not indicate an absolute temperature, but it must be interpreted by software to derive the absolute junction temperature. For information about the use and calibration of the TAU, see the Motorola application note AN1800/D "programming the thermal Assist Unit in the MPC750A Microprocessor. This specification reflects the temperature span supported by design.
2. The comparator settling time value must be converted into the number of CPU clocks that need to be written into the THRM3 SPR.
3. Guaranteed by design and characterization.

Thermal Management Information

This section provides thermal management information for the ceramic ball grid array (CBGA) package for air-cooled applications. Proper thermal control design is primarily dependent upon the system-level design the heat sink, airflow and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods-adhesive, spring clip to holes in the printed circuit board or package, and mounting clip and screw assembly; see Figure 7. This spring force should not exceed 5.5 pounds of force.

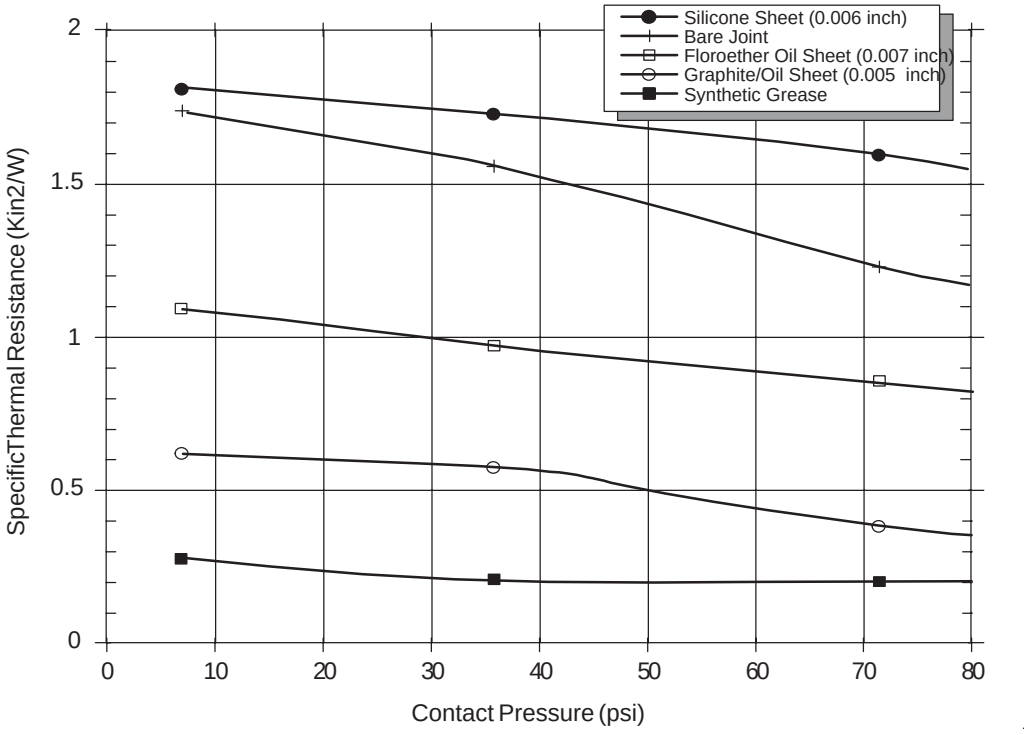
Figure 7. Package Exploded Cross-Sectional View with Several Heat Sink Options



Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

Adhesives and Thermal Interface Materials

Figure 8. Thermal Performance of Select Thermal Interface Material



A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 8 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately 7 times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 7). This spring force should not exceed 5.5 pounds of force. Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure.

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based upon high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements.

Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_a + T_r + (\theta_{jc} + \theta_{int} + \theta_{sa}) * P_d$$

Where:

T_j is the die-junction temperature

T_a is the inlet cabinet ambient temperature

T_r is the air temperature rise within the computer cabinet

θ_{jc} is the junction-to-case thermal resistance

θ_{int} is the adhesive or interface material thermal resistance

θ_{sa} is the heat sink base-to-ambient thermal resistance

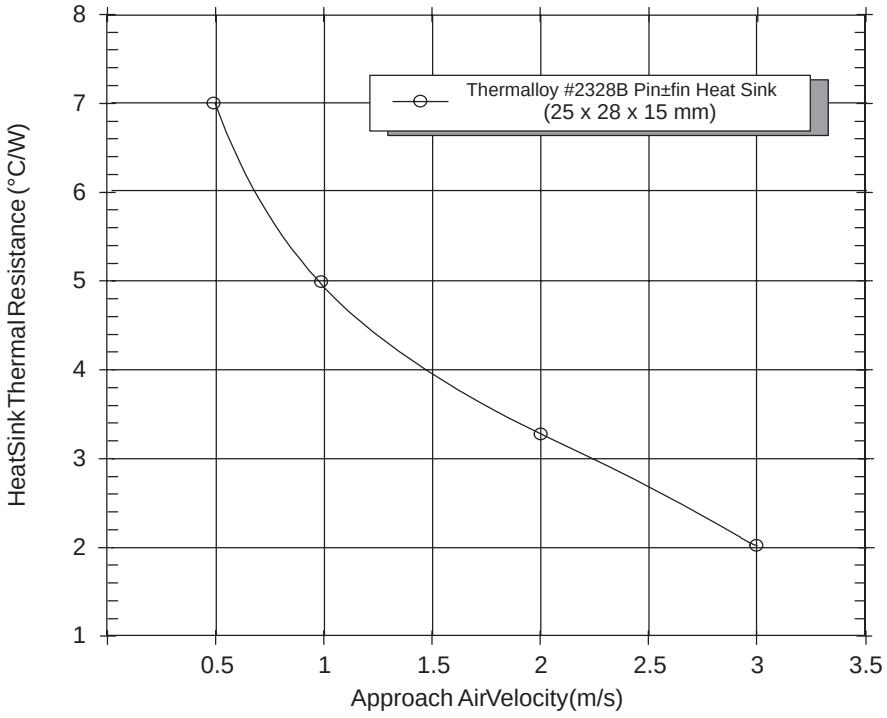
P_d is the power dissipated by the device

During operation the die-junction temperatures (T_j) should be maintained less than the value specified in Table 4. The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_a) may range from 30 to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5 to 10°C. The thermal resistance of the thermal interface material (θ_{int}) is typically about 1°C/W. Assuming a T_a of 30°C, a T_r of 5°C, a CBGA package θ_{jc} = 2.2, and a power consumption (P_d) of 4.5 watts, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (2.2°C/W + 1.0°C/W + \theta_{sa}) * 4.5\ W$

For a Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance (θ_{sa}) versus airflow velocity is shown in Figure 9.

Figure 9. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity



Assuming an air velocity of 0.5 m/s, we have an effective R_{sa} of 7°C/W, thus

T_j = 30°C + 5°C + (2.2°C/W +1.0°C/W + 7°C/W) * 4.5 W,

resulting in a die-junction temperature of approximately 81°C which is well within the maximum operating temperature of the component.

Other heat sinks offered by Chip Coolers, IERC, Thermalloy, Wakefield Engineering, and Aavid Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need air flow.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature, is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature-airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as, system-level designs. To expedite system-level thermal analysis, several "compact" thermal-package models are available within FLOTHERM®. These are available upon request.

Power Consideration

Power Management

The TSPC750A provides four power modes, selectable by setting the appropriate control bits in the MSR and HIDO registers. The four power modes are as follows:

- Full-power: This is the default power state of the TSPC750A. The TSPC750A is fully powered and the internal functional units are operating at the full processor clock speed. If the dynamic power management mode is enabled, functional units that are idle will automatically enter a low-power state without affecting performance, software execution, or external hardware.
- Doze: All the functional units of the TSPC750A are disabled except for the time base/decrementer registers and the bus snooping logic. When the processor is in doze mode, an external asynchronous interrupt, a system management interrupt, a decrementer exception, a hard or soft reset, or machine check brings the TSPC750A into the full-power state. The TSPC750A in doze mode maintains the PLL in a fully powered state and locked to the system external clock input (SYSCLK) so a transition to the full-power state takes only a few processor clock cycles.
- Nap: The nap mode further reduces power consumption by disabling bus snooping, leaving only the time base register and the PLL in a powered state. The TSPC750A returns to the full-power state upon receipt of an external asynchronous interrupt, a system management interrupt, a decrementer exception, a hard or soft reset, or a machine check input ($\overline{\text{MCP}}$). A return to full-power state from a nap state takes only a few processor clock cycles. When the processor is in nap mode, if $\overline{\text{QACK}}$ is negated, the processor is put in doze mode to support snooping.

- Sleep: Sleep mode minimizes power consumption by disabling all internal functional units, after which external system logic may disable the PPL and SUSCLK. Returning the TSPC750A to the full-power state requires the enabling of the PPL and SYSCLK, followed by the assertion of an external asynchronous interrupt, a system management interrupt, a hard or soft reset, or a machine check input ($\overline{MCP}$) signal after the time required to relock the PPL.

Power Dissipation

Table 7. Power Consumption

$V_{DD} = AV_{DD} = L2AV_{DD} = 2.6\ V_{DC} \pm 100$ mV, $OV_{DD} = L2OV_{DD} = 3.3 \pm 5\%\ V_{DC}$, GND = 0 V_{DC}, $-55 \le Tj < 125°C$

	Processor (CPU) Frequency				
	200 MHz	233 MHz	266 MHz	Unit	Notes
Full-On Mode					
Typical	4.2	5.0	5.7	W	1, 3, 4
Maximum	6.0	7.0	7.9	W	1, 2, 4
Doze Mode					
Maximum	1.6	1.8	2.1	W	1, 2
Nap Mode					
Maximum	250	250	250	mW	1, 2
Sleep Mode					
Maximum	300	300	300	mW	1, 2
Sleep Mode—PLL and DLL Disabled					
Typical	30	50	50	mW	1, 3
Maximum	60	100	100	mW	1, 2

Notes:
1. These values apply for all valid 60x bus and L2 bus ratios. The values do not include I/O Supply Power (OV_{DD} and $L2OV_{DD}$) or PLL/DLL supply power (AV_{DD} and $L2AV_{DD}$). OV_{DD} and $L2OV_{DD}$ power is system dependent, but is typically <10% of V_{DD} power. Worst case power consumption for AV_{DD} = 15 mw and $L2AV_{DD}$ = 15 mW.
2. Maximum power is measured at V_{DD} = 2.7V
3. Typical power is an average value measured at $V_{DD} = AV_{DD} = L2AV_{DD}$ = 2.6V, $OV_{DD} = L2OV_{DD}$ = 3.3V in a system executing typical applications and benchmark sequences.
4. Full-On mode is measured using worst-case instruction sequence.

Electrical Characteristics

Static Characteristics

Table 8. DC Electrical Specifications

$V_{DD} = AV_{DD} = L2AV_{DD} = 2.6\ V_{DC} \pm 100$ mV, $OV_{DD} = L2OV_{DD} = 3.3 \pm 5\%\ V_{DC}$, GND = 0 V_{DC}, $-55 \le T_j < 125°C$

Characteristic	Symbol	Min	Max	Unit	Notes
Input High Voltage (all inputs except SYSCLK)	V_{IH}	2	3.465	V	1,2
Input Low Voltage (all inputs except SYSCLK)	V_{IL}	GND	0.8	V	
SYSCLK Input High Voltage	CV_{IH}	2.4	3.465	V	1

Table 8. DC Electrical Specifications

$V_{DD} = AV_{DD} = L2AV_{DD} = 2.6\ V_{DC} \pm 100$ mV, $OV_{DD} = L2OV_{DD} = 3.3 \pm 5\%\ V_{DC}$, GND = 0 V_{DC}, $-55 \le T_j < 125°C$

Characteristic	Symbol	Min	Max	Unit	Notes
SYSCLK Input Low Voltage	CV_{IL}	GND	0.4	V	
Input Leakage Current, $V_{IN} = OV_{DD}$	I_{in}	-	30	µA	1, 2
Hi-Z (off-state) Leakage Current, $V_{IN} = OV_{DD}$	I_{TSI}	-	30	µA	1, 2,4
Output High Voltage, I_{OH} = -6 mA	V_{OH}	2.4	-	V	
Output Low Voltage, I_{OL} = 6 mA	V_{OL}	-	0.4	V	
Capacitance, V_{IN} = 0V, f = 1 MHz	C_{in}	-	5.0	pF	2, 3

Notes:
1. For 60x bus signals, the reference is OV_{DD} while $L2OV_{DD}$ is the reference for the L2 bus signals.
2. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK) and IEEE 1149.1 boundary scan (JTAG) signals.
3. Capacitance is periodically sampled rather than 100% tested.
4. The leakage is measured for nominal OV_{DD} and V_{DD}, or both OV_{DD} and V_{DD} must vary in the same direction (for example, both OV_{DD} and V_{DD} vary by either +5% or -5%).

Dynamic Characteristics

After fabrication, parts are sorted by maximum processor core frequency as shown in "Clock AC Specifications" and tested for conformance to the AC specifications for that frequency. These specifications are for 200, 233, and 266 MHz processor core frequencies. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0-3] signals. Parts are sold by maximum processor core frequency.

Clock AC Specifications

Table 9 provides the clock AC timing specifications as defined in Figure 9.

Table 9. Clock AC Timing Specifications

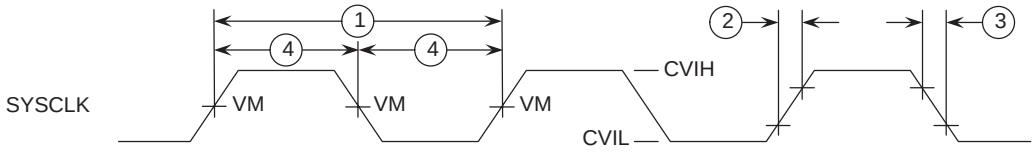
$V_{DD} = AV_{DD} = L2AV_{DD} = 2.6\ V_{DC} \pm 100$ mV, $OV_{DD} = L2OV_{DD} = 3.3 \pm 5\%\ V_{DC}$, GND = 0 V_{DC}, $-55 \le T_j < 125°C$

		200 MHz		233 MHz		266 MHz			
Num	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Notes
	Processor Frequency	150	200	150	233	150	266	MHz	
	VCO Frequency	300	400	300	466	300	533	MHz	
	SYSCLK Frequency	25	83.3	25	83.3	25	83.3	MHz	1
1	SYSCLK Cycle Time	12	40	12	40	12	40	ns	
2, 3	SYSCLK Rise and Fall Time	-	2	-	2	-	2	ns	2
4	SYSCLK Duty Cycle Measured at 1.4V	40	60	40	60	40	60	%	3
	SYSCLK Jitter	-	±150	-	±150	-	±150	ps	4
	Internal PLL Relock Time	-	100	-	100	-	100	µs	5

Notes:
1. **Caution**: The SYSCLK frequency and PLL_CFG[0-3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0-3] signal description in "PLL Configuration," for valid PLL_CFG[0-3] settings
2. Rise and fall times for the SYSCLK input are measured from 0.4 to 2.4V.
3. Timing is guaranteed by design and characterization.
4. The total input jitter (short term and long term combined) must be under ±150 ps.
5. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

Figure 10 provides the SYSCLK input timing diagram.

Figure 10. SYSCLK Input Timing Diagram



VM = Midpoint Voltage (1.4V)

60x Bus Input AC Specifications

Table 10 provides the 60x bus input AC timing specifications for the TSPC750A as defined in Figure 11 and Figure 12. Input timing specifications for the L2 bus are provided in L2 Bus Input AC Specifications.

Table 10. 60x Bus Input AC Timing Specifications[1]

V_{DD} =AV_{DD} = $L2AV_{DD}$ = 2.6 V_{DC} ± 100 mV, OV_{DD} = $L2OV_{DD}$ = 3.3 ± 5% V_{DC}, GND = 0 V_{DC}, -55 ≤ T_j < 125°C

Num	Characteristic	200, 233, 266 MHz		Unit	Notes
		Min	Max		
10a	Address/Data/Transfer Attribute Inputs Valid to SYSCLK (Input Setup)	2.5	-	ns	2
10b	All Other Inputs Valid to SYSCLK (Input Setup)	3.0	-	ns	3
10c	Mode select input setup to $\overline{\text{HRESET}}$ ($\overline{\text{DRTRY}}$, $\overline{\text{TLBISYNC}}$)	8	-	t_{sysclk}	4, 5, 6, 7
11a	SYSCLK to Address/Data/Transfer Attribute Inputs Invalid (Input Hold)	1.0	-	ns	2
11b	SYSCLK to All Other Inputs Invalid (Input Hold)	1.0	-	ns	3
11c	$\overline{\text{HRESET}}$ to mode select input hold ($\overline{\text{DRTRY}}$, $\overline{\text{TLBISYNC}}$)	0	-	ns	4, 6, 7

Notes:
1. All input specifications are measured from the TTL level (0.8 to 2.0V) of the signal in question to the 1.4V of the rising edge of the input SYSCLK. Input and output timings are measured at the pin.
2. Address/Data/Transfer Attribute inputs are composed of the following — A[0-31], AP[0-3], TT[0-4], $\overline{\text{TBST}}$, TSIZ[0-2], $\overline{\text{GBL}}$, DH[0-31], DL[0-31], DP[0-7].
3. All other signal inputs are composed of the following-$\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{BG}}$, $\overline{\text{AACK}}$, $\overline{\text{DBG}}$, $\overline{\text{DBWO}}$, $\overline{\text{TA}}$, $\overline{\text{DRTRY}}$, $\overline{\text{TEA}}$, $\overline{\text{DBDIS}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, $\overline{\text{INT}}$, $\overline{\text{SMI}}$, $\overline{\text{MCP}}$, TBEN, QACK, $\overline{\text{TLBISYNC}}$.
4. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$ (see Figure 12).
5. t_{sysclk} is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
6. Guaranteed by design and characterization.
7. This specification is for configuration mode select only. Also note that the $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL re-lock time during the power-on reset sequence.

Figure 11 provides the input timing diagram for the TSPC750A.

Figure 11. Input Timing Diagram

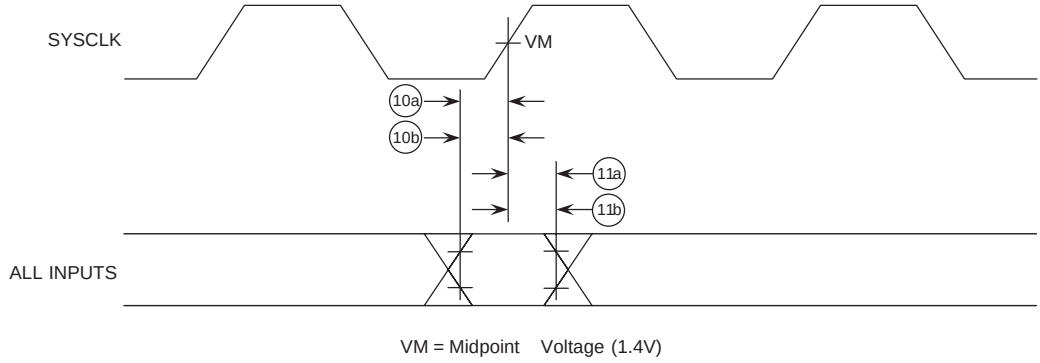
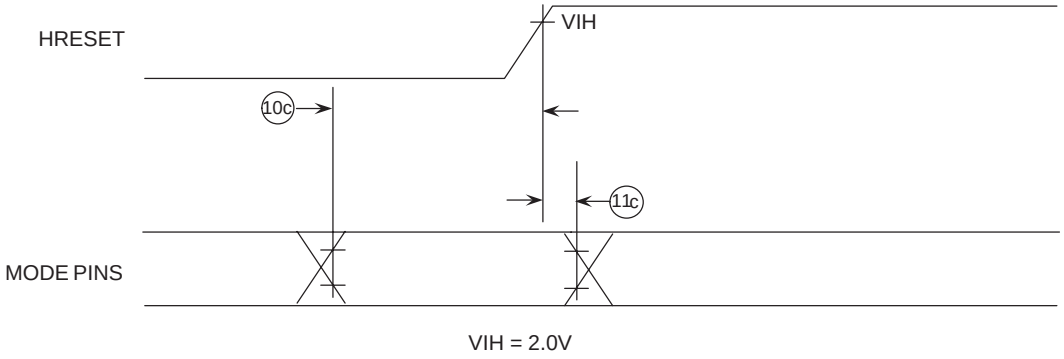


Figure 12 provides the mode select input timing diagram for the TSPC750A.

Figure 12. Mode Select Input Timing Diagram



60x Bus Output AC Specifications

Table 11 provides the 60x bus output AC timing specifications for the TSPC750A as defined in Figure 13. Output timing specifications for the L2 bus are provided in L2 Bus Output AC Specifications.

Table 11. 60x Bus Output AC Timing Specifications (1)

$V_{DD} = AV_{DD} = L2AV_{DD} = 2.6\ V_{DC} \pm 100$ mV, $OV_{DD} = L2OV_{DD} = 3.3 \pm 5\%\ V_{DC}$, GND = 0 V_{DC}, $-55 \le T_j < 125°C$, CL = 50 pF(2)

Num	Characteristic	200, 233, 266 MHz		Unit	Notes
		Min	Max		
12	SYSCLK to Output Driven (Output Enable Time)	0.5	-	ns	
13	SYSCLK to Output Valid (TS, ABB, $\overline{\text{ARTRY}}$, $\overline{\text{DBB}}$)	-	6.5	ns	5
14	SYSCLK to all other Outputs Valid (all except TS, $\overline{\text{ABB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{DBB}}$)	-	6.5	ns	5
15	SYSCLK to Output Invalid (Output Hold)	1.0	-	ns	3
16	SYSCLK to Output High Impedance (all except $\overline{\text{ABB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{DBB}}$)	-	6.0	ns	8
17	SYSCLK to $\overline{\text{ABB}}$, $\overline{\text{DBB}}$ High Impedance after precharge	-	1.0	t_{sysclk}	4, 6, 8
18	SYSCLK to $\overline{\text{ARTRY}}$ High Impedance before precharge	-	5.5	ns	8

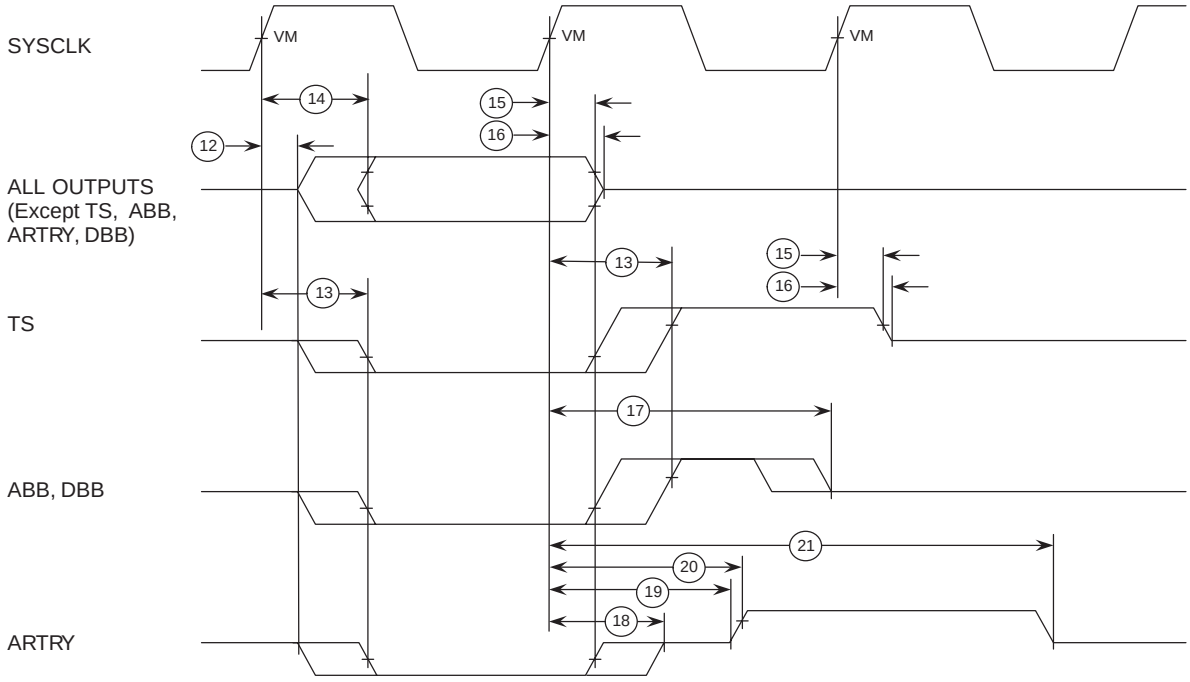
Table 11. 60x Bus Output AC Timing Specifications (Continued)[1]

$V_{DD} = AV_{DD} = L2AV_{DD} = 2.6\ V_{DC} \pm 100$ mV, $OV_{DD} = L2OV_{DD} = 3.3 \pm 5\%\ V_{DC}$, GND = 0 V_{DC}, $-55 \le T_j < 125°C$, CL = 50 pF(2)

Num	Characteristic	200, 233, 266 MHz		Unit	Notes
		Min	Max		
19	SYSCLK to $\overline{\text{ARTRY}}$ Precharge Enable	$0.2*t_{sysclk}$ +1.0	-	ns	3, 4, 7
20	Maximum Delay to $\overline{\text{ARTRY}}$ Precharge	-	1	t_{sysclk}	4, 7
21	SYSCLK to $\overline{\text{ARTRY}}$ High Impedance After Precharge	-	2	t_{sysclk}	4, 7, 8

Notes:
1. All output specifications are measured from the 1.4V of the rising edge of SYSCLK to TTL level (0.8 V or 2.0 V) of the signal in question. Both input and output timing are measured at the pin.
2. All maximum timing specifications assume C_L = 50 pF.
3. This minimum parameter assumes C_L = 0 pF.
4. t_{sysclk} is the period of the external bus clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration of the parameter in question.
5. Output signal transitions from GND to 2.0V or OV_{DD} to 0.8V.
6. Nominal precharge width for $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ is 0.5 t_{sysclk}.
7. Nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 t_{sysclk}.
8. Guaranteed by design and characterization.

Figure 13. Output Timing Diagram



VM = Midpoint Voltage (1.4V)

L2 Clock AC Specifications

Table 12. L2CLK Output AC Timing Specifications

$V_{DD} = AV_{DD} = L2AV_{DD} = 2.6\ V_{DC} \pm 100$ mV, $OV_{DD} = L2OV_{DD} = 3.3 \pm 5\%\ V_{DC}$, GND = 0 V_{DC},$-55 \le T_j < 125°C$

Num	Characteristic	Min	Max	Unit	Notes
	L2CLK Frequency	80	133	MHz	1, 5
22	L2CLK Cycle Time	7.5	12.5	ns	
23	L2CLK Duty Cycle	50		%	2
	L2CLK Jitter		±150	ps	3
	Internal DLL-relock Time	640	-	L2CLK	4

Notes:
1. L2CLK outputs are L2CLK_OUTA, L2CLK_OUTB and L2SYNC_OUT pins. The L2 cache interface supports higher frequencies when appropriate load conditions have been considered. The L2 I/O drivers have been designed to support a 133 MHz L2 bus loaded with 4 off-the-shelf pipelined synchronous burst SRAMs. Running the L2 bus beyond 133 MHz requires tightly coupled customized SRAMs or a multi-chip module (MCM) implementation. The L2CLK frequency to core frequency settings must be chosen such that the resulting L2CLK frequency and core frequency do not exceed their respective maximum or minimum operating frequencies. L2CLK_OUTA and L2CLK_OUTB must have equal loading.
2. The nominal duty cycle of the L2CLK is 50% measured at midpoint voltage.
3. The total input jitter (short term and long term combined) must be under ±150 ps.
4. The DLL re-lock time is specified in terms of L2CLKs. The number in the table must be multiplied by the period of L2CLK to compute the actual time duration in nanoseconds. Re-lock timing is guaranteed by design and characterization.
5. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 110 MHz.

The L2CLK_OUT timing diagram is shown in Figure 14.

Figure 14. L2CLK_OUT Output Timing Diagram

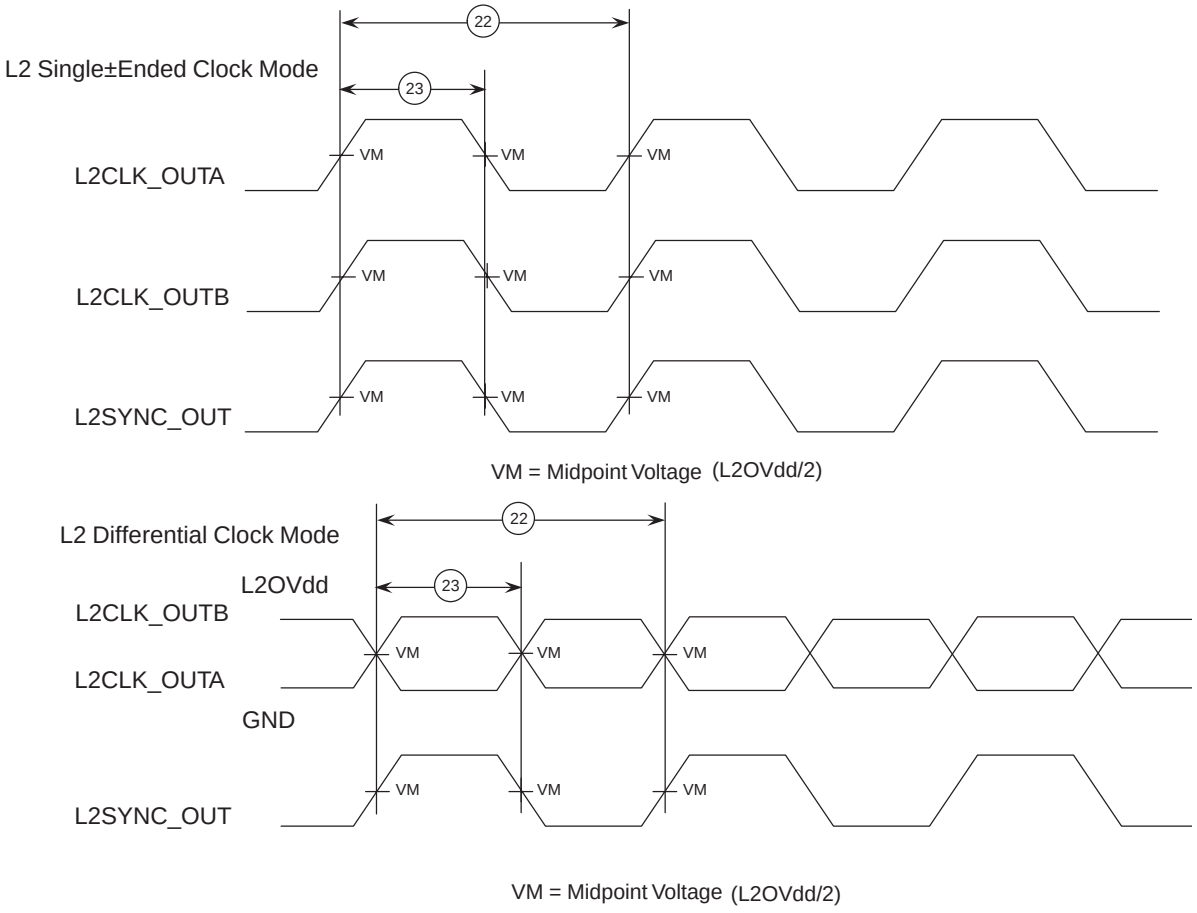
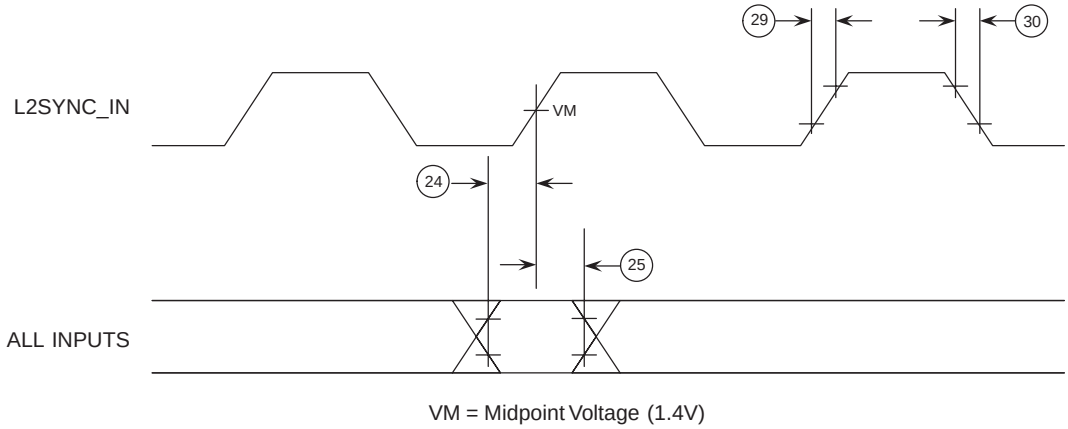


Table 13 shows the L2 bus input timing diagrams for the TSPC750A.

Figure 15. L2 Bus Input Timing Diagrams



L2 Bus Input AC Specifications

The L2 bus input interface AC timing specifications are found in Table 13.

Table 13. L2 Bus Input Interface AC Timing Specifications, see note (1)

$V_{DD} = AV_{DD} = L2AV_{DD} = 2.6\ V_{DC} \pm 100$ mV, $OV_{DD} = L2OV_{DD} = 3.3 \pm 5\%\ V_{DC}$, GND = 0 V_{DC}, $-55 \le T_j < 125°C$

Num	Characteristic	Processor Frequency 200-266 MHz		Unit	Notes
		Min	Max		
29, 30	L2SYNC_IN rise and fall time	-	1.0	ns	2
24	Data and parity input setup to L2SYNC_IN	2.0	-	ns	
25	L2SYNC_IN to data and parity input hold	0.5	_	ns	

Notes:
1. All input specifications are measured from the TTL level (0.8V or 2.0V) of the signal in question to the midpoint voltage of the rising edge of the input L2SYNC_IN. Input timings are measured at the pins (see Figure 15).
2. Rise and fall times for the L2SYNC_IN input are measured from 0.4 to 2.4V.

L2 Bus Output AC Specifications

Table 14 provides the L2 bus output interface AC timing specifications for the TSPC750A as defined in Figure 16.

Table 14. L2 Bus Output Interface AC Timing Specifications see note (1)

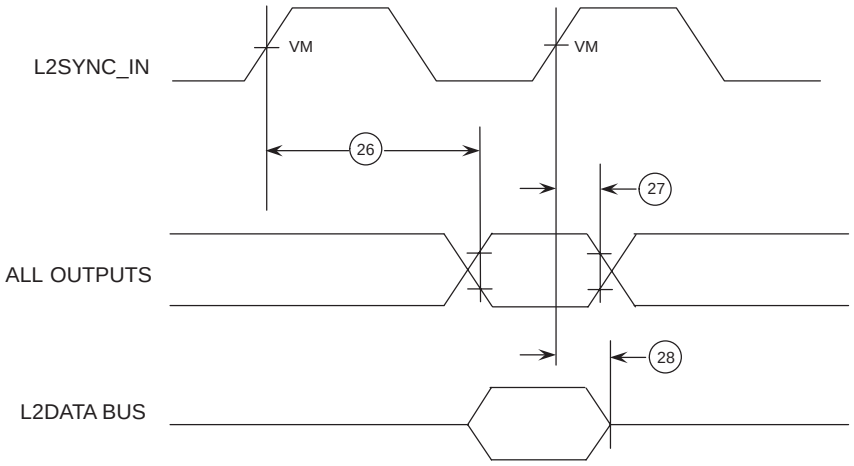
$V_{DD} = AV_{DD} = L2AV_{DD} = 2.6\ V_{DC} \pm 100$ mV, $OV_{DD} = L2OV_{DD} = 3.3 \pm 5\%\ V_{DC}$, GND = 0 V_{DC}, $-55 \le T_j < 125°C$, CL = 20 pF see note (3)

Num	Characteristic	L2CR[14-15] is equivalent to:								Unit	Notes
		00(2)		01		10		11			
		Min	Max	Min	Max	Min	Max	Min	Max		
26	L2SYNC_IN to output valid	-	5.0	-	5.5	-	5.7	-	6	ns	
27	L2SYNC_IN to output hold	0.5	-	1.0	-	1,2	-	1,5	-	ns	4
28	L2SYNC_IN to high impedance	-	4.0	-	4.5	-	4.7	-	5	ns	

Notes:
1. All outputs are measured from the midpoint voltage of the rising edge of L2SYNC_IN to the TTL level (0.8V or 2.0V) of the signal in question. The output timings are measured at the pins.
2. The outputs are valid for both single-ended and differential L2CLK modes. For flow-THRU and pipelined reg-reg synchronous burst RAMs, L2CR[14-15] = 00 is recommended. For pipelined delay-write synchronous burst SRAMs, L2CR[14-15] = 01 is recommended.
3. All maximum timing specifications assume $C_L = 20$ pF.
4. This measurement assumes $C_L = 5$ pF.
5. Reserved for future use.

Figure 16 shows the L2 bus output timing diagrams for the TSPC750A.

Figure 16. L2 Bus Output Timing Diagrams



VM = Midpoint Voltage(1.4V)

IEEE 1149.1 AC Timing Specifications

Table 15 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 17, Figure 18, Figure 19, and Figure 20.

Table 15. JTAG AC Timing Specifications (Independent of SYSCLK)

$V_{DD} = AV_{DD} = L2AV_{DD} = 2.6\ V_{DC} \pm 100$ mV, $OV_{DD} = L2OV_{DD} = 3.3 \pm 5\%\ V_{DC}$, GND = 0 V_{DC}, $-55 \le T_j < 125°C$, $C_L = 50$ pF

Num	Characteristic	Min	Max	Unit	Notes
	TCK Frequency Of Operation	0	33.3	MHz	
1	TCK Cycle Time	30	-	ns	
2	TCK Clock Pulse Width Measured at 1.4V	15	-	ns	
3	TCK Rise and Fall Times	0	2	ns	
4	Specification Obsolete, Intentionally Omitted				
5	TRST Assert Time	25	-	ns	1
6	Boundary-scan Input Data Setup Time	4	-	ns	2
7	Boundary-scan Input Data Hold Time	15	-	ns	2
8	TCK to Output Data Valid	4	20	ns	3
9	TCK to Output High Impedance	3	19	ns	3, 4
10	TMS, TDI Data Setup Time	0	-	ns	
11	TMS, TDI Data Hold Time	12	-	ns	
12	TCK to TDO Data Valid	4	12	ns	
13	TCK to TDO High Impedance	3	9	ns	4

Notes:
1. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.
2. Non-JTAG signal input timing with respect to TCK.
3. Non-JTAG signal output timing with respect to TCK.
4. Guaranteed by design and characterization.

Figure 17 provides the JTAG clock input timing diagram.

Figure 17. JTAG Clock Input Timing Diagram

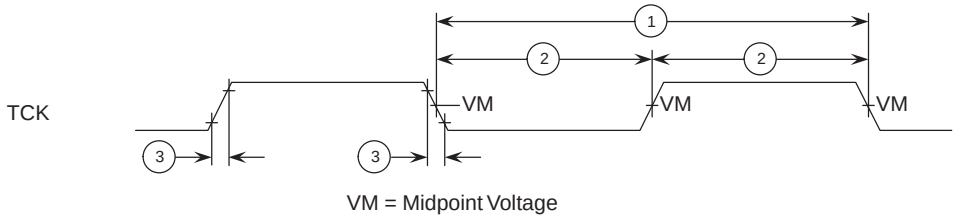


Figure 18 provides the $\overline{\text{TRST}}$ timing diagram.

Figure 18. $\overline{\text{TRST}}$ Timing Diagram

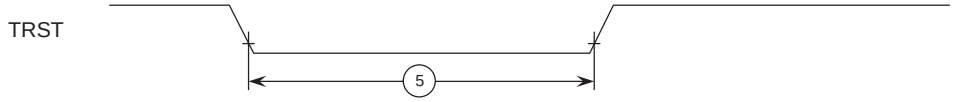


Figure 19 provides the boundary-scan timing diagram.

Figure 19. Boundary-Scan Timing Diagram

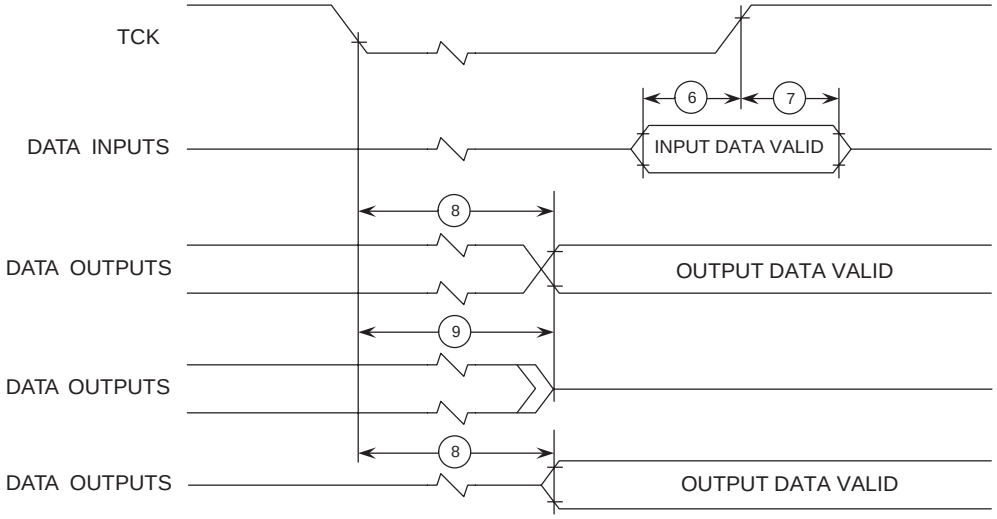
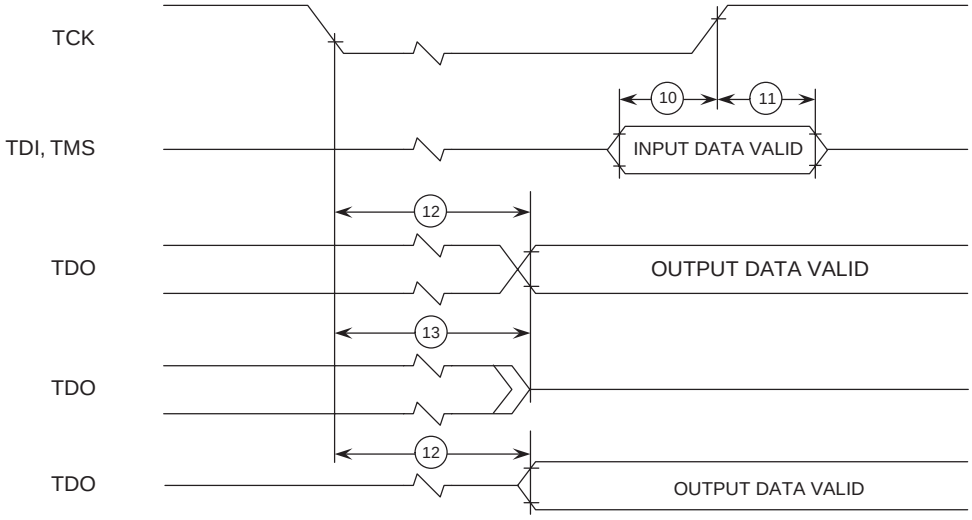


Figure 20 provides the test access port timing diagram.

Figure 20. Test Access Port Timing Diagram



Preparation for Delivery

Packaging

Microcircuits are prepared for delivery in accordance with MIL-PRF-38535.

Certificate of Compliance

ATMEL-Grenoble offers a certificate of compliances with each shipment of parts, affirming the products are in compliance either with MIL-PRF-883 and guaranteeing the parameters not tested at temperature extremes for the entire temperature range.

Handling

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of static buildup. However, the following handling practices are recommended:

a) Devices should be handled on benches with conductive and grounded surfaces.

b) Ground test equipment, tools and operator.

c) Do not handle devices by the leads.

d) Store devices in conductive foam or carriers.

e) Avoid use of plastic, rubber, or silk in MOS areas.

f) Maintain relative humidity above 50 percent if practical.

g) For CI-CGA packages, use specific tray to take care of the highest height of the package compared with the regular CBGA.

Clock Relationships Choice

The TSPC750A's PLL is configured by the PLL_CFG[0-3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the TSPC750A is shown in Table 16 for nominal frequencies. Table 17 provides sample core-to-L2 frequencies.

Table 16. TSPC750A Microprocessor PLL Configuration

	Sample Bus-to-Core Frequency in MHz (VCO Frequency in MHz)									
PLL_CFG [0-3]	**Bus-to-Core Multiplier**	**Core-to VCO Multiplier**	**Bus 25 MHz**	**Bus 33.3 MHz**	**Bus 40 MHz**	**Bus 50 MHz**	**Bus 66.6 MHz**	**Bus 75 MHz**	**Bus 83.3 MHz**	**Bus 100 MHz**
1000	3x	2x				150 (300)	200 (400)	225 (450)	250 (500)	
1110	3.5x	2x				175 (350)	233 (466)	262 (525)		
1010	4x	2x			160 (320)	200 (400)	266 (533)			
0111	4.5x	2x		150 (300)	180 (360)	225 (450)				
1011	5x	2x		166 (333)	200 (400)	250 (500)				
1001	5.5x	2x		183 (366)	220 (440)					
1101	6x	2x	150 (300)	200 (400)	240 (480)					
0101	6.5x	2x	162 (325)	216 (433)	260 (520)					
0010	7x	2x	175 (350)	233 (466)						
0001	7.5x	2x	187 (375)	250 (500)						
1100	8x	2x	200 (400)	266 (533)						
0011	PLL off/bypass		PLL off, SYSCLK clocks core circuitry directly, 1x bus-to-core implied							
1111	PLL off		PLL off, no core clocking occurs							

Notes:
1. PLL_CFG[0—3] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the TSPC750A; see "Clock AC Specifications," for valid SYSCLK and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In clock-off mode, no clocking occurs inside the TSPC750A regardless of the SYSCLK input.

Table 17. Sample Core-to-L2 Frequencies

Core Frequency in MHz	÷1	÷1.5	÷2	÷2.5	÷3
200	200	133.3	100	80	-
208.3	208	138.6	104	83.3	-
210	210	140	105	84	-
220	220	146.6	110	88	-
225	225	150	112.5	90	-
233.3	233.3	155.5	116.6	93.3	-
240	240	160	120	96	80
266	266	177.3	133	106.4	88.6

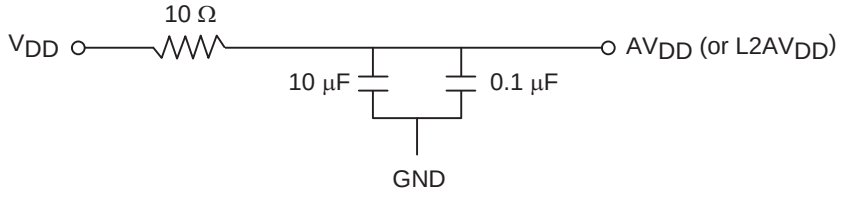
Note: 1. The core and L2 frequencies are for reference only. Some configurations may select core or L2 frequencies which are not useful, not supported, or not tested for by the TSPC750A; see “L2 Clock AC Specifications,” for valid L2CLK frequencies. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 110 MHz.

System Design Information

PLL Power Supply Filtering

The AV_{DD} and $L2AV_{DD}$ power signals are provided on the TSPC750A to provide power to the clock generation phase-locked loop and L2 cache delay-locked loop respectively. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered using a circuit similar to the one shown in Figure 21. The circuit should be placed as close as possible to the AV_{DD} pin to ensure it filters out as much noise as possible. An identical but separate circuit should be placed as close as possible to the $L2AV_{DD}$ pin.

Figure 21. PLL Power Supply Filter Circuit



Decoupling Recommendations

Due to the TSPC750A’s dynamic power management feature, large address and data buses, and high operating frequencies, the TSPC750A can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the TSPC750A system, and the TSPC750A itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} and OV_{DD} pin (and $L2OV_{DD}$ for the 360 CBGA) of the TSPC750A. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, OV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should vary in value from 220 pF to 10 µF to provide both high- and low-frequency filtering, and should be placed as close as possible to their associated V_{DD} or OV_{DD} pins. Suggested values for the V_{DD} pins-220 pF (ceramic), 0.01 µF (ceramic), and 0.1 µF (ceramic). Suggested values for the OV_{DD} pins — 0.01 µF (ceramic), 0.1 µF (ceramic), and 10 µF (tantalum). Only SMT (surface mount technology) capacitors should be used to minimize lead inductance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors-100 µF (AVX TPS tantalum) or 330 µF (AVX TPS tantalum).

Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to V_{DD}. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, and GND pins of the TSPC750A.

External clock routing should ensure that the rising-edge of the L2 clock is coincident at the CLK input of all SRAMs and at the L2SYNC_IN input of the TSPC750A. The L2CLKOUTA network could be used only, or the L2CLKOUTB network could also be used depending on the loading, frequency, and number of SRAMs.

Output Buffer DC Impedance

The TSPC750A 60x and L2 I/O drivers were characterized over process, voltage, and temperature. To measure Z_0, an external resistor is connected to the chip pad, either to OV_{DD} or OGND. Then, the value of such resistor is varied until the pad voltage is $OV_{DD}/2$; see Figure 22.

The output impedance is actually the average of two components, the resistances of the pull-up and pull-down devices. When Data is held low, SW1 is closed (SW2 is open), and R_N is trimmed until Pad = $OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When Data is held high, SW2 is closed (SW1 is open), and R_P is trimmed until Pad = $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. With a properly designed driver R_P and R_N are close to each other in value. Then $Z_0 = (R_P + R_N)/2$.

Figure 22. Driver Impedance Measurement

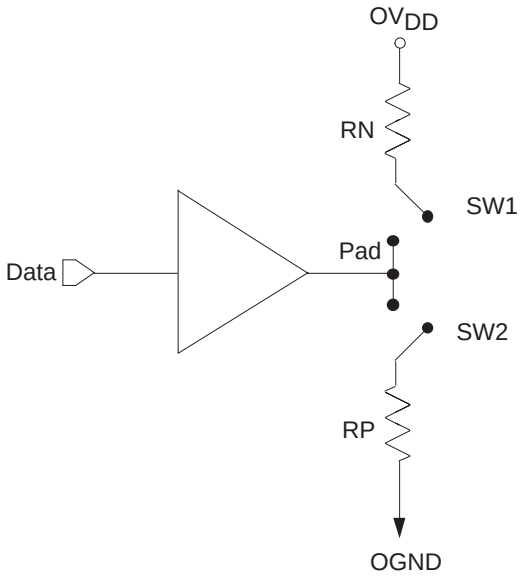


Table 18 summarizes the signal impedance results. The driver impedance values were derived by simulation at 65°C. As the process varies, the output impedance will be reduced by several ohms.

Table 18. Impedance Characteristics

V_{DD} = 2.6V, OV_{DD} = 3.3V, Tj = 65°C

Process	60x	L2	Symbol	Unit
TYP	43	38	Z_0	Ohms

Pull-up Resistor Requirements

The TSPC750A requires high-resistive (weak: 10KΩ) pull-up resistors on several control signals of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the TSPC750A or other bus masters. These signals are $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$.

In addition, the TSPC750A has one open-drain style output that requires a pull-up resistors (weak or stronger: 4.7KΩ - 10KΩ) if it is used by the system. This signal is $\overline{CKSTP\_OUT}$.

During inactive periods on the bus, the address and transfer attributes on the bus are not driven by any master and may float in the high-impedance state for relatively long periods of time. Since the TSPC750A must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on the TSPC750A or by other receivers in the system. It is recommended that these signals be pulled up through weak (10KΩ) pull-up resistors or restored in some manner by the system. The snooped address and transfer attribute inputs are A[0-31], AP[0-3], TT[0-4], $\overline{TBST}$, and $\overline{GBL}$.

The data bus input receivers are normally turned off when no read operation is in progress and do not require pull-up resistors on the data bus. Other data bus receivers in the system, however, may require pull-ups, or that those signals be otherwise driven by the system during inactive periods. The data bus signals are DH[0-31], DL[0-31], DP[0-7].

If address or data parity is not used by the system, and the respective parity checking is disabled through HID0, the input receivers for those pins are disabled, and those pins do not require pull-up resistors and should be left unconnected by the system. If all parity generation is disabled through HID0, then all parity checking should also be disabled through HID0, and all parity pins may be left unconnected by the system.

No pull-up resistors are normally required for the L2 interface.

Definitions

Datasheet status		**Validity**
Objective specification	This datasheet contains target and goal specification for discussion with customer and application validation.	Before design phase.
Target specification	This datasheet contains target or goal specification for product development.	Valid during the design phase.
Preliminary specification ∝ site	This datasheet contains preliminary data. Additional data may be published later; could include simulation result.	Valid before characterization phase.
Preliminary specification β site	This datasheet contains also characterization results.	Valid before the industrialization phase.
Product specification	This datasheet contains final product specification.	Valid for production purpose.
Limiting values		
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.		
Application information		
Where application information is given, it is advisory and does not form part of the specification.		

Life Support Applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. ATMEL-Grenoble customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify ATMEL-Grenoble for any damages resulting from such improper use or sale.

Package Mechanical Data

Parameters for the TSPC740A

The package parameters are as provided in the following list. The package types are 21 x 21 mm, 255-lead CBGA and CI-CGA.

Package outline — 21 x 21 mm

Interconnects — 255 (16 x 16 ball array - 1)

Pitch — 1.27 mm (50 mil)

Minimum module height — 2.45 mm (CBGA), 3,45 mm (CI-CGA)

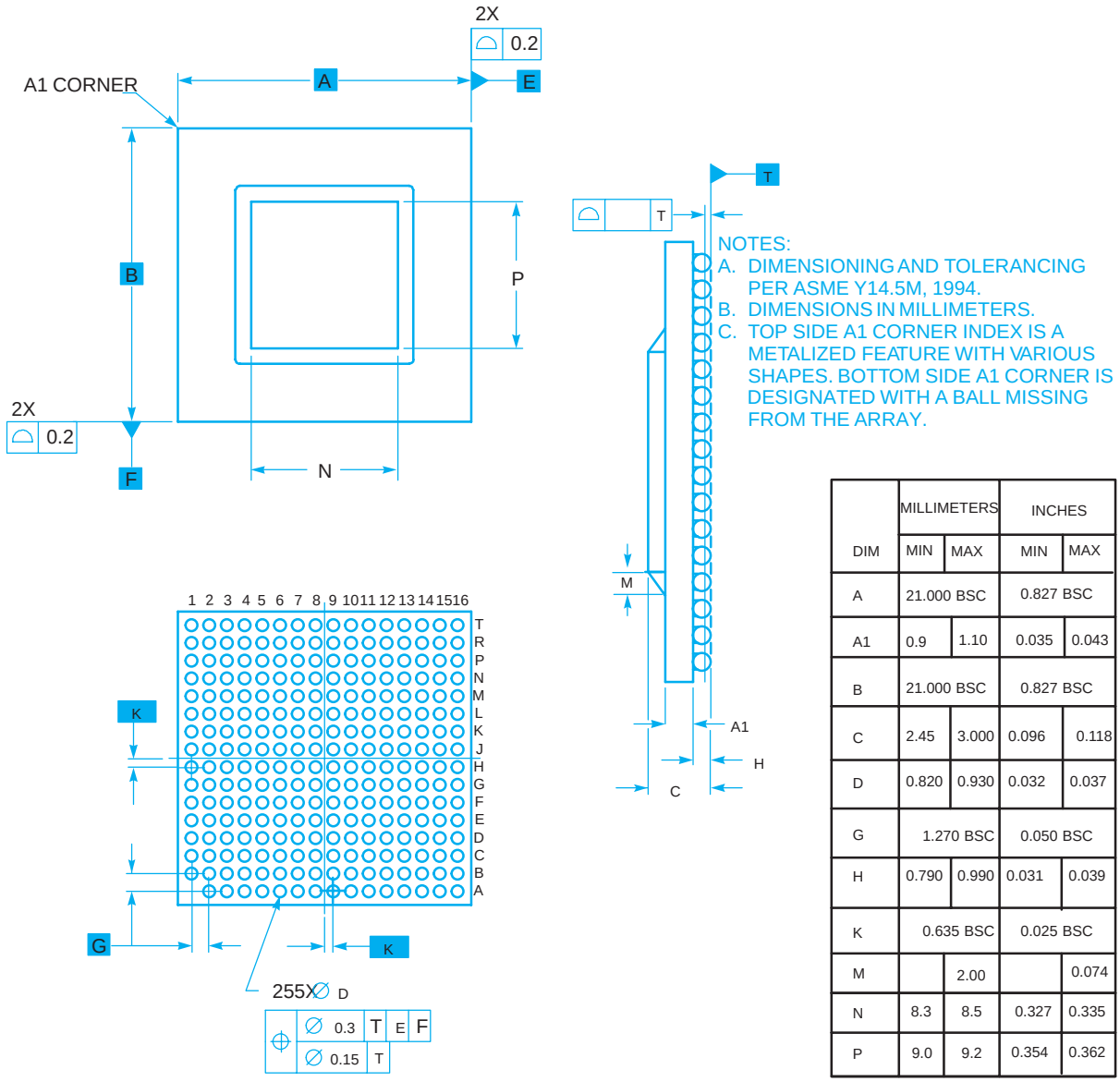
Maximum module height — 3.00 mm (CBGA), 4.00 mm (CI-CGA

Ball or column diameter — 0.89 mm (35 mil)

Mechanical Dimensions of the TSPC740A CBGA Package

Figure 23 provides the mechanical dimensions and bottom surface nomenclature of the TSPC740A, 255 CBGA package.

Figure 23. Mechanical Dimensions and Bottom Surface Nomenclature of TSPC740A (CBGA)

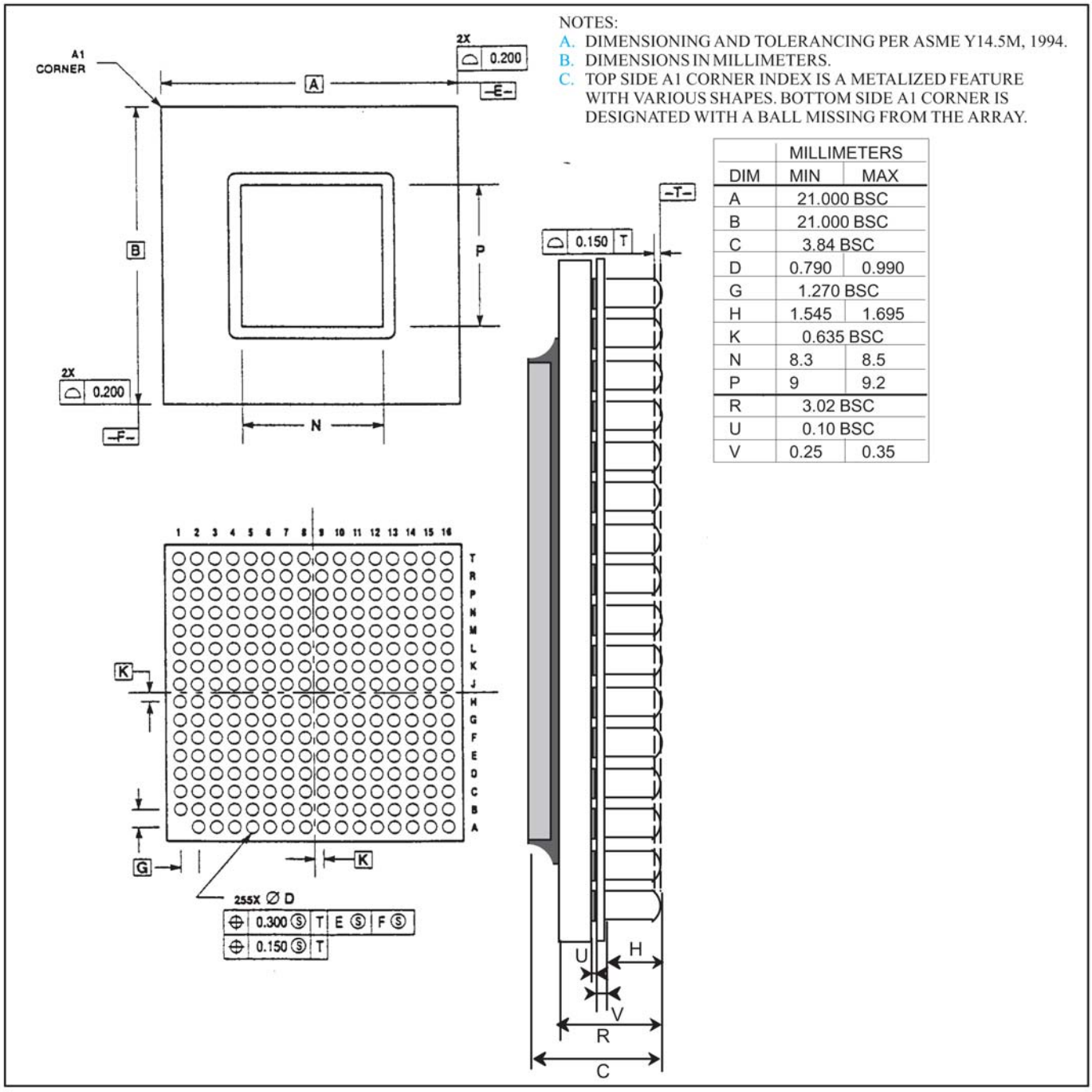


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	21.000 BSC		0.827 BSC	
A1	0.9	1.10	0.035	0.043
B	21.000 BSC		0.827 BSC	
C	2.45	3.000	0.096	0.118
D	0.820	0.930	0.032	0.037
G	1.270 BSC		0.050 BSC	
H	0.790	0.990	0.031	0.039
K	0.635 BSC		0.025 BSC	
M		2.00		0.074
N	8.3	8.5	0.327	0.335
P	9.0	9.2	0.354	0.362

Mechanical Dimensions of the TSPC740A CI-CGA Package

Figure 24 provides the mechanical dimensions and bottom surface nomenclature of TSPC740A, 255 CI-CGA package.

Figure 24. Mechanical Dimensions and Bottom Surface Nomenclature of TSPC740A (CI-CGA)



DIM	MILLIMETERS MIN	MAX
A	21.000 BSC	
B	21.000 BSC	
C	3.84 BSC	
D	0.790	0.990
G	1.270 BSC	
H	1.545	1.695
K	0.635 BSC	
N	8.3	8.5
P	9	9.2
R	3.02 BSC	
U	0.10 BSC	
V	0.25	0.35

Parameters for the TSPC750A

The package parameters are as provided in the following list. The package type is 25 x 25 mm, 360-lead CBGA and CI-CGA.

Package outline — 25 x 25 mm

Interconnects — 360 (19 x 19 ball array - 1)

Pitch — 1.27 mm (50 mil)

Minimum module height — 2.65 mm (CBGA), 3,65 mm (CI-CGA)

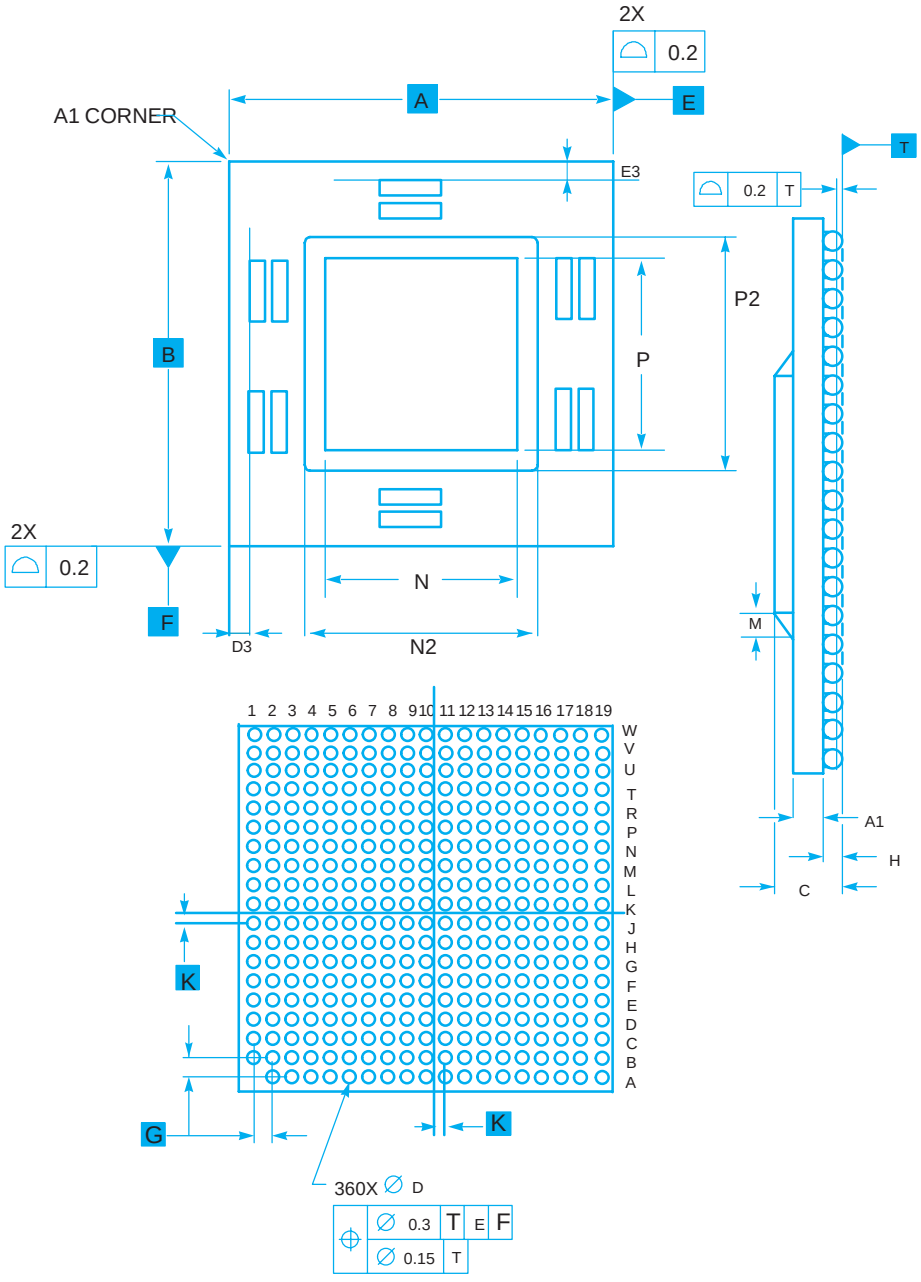
Maximum module height — 3.20 mm (CBGA), 4,20 mm (CI-CGA)

Ball or column diameter — 0.89 mm (35 mil)

Mechanical Dimensions of the TSPC750A CBGA Package

Figure 25 provides the mechanical dimensions and bottom surface nomenclature of the TSPC750A, 360 CBGA package.

Figure 25. Mechanical Dimensions and Bottom Surface Nomenclature of the TSPC750A



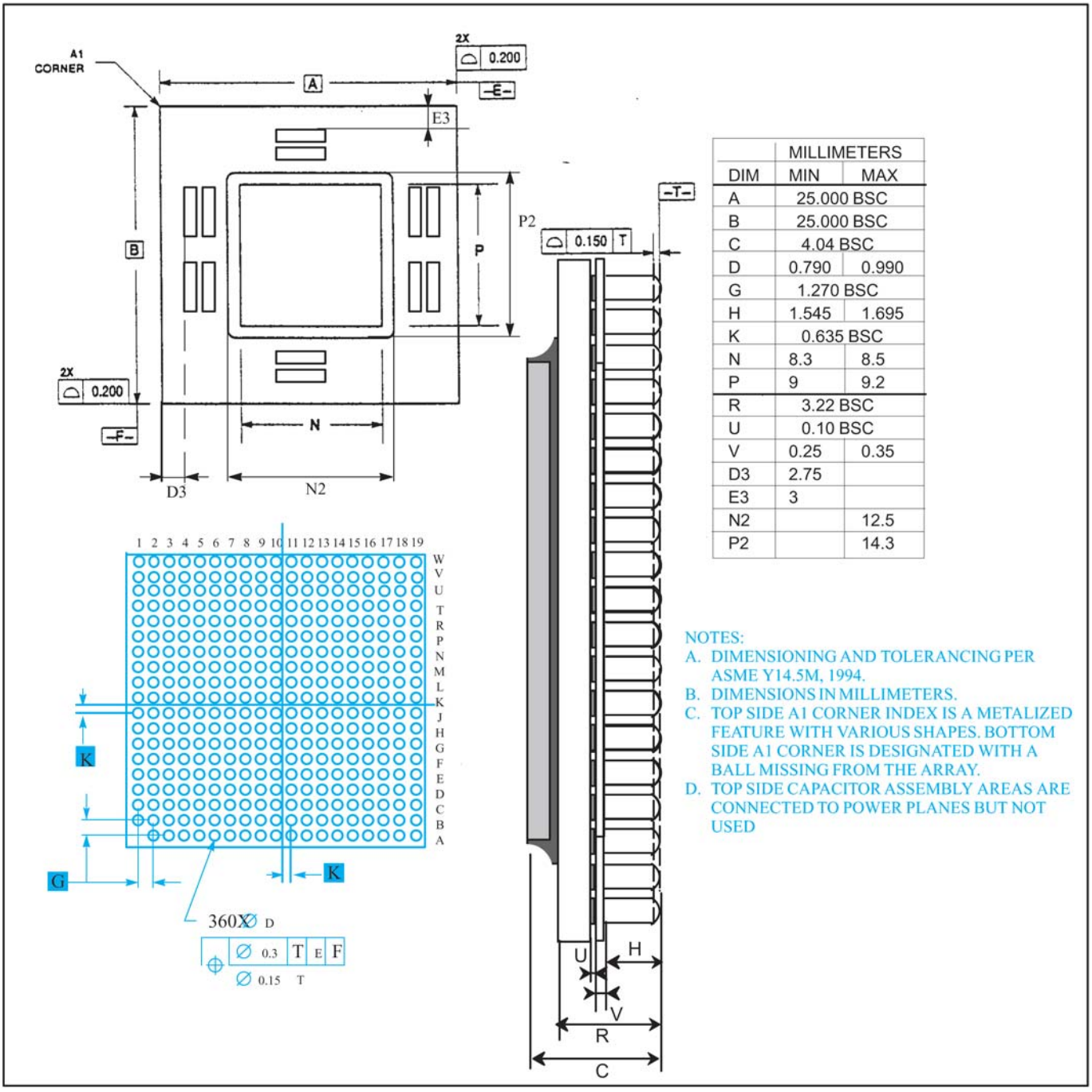
NOTES:
A. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
B. DIMENSIONS IN MILLIMETERS.
C. TOP SIDE A1 CORNER INDEX IS A METALIZED FEATURE WITH VARIOUS SHAPES. BOTTOM SIDE A1 CORNER IS DESIGNATED WITH A BALL MISSING FROM THE ARRAY.
D. TOP SIDE CAPACITOR ASSEMBLY AREAS ARE CONNECTED TO POWER PLANES BUT NOT USED

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.000 BSC		0.984 BSC	
A1	1.1	1.3	0.043	0.052
B	25.000 BSC		0.984 BSC	
C	2.65	3.2	0.104	0.126
D	0.820	0.930	0.032	0.037
G	1.270 BSC		0.050 BSC	
H	0.790	0.990	0.031	0.039
K	0.635 BSC		0.025 BSC	
M		2.00		0.079
N	8.3	8.5	0.327	0.335
P	9.0	9.2	0.354	0.362
D3	2.75		0.108	
E3	3		0.118	
N2		12,5		0.492
P2		14.3		0.563

Mechanical Dimensions of the TSPC750A CI-CGA Package

Figure 26 provides the mechanical dimensions and bottom surface nomenclature of TSPC750A, 360 CI-CGA package

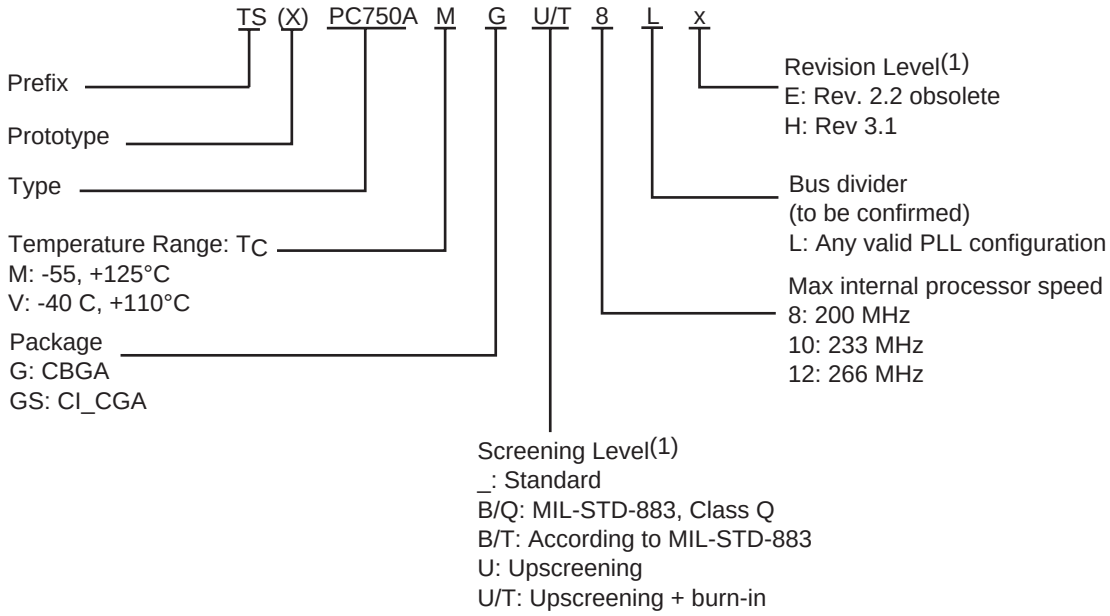
Figure 26. Mechanical Dimensions and Bottom Surface Nomenclature of TSPC750A (CI-CGA)



DIM	MILLIMETERS MIN	MAX
A	25.000 BSC	
B	25.000 BSC	
C	4.04 BSC	
D	0.790	0.990
G	1.270 BSC	
H	1.545	1.695
K	0.635 BSC	
N	8.3	8.5
P	9	9.2
R	3.22 BSC	
U	0.10 BSC	
V	0.25	0.35
D3	2.75	
E3	3	
N2		12.5
P2		14.3

NOTES:
A. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
B. DIMENSIONS IN MILLIMETERS.
C. TOP SIDE A1 CORNER INDEX IS A METALIZED FEATURE WITH VARIOUS SHAPES. BOTTOM SIDE A1 CORNER IS DESIGNATED WITH A BALL MISSING FROM THE ARRAY.
D. TOP SIDE CAPACITOR ASSEMBLY AREAS ARE CONNECTED TO POWER PLANES BUT NOT USED

Ordering Information



Note: 1. For availability of different versions, contact your Atmel sales office.

Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 487-2600

Europe
Atmel SarL
Route des Arsenaux 41
Casa Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Memory
Atmel Corporate
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 436-4270
FAX 1(408) 436-4314

Microcontrollers
Atmel Corporate
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 436-4270
FAX 1(408) 436-4314

Atmel Nantes
La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
TEL (33) 2-40-18-18-18
FAX (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Atmel Rousset
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4-42-53-60-00
FAX (33) 4-42-53-60-01

Atmel Colorado Springs
1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Atmel Smart Card ICs
Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
TEL (44) 1355-803-000
FAX (44) 1355-242-743

RF/Automotive
Atmel Heilbronn
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
TEL (49) 71-31-67-0
FAX (49) 71-31-67-2340

Atmel Colorado Springs
1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Datacom
Atmel Grenoble
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-76-58-30-00
FAX (33) 4-76-58-34-80

---

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

2128A–HIREL–01/02 0M