AUTOMOTIVE GRADE

CS8135

5V, 5V Low Dropout Dual Regulator with $\overline{\text{RESET}}$/ENABLE

Description

The CS8135 is a low dropout, high current, dual 5V linear regulator. The secondary 5V/10mA output is often used for powering systems with standby memory. Quiescent current drain is less than 3mA when supplying 10mA loads from the standby regulator.

In automotive applications, the CS8135 and all regulated circuits are protected from reverse battery installations, as well as two-battery jumps. During line transients, such as a 60V load dump, the 500mA output will automatically shut down the primary output to protect both internal circuits and the load. The standby regulator will continue to power any standby load.

The CS8135 is packaged in a 5 lead TO-220.

NOTE: The CS8135 is compatible with the LM2935.

Features

- **Two Regulated Outputs**
  - **Primary Output 5V ± 5%; 500mA**
  - **Secondary Standby 5V ±5%; 10mA**
- **Low Dropout Voltage (0.6V at 0.5A)**
- **ON/OFF Control Option**
- **Low Quiescent Drain (<3mA)**
- **$\overline{\text{RESET}}$ Option**
- **Protection Features**
  - **Reverse Battery**
  - **60V Load Dump**
  - **-50V Reverse Transient**
  - **Short Circuit**
  - **Thermal Shutdown**
  - **Overvoltage Shutdown**

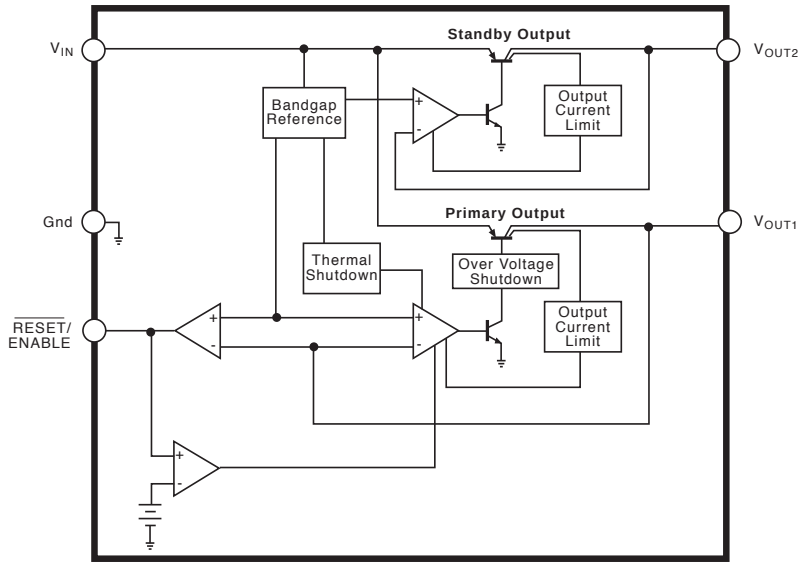
Absolute Maximum Ratings

Input Voltage
- Operating Range ..... -0.5V to 26V
- Load Dump 60V

Internal Power Dissipation ..... Internally Limited
Junction Temperature Range (T_J) ..... -40°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature Soldering
- Wave Solder (through hole styles only) ..... 10 sec. max, 260°C peak

Electrostatic Discharge (Human Body Model) 2kV

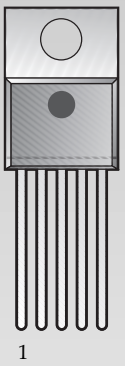
Block Diagram



Package Option

5 Lead TO-220

Tab (Gnd)



1

1 V_{IN}
2 V_{OUT1}
3 Gnd
4 $\overline{\text{RESET}}$ / ENABLE
5 V_{OUT2}

Cherry Semiconductor

Cherry Semiconductor Corporation
2000 South County Trail, East Greenwich, RI 02818
Tel: (401)885-3600 Fax: (401)885-5786
Email: info@cherry-semi.com
Web Site: www.cherry-semi.com

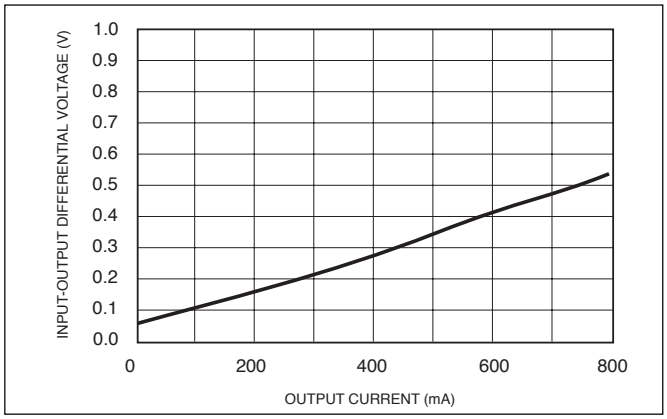
Electrical Characteristics : V_{IN} = 14V, I_{OUT1} = 5mA, I_{OUT2} = 1mA, -40°C ≤ T_A ≤ 125°C, -40°C ≤ T_J ≤ 150°C unless otherwise specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Output Stage (V_{OUT1})					
Output Voltage, V_{OUT1}	6V ≤ V_{IN} ≤ 26V, 5mA ≤ I_{OUT1} ≤ 500mA	4.75	5.00	5.25	V
Dropout Voltage	I_{OUT} = 500mA I_{OUT} = 750mA		0.35 0.50	0.60	V V
Line Regulation	6V ≤ V_{IN} ≤ 26V, I_{OUT1} = 5mA		10	50	mV
Load Regulation	5mA ≤ I_{OUT} ≤ 500mA		10	50	mV
Quiescent Current	I_{OUT1} ≤ 10mA, No Load on Standby I_{OUT1} = 500mA, No Load on Standby I_{OUT1} = 750mA, No Load on Standby		3 30 60	7 100 150	mA mA mA
Ripple Rejection	f = 120Hz		66		dB
Current Limit		0.75	1.40		A
Maximum Line Transient	V_{OUT1} ≤ 5.5V		90		V
Reverse Polarity Input Voltage, DC	V_{OUT1} ≥ -0.6V, 10Ω Load		-50		V
Reverse Polarity Input Voltage, Transient	1% Duty Cycle, t = 100ms, V_{OUT1} ≥ -6V, 10Ω Load		-80		V
Output Noise Voltage	10Hz-100kHz		100		μVrms
Long Term Stability			20		mV/khr
Output Impedance	500mA DC and 10mA rms, 100Hz-10kHz		200		mΩ
Overvoltage Shutdown			30		V
■ Standby Output (V_{OUT2})					
Output Voltage (V_{OUT2})	6V ≤ V_{IN} ≤ 26V, 1mA ≤ I_{OUT1} ≤ 10mA	4.75	5.00	5.25	V
Dropout Voltage	I_{OUT2} = 10mA		0.3	0.7	V
Tracking	V_{OUT1}-V_{OUT2}		50	200	mV
Line Regulation	6V ≤ V_{IN} ≤ 26V		4	50	mV
Load Regulation	1mA ≤ I_{OUT1} ≤ 10mA		10	50	mV
Quiescent Current	I_{OUT} ≤ 10mA, V_{OUT} OFF		2	3	mA
Ripple Rejection	f = 120Hz		66		dB
Current Limit		25	70		mA
Output Noise Voltage	10Hz-100kHz		300		μV
Long Term Stability			20		mV/khr
Output Impedance	10mA DC and 1mA rms, 100Hz-10kHz		1		Ω
■ $\overline{\text{RESET}}$ Function					
$\overline{\text{RESET}}$ Output Voltage Low R_1 = 20kΩ, V_{IN} = 4.5V High R_1 = 20kΩ, V_{IN} = 14V	 See Test & Application Circuit (page 6)	 4.5	 0.8 5.0	 1.1 6.0	 V V
$\overline{\text{RESET}}$ Output Current	V_{IN} = 4.5V, $\overline{\text{RESET}}$ in Low State		5		mA
ON/OFF Resistor	R1 (±10% Tolerance)		20	30	kΩ

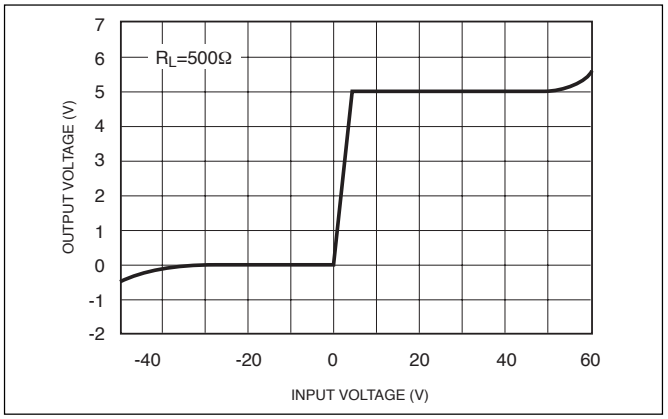
Package Lead Description

PACKAGE LEAD #	LEAD SYMBOL	FUNCTION
TO-220		
1	V_{IN}	Supply voltage to IC, usually direct from battery.
2	V_{OUT1}	Regulated output voltage 5V, 500mA (typ) switched.
3	Gnd	Ground connection.
4	$\overline{\text{RESET}}$/ENABLE	CMOS compatible output lead, $\overline{\text{RESET}}$ goes low whenever V_{OUT1} becomes unregulated. To use the ENABLE option, connect the lead via a resistor to V_{IN} (see app. notes).
5	V_{OUT2}	STANDBY output 5V, 10mA typ, always on.

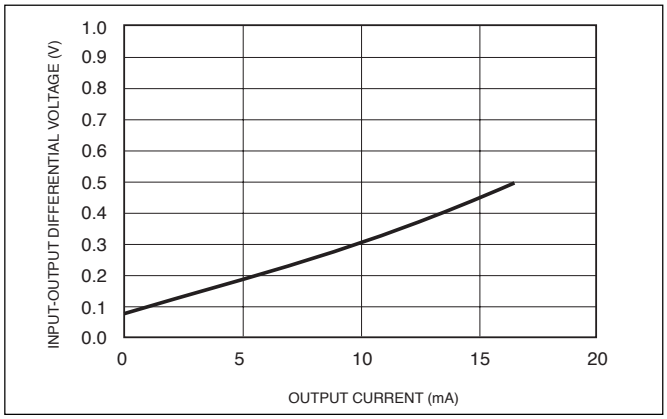
Typical Performance Characteristics



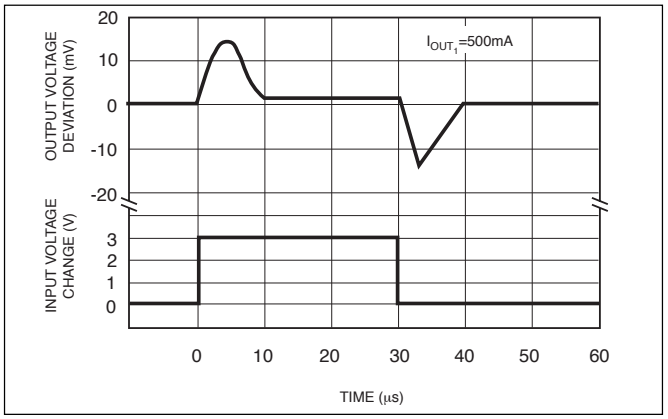
Dropout Voltage vs. Output Current



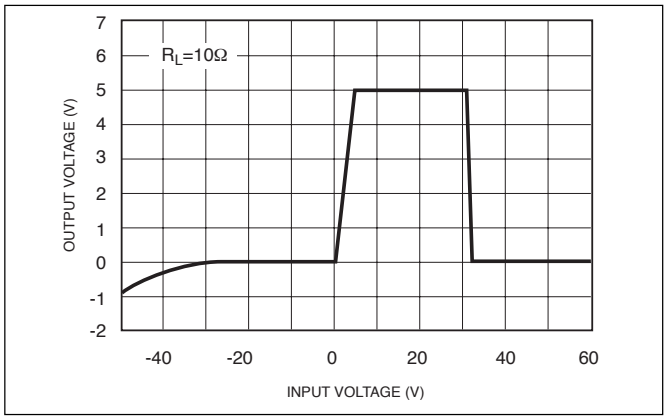
Standby Output Voltage vs. Input Voltage



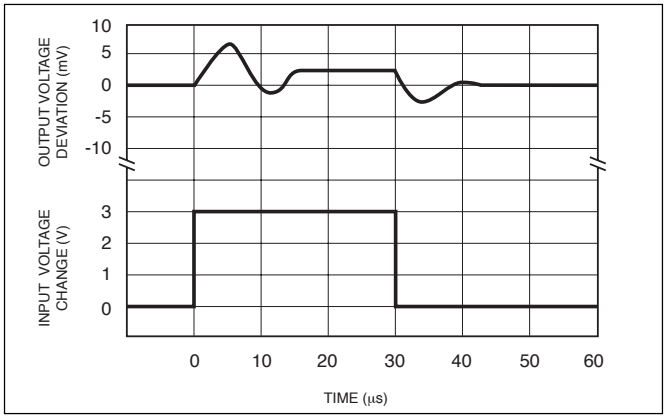
Standby Dropout Voltage vs. Output Current



Line Transient Response (V_{OUT1})

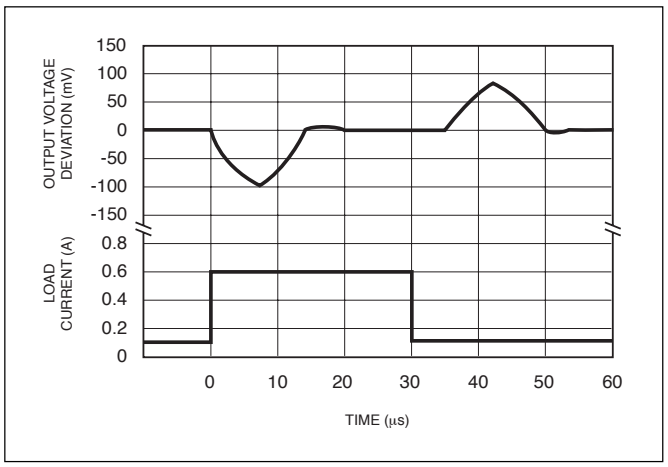


Output Voltage vs. Input Voltage

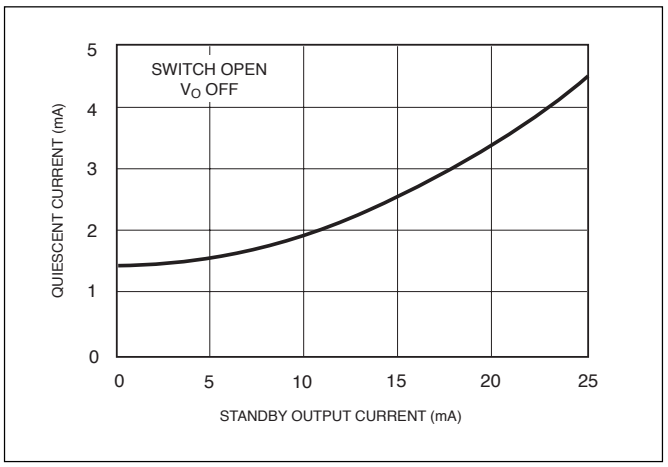


Line Transient Response (V_{OUT2})

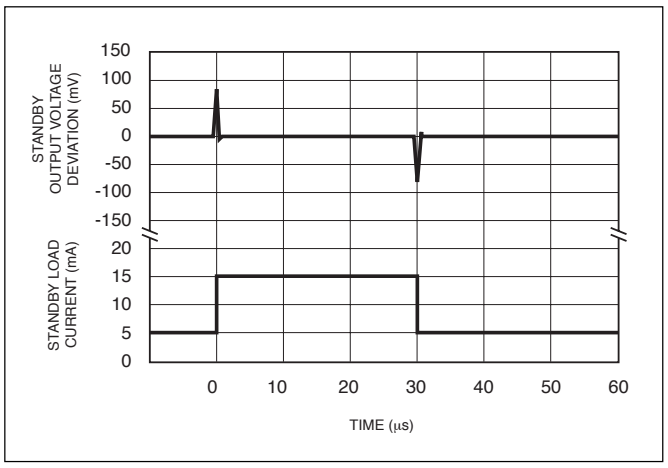
Typical Performance Characteristics: continued



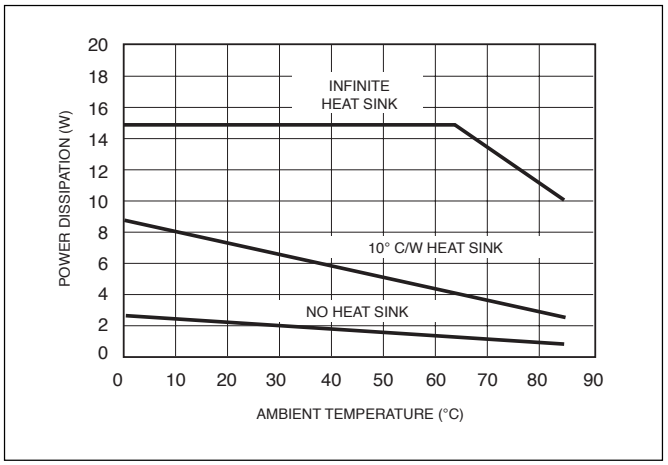
Load Transient Response (V_{OUT1})



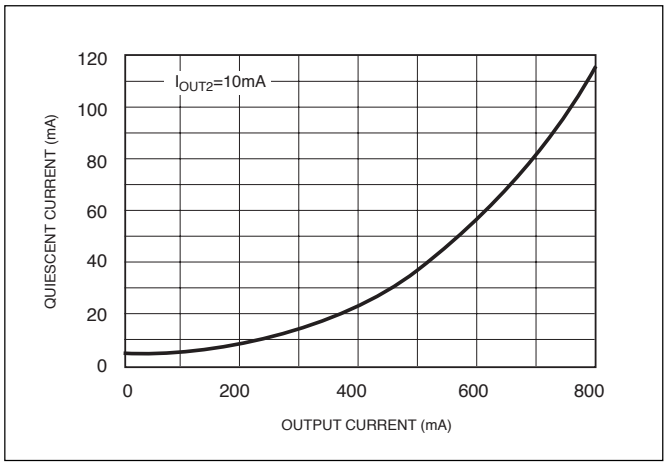
Quiescent Current vs. Standby Output Current



Load Transient Response (V_{OUT2})



Maximum Power Dissipation (TO-220)



Quiescent Current vs. Output Current

Definition of Terms

Dropout Voltage
The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage
The DC voltage applied to the input with respect to ground.

Input Output Differential
The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation
The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation
The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability
Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage
The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

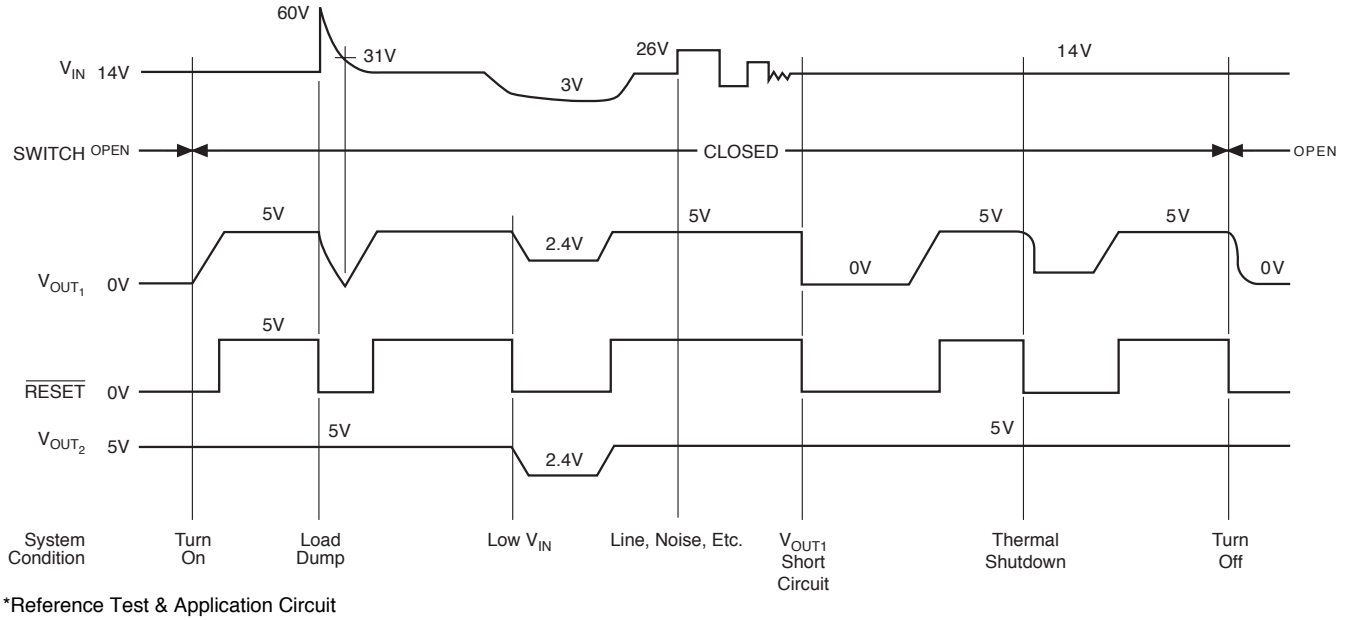
Quiescent Current
The part of the positive input current that does not contribute to the positive load current. i.e., the regulator ground lead current.

Ripple Rejection
The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of V_{OUT}
The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

Current Limit
Peak current that can be delivered to the output.

Typical Circuit Waveform



*Reference Test & Application Circuit

Circuit Description

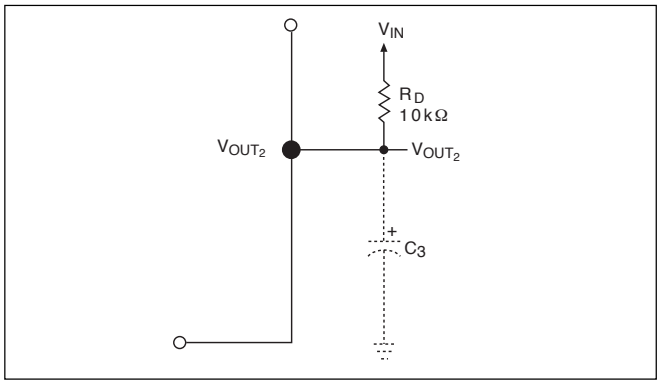
Standby Output

The CS8135 is equipped with two outputs. The second output is intended for use in systems requiring standby memory circuits. While the high current regulator output can be controlled with the $\overline{\text{RESET}}$ lead described below, the standby output remains on under all conditions as long as sufficient input voltage is applied to the IC. Thus, memory and other circuits powered by this output remain unaffected by positive line transients, thermal shutdown, etc.

The standby regulator circuit is designed so that the quiescent current to the IC is very low (<3mA) when the other regulator output is off.

In applications where the standby output is not needed, it may be disabled by connecting a resistor from the standby output to the supply voltage. This eliminates the need for a capacitor on the output to prevent unwanted oscillations. The value of the resistor depends upon the minimum input voltage expected for a given system. Since the standby output is shunted with an internal diode zener, the current through the external resistor should be sufficient to bias V_{OUT2} up to this point. Approximately 60μA will suffice, resulting in a 10kΩ external resistor for most applications.

Circuit Description: continued



Disabling V_{OUT2} when it is not needed. C3 is no longer needed.

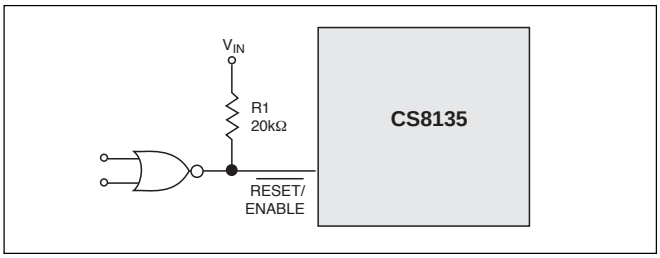
High Current Output

Unlike the standby regulated output, which must remain on whenever possible, the high current regulated output is fault protected against overvoltage and also incorporates thermal shutdown. If the input voltage rises above approximately 30V (e.g., load dump), this output will automatically shutdown. This protects the internal circuitry and enables the IC to survive higher voltage transients than would otherwise be expected. Thermal shutdown is effective against die overheating since the high current output is the dominant source of power dissipation in the IC.

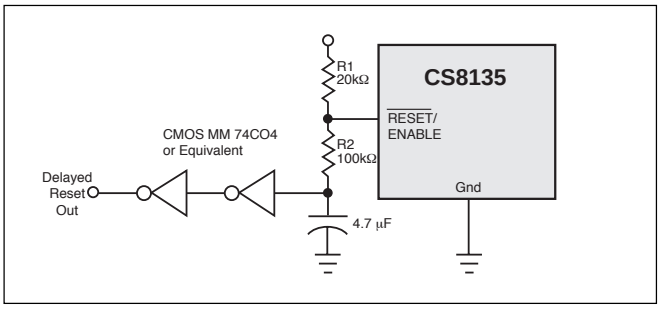
$\overline{\text{RESET}}$ Function

The $\overline{\text{RESET}}$ function has the ability to serve a dual purpose if desired. When controlled in the manner shown in the test circuit (common in automotive systems where $\overline{\text{RESET}}$ /ENABLE is connected to the ignition switch), the lead also serves as an output flag that is active low whenever a fault condition is detected with the high current regulated output. Under normal operating conditions, the output voltage of this lead is high (5V). This is set by an internal clamp. If the high current output becomes unregulated for any reason (line transients, short circuit, thermal shutdown, low input voltage, etc.) the lead switches to the active low state, and is capable of sinking several milliamps. This output signal can be used to initiate any reset or start-up procedure that may be required of the system.

The $\overline{\text{RESET}}$ lead can also be driven directly from logic circuits. The only requirement is that the 20kΩ pull-up resistor remain in place. This will not affect the logic gate since the voltage on this lead is limited by the internal clamp to 5V. The $\overline{\text{RESET}}$ signal is sacrificed in this arrangement since the maximum sink capability of the lead in the active low state (approximately 5mA), is usually not sufficient to pull down the active high logic gate. The flag can be retained if the driving gate is open collector logic.



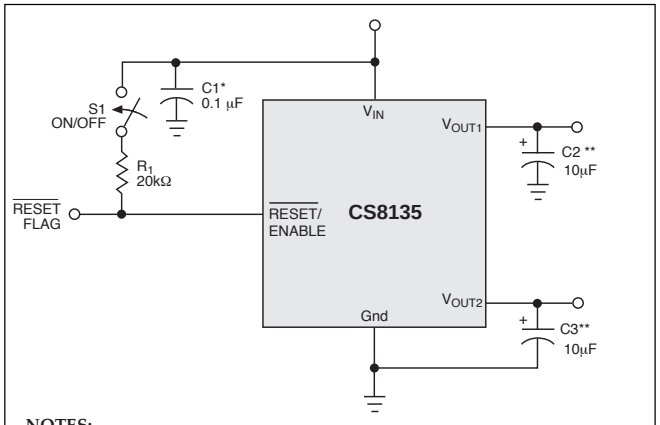
Controlling ON/OFF Terminal with a typical CMOS or TTL Logic Gate



Reset Pulse on Power-Up (with approximately 300ms delay)

Application Notes

Test & Application Circuit



NOTES:
* C1 required if regulator is located far from power supply filter.
** C2, C3 required for stability.

Stability Considerations

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR, can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (-25°C to -40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for output capacitor C_2 shown in the test and applications circuit should work for most applications, however it is not necessarily the optimized solution.

To determine acceptable values for C_2 and C_3 for a particular application, start with a tantalum capacitor of the rec-

ommended value and work towards a less expensive alternative part for each output.

Step 1: Place the completed circuit with the tantalum capacitors of the recommended values in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with capacitor C_2 will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load on the output under observation and look for oscillations on the output. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the output at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

Step 7: Remove the unit from the environmental chamber and heat the IC with a heat gun. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of ±20% so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than 50% of the maximum allowable ESR found in step 3 above.

Repeat steps 1 through 7 with the capacitor on the other output, C_3.

Calculating Power Dissipation in a Dual Output Linear Regulator

The maximum power dissipation for a dual output regulator (Figure 1) is:

$$P_{D(max)} = \{V_{IN(max)}-V_{OUT1(min)}\}I_{OUT1(max)}+ \{V_{IN(max)}-V_{OUT2(min)}\}I_{OUT2(max)}+V_{IN(max)}I_Q \quad (1)$$

Where

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT1(min)}$ is the minimum output voltage from V_{OUT1},

$V_{OUT2(min)}$ is the minimum output voltage from V_{OUT2},

$I_{OUT1(max)}$ is the maximum output current for the application,

$I_{OUT2(max)}$ is the maximum output current, for the application, and

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\Theta JA}$ can be calculated:

$$R_{\Theta JA} = \frac{150°C - T_A}{P_D} \quad (2)$$

The value of $R_{\Theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\Theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

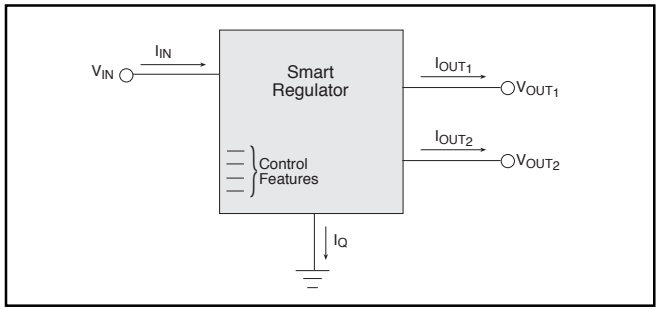


Figure 1: Dual output regulator with key performance parameters labeled.

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\Theta JA}$.

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA} \quad (3)$$

where

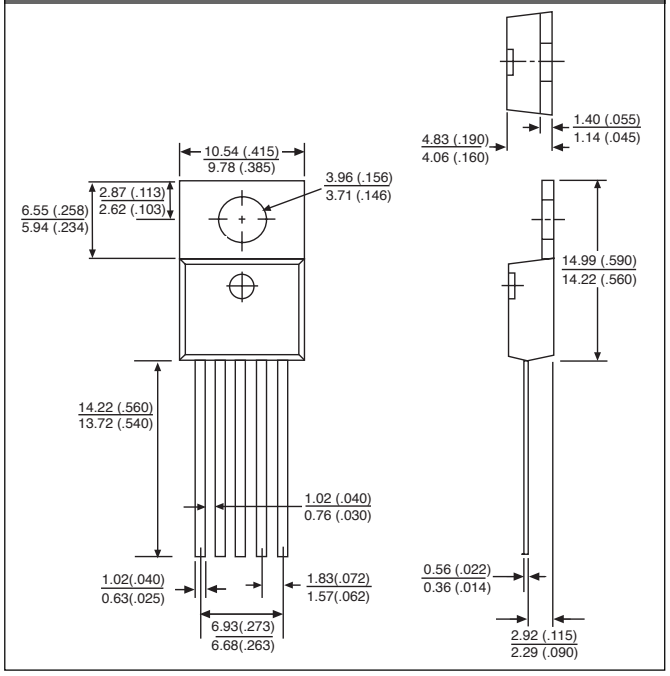
$R_{\Theta JC}$ = the junction-to-case thermal resistance,
$R_{\Theta CS}$ = the case-to-heatsink thermal resistance, and
$R_{\Theta SA}$ = the heatsink-to-ambient thermal resistance.

$R_{\Theta JC}$ appears in the package section of the data sheet. Like $R_{\Theta JA}$, it too is a function of package type. $R_{\Theta CS}$ and $R_{\Theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

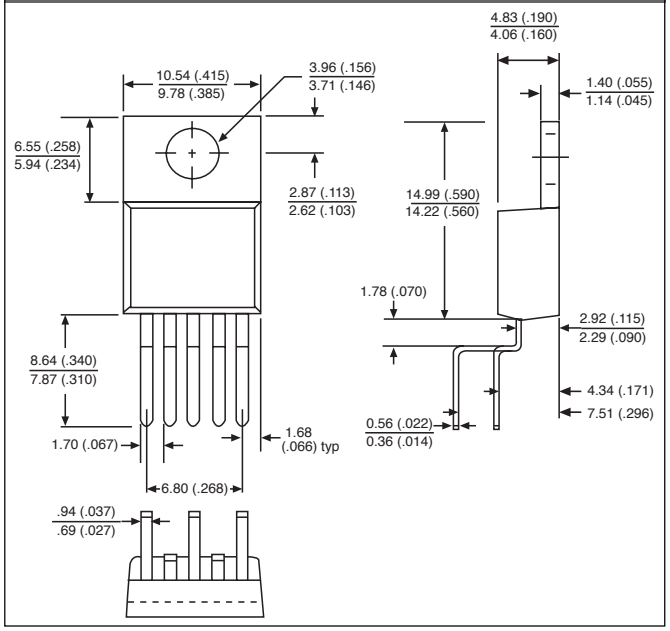
Package Specification

Package Dimensions in MM (Inches)

5 Lead TO-220 (T) Straight



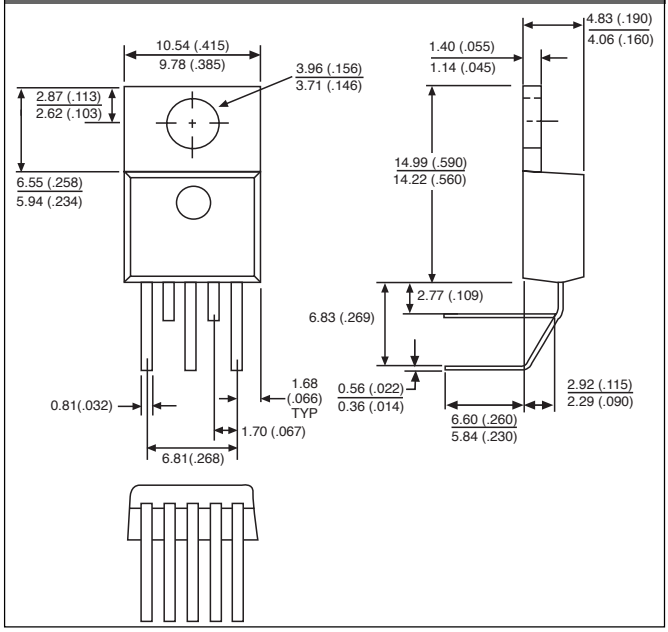
5 Lead TO-220 (TVA) Vertical



PACKAGE THERMAL DATA

Thermal Data		5 Lead TO-220	
$R_{\Theta JC}$	typ	2.3	°C/W
$R_{\Theta JA}$	typ	50	°C/W

5 Lead TO-220 (THA) Horizontal



Ordering Information

Part Number	Description
CS8135YT5	5 Lead TO-220 Straight
CS8135YTVA5	5 Lead TO-220 Vertical
CS8135YTHA5	5 Lead TO-220 Horizontal

Cherry Semiconductor Corporation reserves the right to make changes to the specifications without notice. Please contact Cherry Semiconductor Corporation for the latest available information.