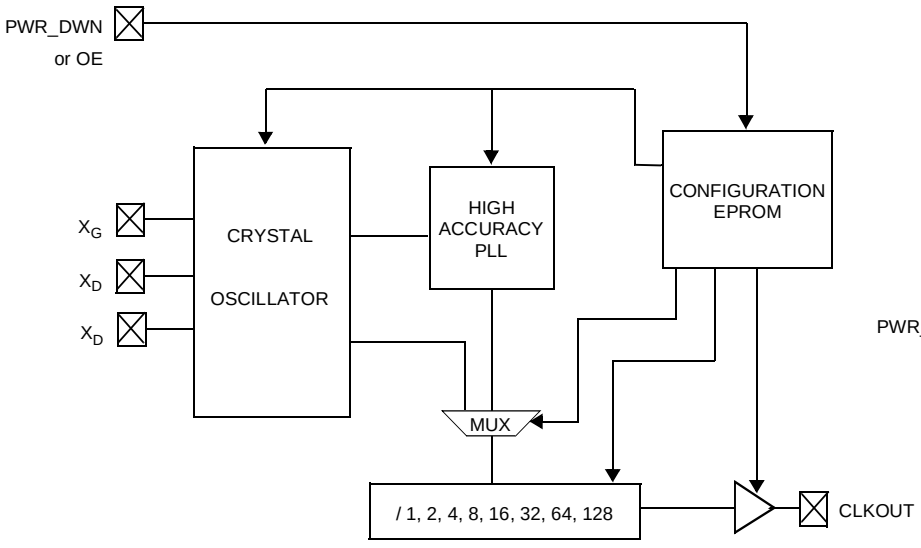
PRELIMINARY

CY2037

High Accuracy EPROM Programmable PLL Die for Crystal Oscillators

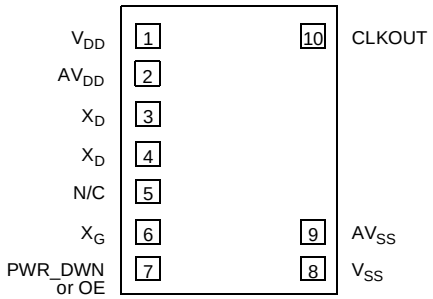
Features	Benefits
• EPROM-programmable die for in-package programming of crystal oscillators	Enables quick turnaround of custom oscillators Lowers inventory costs through stocking of blank parts
• High resolution PLL with 12 bit multiplier and 10 bit divider	Enables synthesis of highly accurate and stable output clock frequencies with zero or low PPM
• EPROM-programmable capacitor tuning array	Enables fine-tuning of output clock frequency by adjusting C_{Load} of the crystal
• Twice programmable die	Enables reprogramming of programmed part, to correct errors, and control excess inventory
• Simple 4-wire programming interface	Enables programming of output frequency after packaging
• On-chip oscillator runs from 10–30 MHz crystal	Lowers cost of oscillator as PLL can be programmed to a high frequency using a low-frequency, low-cost crystal
• EPROM-selectable TTL or CMOS duty cycle levels	Duty cycle centered at 1.5V or $V_{DD}/2$ Provides flexibility to service most TTL or CMOS applications
• Operating frequency — 1–200 MHz at 5V — 1–100 MHz at 3.3V — 1–66.67 MHz at 2.7V	Services most PC, networking, and consumer applications
• Sixteen selectable post-divide options, using either PLL or reference oscillator output	Provides flexibility in output configurations and testing
• Programmable PWR_DWN or OE pin	Enables low-power operation or output enable function
• Programmable asynchronous or synchronous OE and PWR_DWN modes	Provides flexibility for system applications, through selectable instantaneous or synchronous change in outputs
• Low Jitter outputs — < ±100ps (pk-pk) at 5V — < ±125ps (pk-pk) at 3.3V	Suitable for most PC, consumer, and networking applications
• 3.3V or 5V operation	Lowers inventory cost as same die services both applications
• Small Die	Enables encapsulation in small-size, surface mount packages
• Controlled rise and fall times and output slew rate	Has lower EMI than oscillators

CY2037 Logic Block Diagram



Die Configuration

Top View



Functional Description

The CY2037 is an EPROM programmable, high accuracy, PLL-based die designed for the crystal oscillator market. The die attaches directly to a low-cost 10-30MHz crystal and can be packaged into 4-pin through-hole or surface mount packages. The oscillator devices can be stocked as blank parts and custom frequencies programmed in-package at the last stage before shipping. This enables fast-turn manufacture of custom and standard crystal oscillators without the need for dedicated, expensive crystals.

The CY2037 contains an on-chip oscillator and a unique oscillator tuning circuit for fine-tuning of the output frequency. The crystal C_{load} can be selectively adjusted by programming a set of seven EPROM bits. This feature can be used to compensate for crystal variations or to obtain a more accurate synthesized frequency.

The CY2037 uses EPROM programming with a simple 2-wire, 4-pin interface that includes V_{SS} and V_{DD}. Clock outputs can be generated up to 200 MHz at 5V or up to 100 MHz at 3.3V. The entire configuration can be reprogrammed one time allowing programmed inventory to be altered or reused.

The CY2037 PLL die has been designed for very high resolution. It has a 12 bit feedback counter multiplier and a 10 bit reference counter divider. This enables the synthesis of highly accurate and stable output clock frequencies with zero or low PPM. The clock can be further modified by eight output divider options of 1, 2, 4, 8, 16, 32, 64 and 128. The divider input can be selected as either the PLL or crystal oscillator output providing a total of sixteen separate output options. For further flexibility, the ouput is selectable between TTL and CMOS duty cycle levels.

The CY2037 also contains flexible power management control. The part includes both PWR_DWN and OE features with integrated pull-up resistors. The PWR_DWN and OE modes have an additional setting to determine timing (asynchronous or synchronous) with respect to the output signal.

Controlled rise and fall times, unique output driver circuits, and innovative circuit layout techniques enable the CY2037 to have low jitter and accurate outputs making it suitable for most PC, networking and consumer applications

EPROM Configuration Block

The following table summarizes the features which are configurable by EPROM. Please refer to the “CY2037 Programming Specification” for further details. The specification can be obtained from your local Cypress representative.

EPROM Adjustable Features
Feedback counter value (P)
Reference counter value (Q)
Output divider selection
Oscillator Tuning (load capacitance values)
Duty cycle levels (TTL or CMOS)
Power management mode (OE or PWR_DWN)
Power management timing (synchronous or asynchronous)

PLL Output Frequency

The CY2037 contains a high resolution PLL with 12 bit multiplier and 10 bit divider.The output frequency of the PLL is determined by the following formula:

$$F_{PLL} = \frac{2 \bullet (P + 5)}{(Q + 2)} \bullet F_{REF}$$

where P is the feedback counter value and Q is the reference counter value. P and Q are EPROM programmable values.

Power Management features

The CY2037 contains EPROM programmable PWR_DWN and OE functions. If Powerdown is selected, all active circuitry on the chip is shut down when the control pin goes low. The output is forced to a hard low in this mode and the oscillator and PLL circuits must re-lock when the part leaves the Powerdown mode. If Output Enable mode is selected, the output is three-stated when the Control pin goes low. In this mode the oscillator and PLL circuits continue to operate, allowing a rapid return to normal operation when the Control input is deasserted.

In addition, the PWR_DWN and OE modes can be programmed to occur synchronously or asynchronously with respect to the output signal. When the asynchronous setting is used, the powerdown or output three-state occurs immediately (allowing for logic delays) irrespective of position in the clock cycle. However, when the synchronous setting is used, the part waits for a falling edge at the output before powerdown or output enable is initiated, thus preventing output glitches.

Crystal Oscillator Tuning Circuit

The CY2037 contains a unique tuning circuit to fine-tune the output frequency of the device. The tuning circuit consists of an array of seven load capacitors on the input side of the oscillator drive inverter. The capacitor load values are EPROM programmable and can be increased in small increments. As the capacitor load is increased the circuit is fine-tuned to a lower frequency. The capacitor load values vary from 0.17pF to 8 pF for a 100:1 total control ratio. The tuning increments are shown in the table below

Table 1. Crystal Tuning Increments

+8pF	+4.2pF	+2.2pF	+1.2pF	+0.6pF	+0.3pF	+0.17pF

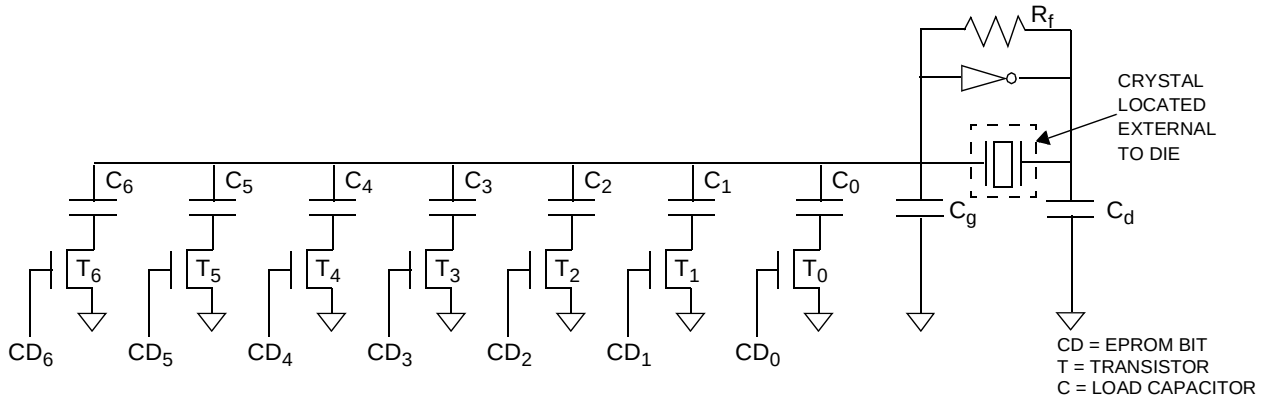
Die Pad Summary

Name	Die Pad	Description
V_{DD}	1	Digital voltage supply
AV_{DD}	2	Analog voltage supply, 3.3V or 5V
V_{SS}	8	Digital Ground
AV_{SS}	9	Analog Ground
X_D	3,4	Crystal connection, drain pad. Bond to crystal drain.
X_G	6	Crystal connection, gate pad. Bond to crystal gate.
PWR_DWN / OE	7	EPROM programmable power down or output enable pad. Serves as V_{PP} in programming mode.
CLKOUT	10	Clock output. Also serves as three-state input during programming.
N/C	5	No Connect. Do not connect.

Device Functionality: Output Frequencies

Symbol	Description	Condition	Min.	Max.	Unit
Fo	Output frequency	V_{DD} = 4.5–5.5V	1	200	MHz
		V_{DD} = 3.0–3.6V	1	100	MHz
		V_{DD} = 2.7–3.6V	1	66	MHz

Crystal Oscillator Tuning Circuit



Symbol	Description	Min	Typ	Max	Unit
R_f	Feedback resistor, V_{DD} = 4.5–5.5V Feedback resistor, V_{DD} = 3.0–3.6V	0.5 1.0	2 4	3.5 9.0	MΩ MΩ
C_g	Gate capacitor	6.4	8	9.6	pF
C_d	Drain Capacitor	12	15	18	pF
C_0	Series Cap	0.14	0.17	0.20	pF
C_1	Series Cap	0.26	0.32	0.38	pF
C_2	Series Cap	0.49	0.61	0.73	pF
C_3	Series Cap	0.93	1.16	1.39	pF
C_4	Series Cap	1.77	2.21	2.65	pF
C_5	Series Cap	3.36	4.2	5.04	pF
C_6	Series Cap	6.4	8	9.6	pF

Absolute Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage.....–0.5 to +7.0V

Input Voltage.....–0.5V to V_{DD}+0.5

Storage Temperature (Non-Condensing)... –55°C to +150°C

Junction Temperature ..... –55°C to +150°C

Static Discharge Voltage ..... >2000V (per MIL-STD-883, Method 3015)

Operating Conditions

Parameter	Description	Min.	Max.	Unit
AV_{DD}, V_{DD}	Analog and Digital Supply Voltage	2.7	5.5	V
T_{AJ} [1]	Operating Temperature, Junction	–40	+100	°C
C_{TTL}	Max. Capacitive Load on outputs for TTL levels V_{DD} = 4.5–5.5V, Output frequency = 1–40 MHz V_{DD} = 4.5–5.5V, Output frequency = 40–125 MHz V_{DD} = 4.5–5.5V, Output frequency = 125–200 MHz		 50 25 15	 pF pF pF
C_{CMOS}	Max. Capacitive Load on outputs for CMOS levels V_{DD} = 4.5–5.5V, Output frequency = 1–66.6 MHz V_{DD} = 4.5–5.5V, Output frequency = 66.6–125 MHz V_{DD} = 4.5–5.5V, Output frequency = 125–200 MHz V_{DD} = 3.0–3.6V, Output frequency = 1–50 MHz V_{DD} = 3.0–3.6V, Output frequency = 50–100 MHz V_{DD} = 2.7–3.6V, Output frequency = 1–66.6 MHz		 50 25 15 30 15 15	 pF pF pF pF pF pF
X_{REF}	Reference Frequency, input crystal	10	30	MHz

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low-level Input Voltage	V_{DD} = 4.5–5.5V V_{DD} = 3.0–3.6V V_{DD} = 2.7–3.6V			0.8 $0.2V_{DD}$ $0.2V_{DD}$	V V V
V_{IH}	High-level Input Voltage	V_{DD} = 4.5–5.5V V_{DD} = 3.0–3.6V V_{DD} = 2.7–3.6V	2.0 $0.5V_{DD}$ $0.5V_{DD}$			V V V
V_{OL}	Low-level Output Voltage	V_{DD} = 4.5–5.5V, I_{OL}= 16 mA V_{DD} = 3.0–3.6V, I_{OL}= 8 mA V_{DD} = 2.7–3.6V, I_{OL}= 8 mA			0.4 0.4 0.4	V V V
V_{OHCMOS}	High-level Output Voltage, CMOS levels	V_{DD} = 4.5–5.5V, I_{OH}= –16 mA V_{DD} = 3.0–3.6V, I_{OH}= –8 mA V_{DD} = 2.7–3.6V, I_{OH}= –8 mA	V_{DD}–0.4 V_{DD}–0.4 V_{DD}–0.4			V V V
V_{OHTTL}	High-level Output Voltage, TTL levels	V_{DD} = 4.5–5.5V, I_{OH}= –16 mA	2.4			V
I_{IL}	Input Low Current	V_{IN} = 0V			10	µA
I_{IH}	Input High Current	V_{IN} = V_{DD}			5	µA
I_{DD}	Power Supply Current, Unloaded	V_{DD} = 4.5–5.5V, Output frequency <= 200 MHz V_{DD} = 3.0–3.6V, Output frequency <= 100 MHz V_{DD} = 2.7–3.6V, Output frequency <= 66.6 MHz			45 25 20	mA mA mA
I_{DDS}	Stand-by current	V_{DD} = 4.5–5.5V V_{DD} = 3.0–3.6V V_{DD} = 2.7–3.6V		10 2 2	50 20 20	µA µA µA
Rup	Input pull-Up resistor	V_{DD} = 4.5–5.5V, V_{IN} = 0V V_{DD} = 4.5–5.5V, V_{IN} = $0.7V_{DD}$	1.1 15	3.0 30	8.0 100	MΩ kΩ

Note:

1. This product is sold in die form so operating conditions are specified for the die, or junction temperature

Output Clock Switching Characteristics Over the Operating Range

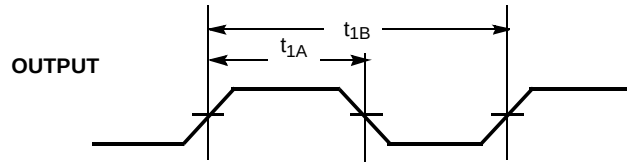
Symbol	Description	Test Conditions	Min	Typ	Max	Unit
t_{1w}	Output Duty Cycle at 1.4V, V_{DD} = 4.5–5.5V $t_{1w} = t_{1A} \div t_{1B}$	1–27 MHz, C_L <= 50 pF 27–80 MHz, C_L <= 15pF 27–125 MHz, C_L <= 25pF 125–200 MHz, C_L <= 15pF	45 45 40 40		55 55 60 60	% % % %
t_{1x}	Output Duty Cycle at $V_{DD}/2$, V_{DD} = 4.5–5.5V $t_{1x} = t_{1A} \div t_{1B}$	1–66.6 MHz, C_L <= 50 pF 66.6–125 MHz, C_L <= 25 pF 125–200 MHz, C_L <= 15pF	45 40 40		55 60 60	% % %
t_{1y}	Output Duty Cycle at $V_{DD}/2$, V_{DD} = 3.0–3.6 $t_{1y} = t_{1A} \div t_{1B}$	1–50 MHz, C_L <= 30 pF 50–100 MHz, C_L <= 15pF	45 40		55 60	% %
t_{1z}	Output Duty Cycle at $V_{DD}/2$, V_{DD} = 2.7–3.6V $t_{1z} = t_{1A} \div t_{1B}$	1–40 MHz, C_L <= 15 pF 40–66.6 MHz, C_L <= 15 pF	45 40		55 60	% %
t_2	Output Clock Rise time	Between 0.8 –2.0V, V_{DD} = 4.5V–5.5V, C_L = 50 pF Between 0.8 –2.0V, V_{DD} = 4.5V–5.5V, C_L = 25 pF Between 0.8 –2.0V, V_{DD} = 4.5V–5.5V, C_L = 15 pF Between $0.2V_{DD}$– $0.8V_{DD}$, V_{DD}= 4.5V–5.5V, C_L = 50 pF Between $0.2V_{DD}$– $0.8V_{DD}$, V_{DD}= 3.0V–3.6V, C_L = 30 pF Between $0.2V_{DD}$– $0.8V_{DD}$, V_{DD}= 3.0V–3.6V, C_L = 15 pF Between $0.2V_{DD}$– $0.8V_{DD}$, V_{DD}= 2.7V–3.6V, C_L = 15 pF			1.8 1.2 0.9 3.4 4.0 2.4 4.0	ns ns ns ns ns ns ns
t_3	Output Clock Fall time	Between 0.8V–2.0V, V_{DD} = 4.5V–5.5V, C_L = 50 pF Between 0.8 –2.0V, V_{DD} = 4.5V–5.5V, C_L = 25 pF Between 0.8 –2.0V, V_{DD} = 4.5V–5.5V, C_L = 15 pF Between $0.2V_{DD}$– $0.8V_{DD}$, V_{DD}= 4.5V-5.5V, C_L = 50 pF Between $0.2V_{DD}$– $0.8V_{DD}$, V_{DD}= 3.0V–3.6V, C_L = 30 pF Between $0.2V_{DD}$– $0.8V_{DD}$, V_{DD}= 3.0V–3.6V, C_L = 15 pF Between $0.2V_{DD}$– $0.8V_{DD}$, V_{DD}= 2.7V–3.6V, C_L = 15 pF			1.8 1.2 0.9 3.4 4.0 2.4 4.0	ns ns ns ns ns ns ns
t_4	Start-up time out of power-down	PWR_DWN or OE pin LOW to HIGH[2]		1	2	ms
t_{5a}	Power Down delay time (synchronous setting)	PWR_DWN pin HIGH to output LOW (T=frequency oscillator period)		T/2	T+10	ns
t_{5b}	Power Down delay time (asynchronous setting)	PWR_DWN pin HIGH to output LOW		10	15	ns
t_6	Power Up time	From power on[2]		1	2	ms
t_{7a}	Output disable time (synchronous setting)	OE pin HIGH to output Hi-Z (T=frequency oscillator period)		T/2	T+10	ns
t_{7b}	Output disable time (asynchronous setting)	OE pin HIGH to output Hi-Z		10	15	ns
t_8	Output enable time	PWR_DWN or OE pin LOW to HIGH			100	ns
t_9	Peak-to-Peak Period Jitter	V_{DD}= 4.5V–5.5V, Fo > 33 MHz, VCO > 100 MHz V_{DD}= 3.0V–3.6V, Fo > 33 MHz, VCO >100 MHz V_{DD}= 3.0V–5.5V, Fo <33 MHz		±50 ±75 ±100	±100 ±125 ±250	ps ps ps

Note:

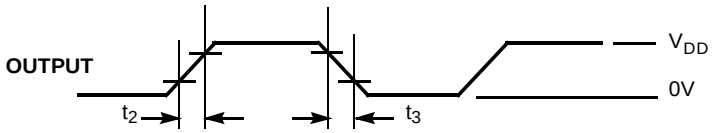
2. Oscillator start time cannot be guaranteed for all crystal types. This specification is for operation with AT cut crystals with ESR < 70 ohms.

Switching Waveforms

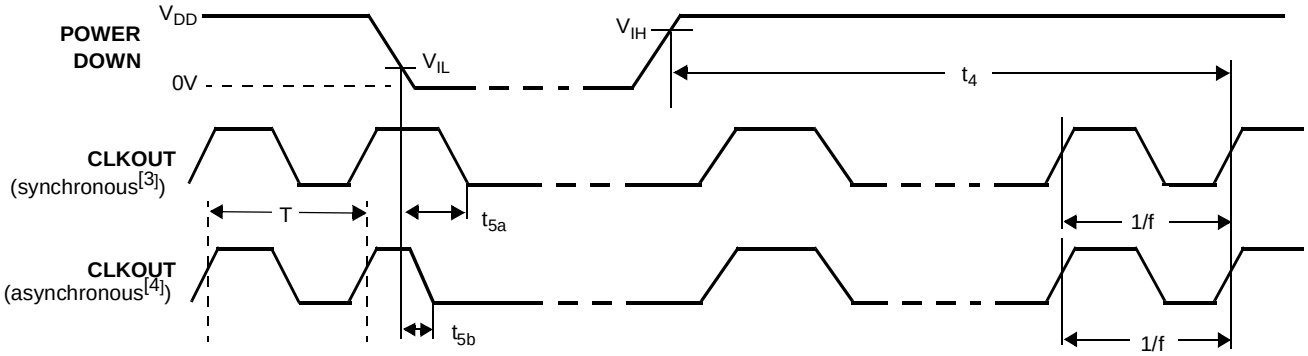
Duty Cycle Timing (t_{1w}, t_{1x}, t_{1y}, t_{1z})



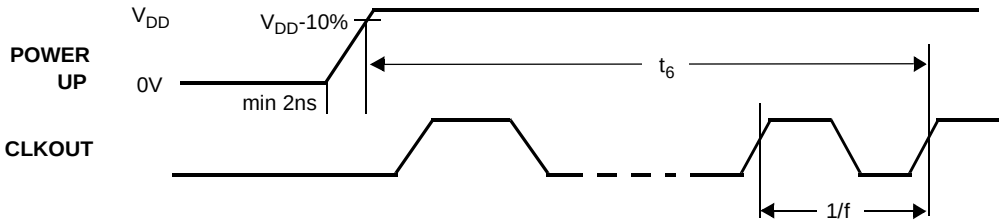
Output Rise/Fall Time



Power Down Timing (synchronous and asynchronous modes)



Power Up Timing

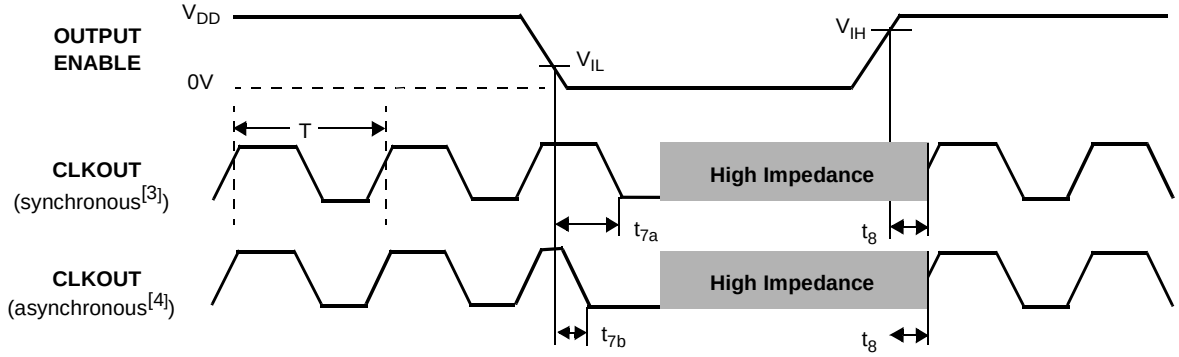


Notes:

3. In synchronous mode the powerdown or output 3-state is not initiated until the next falling edge of the output clock.
4. In asynchronous mode the powerdown or output 3-state occurs within 25ns irrespective of position in the ouput clock cycle.

Switching Waveforms (continued)

Output Enable Timing (synchronous and asynchronous modes)



Ordering Information

Ordering Code	Type	Operating Range
CY2037WAF	Wafer	Industrial

Die Size Dimensions

x by y	1497x1105 microns
Wafer Thickness	14 ±0.5 mils

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