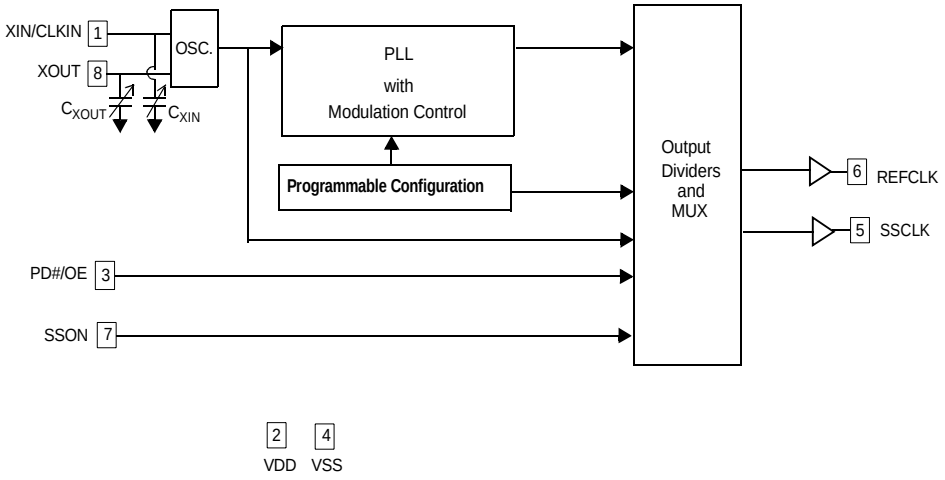
Programmable Spread Spectrum Clock Generator for EMI Reduction

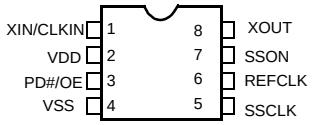
Features	Benefits
• **Wide operating output (SSCLK) frequency range** **— 3–200 MHz**	Services most PC peripherals, networking, and consumer applications.
• **Programmable spread spectrum with nominal 30-kHz modulation frequency.** **— Center spread: ±0.25% to ±2.5%** **— Down spread: –0.5% to –5.0%**	Provides wide range of spread percentages for maximum EMI reduction, to meet regulatory agency Electro Magnetic Compliance (EMC) requirements. Reduces development and manufacturing costs and time-to-market.
• **Input frequency range** **— External crystal: 8–30 MHz fundamental crystals.** **— External reference: 8–166 MHz Clock**	Eliminates the need for expensive and difficult to use higher order crystals.
• **Integrated phase-locked loop (PLL)**	Internal PLL to generate up to 200-MHz output. Able to generate custom frequencies from an external crystal or a driven source.
• **Programmable crystal load capacitor tuning array**	Enables fine-tuning of output clock frequency by adjusting C_{Load} of the crystal. Eliminates the need for external C_{Load} capacitors.
• **Low cycle-to-cycle Jitter**	Suitable for most PC, consumer, and networking applications
• **3.3V operation**	Application compatibility in standard and low-power systems.
• **Spread spectrum On/Off function**	Provides ability to enable or disable spread spectrum with an external pin.
• **Power-down or Output Enable function**	Enables low-power state or output clocks to High-Z state.

Logic Block Diagram



Pin Configuration

CY25000
8-pin SOIC



General Description

The CY25000 is a Spread Spectrum Clock Generator (SSCG) IC used for the purpose of reducing Electro Magnetic Interference (EMI) found in today's high-speed digital electronic systems.

The device uses a Cypress proprietary Phase-Locked Loop (PLL) and Spread Spectrum Clock (SSC) technology to synthesize and modulate the frequency of the input clock. By frequency modulating the clock, the measured EMI at the fundamental and harmonic frequencies are greatly reduced. This reduction in radiated energy can significantly reduce the cost of complying with regulatory agency requirements (EMC) and improve time to market without degrading system performance.

The CY25000 uses a factory-programmable configuration memory array to synthesize output frequency, spread %, crystal load capacitor, reference clock on/off and PD#/OE options.

The spread % is factory programmed to either center spread or down spread with various spread percentages. The range for center spread is from ±0.25% to ±2.50%. The range for down spread is from –0.5% to –5.0%. Contact the factory for smaller or larger spread % amounts if required.

The input to the CY25000 can be either a crystal or a clock signal. The input frequency range for crystals is 8–30 MHz, and for clock signals is 8–166 MHz.

The CY25000 has two clock outputs, REFCLK and SSCLK. The non-spread spectrum REFCLK output has the same frequency as the input of the CY25000. The frequency modulated SSCLK output can be programmed from 3–200 MHz.

The CY25000 products are available in an 8-pin SOIC (150-mil) package with a commercial operating temperature range of 0 to 70°C.

Pin Description

Pin	Name	Description
1	XIN/CLKIN	Crystal input or reference clock input
2	VDD	3.3V voltage supply
3	PD#/OE	Power-down pin: Active LOW. If PD# = 0, SSCLK and REFCLK are three-stated. Output Enable pin: Active HIGH. If OE = 1, SSCLK and REFCLK are enabled. User has the option of choosing either PD# or OE function.
4	VSS	GND
5	SSCLK	Spread spectrum clock output
6	REFCLK	Buffered reference output.
7	SSON	Spread spectrum control. 1 = Spread on. 0 = Spread off.
8	XOUT	Crystal output. Leave this pin floating if external clock is used.

Absolute Maximum Rating

Supply Voltage (VDD) ..... –0.5 to +7.0V

DC Input Voltage ..... –0.5V to V_{DD} + 0.5

Storage Temperature (Non-Condensing) .... –55°C to +125°C

Junction Temperature ..... –40°C to +125°C

Data Retention @ Tj=125°C ..... > 10 Years

Package Power Dissipation ..... 350 mW

Static Discharge Voltage ..... $\geq$ 2000V (per MIL-STD-883, Method 3015)

Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3.13	3.30	3.45	V
T_A	Ambient Temperature	0		70	°C
C_{LOAD}	Max. Load Capacitance @ pin 5 and pin 6			15	pF
F_{ref}	External Reference Crystal (Fundamental tuned crystals only)	8		30	MHz
	External Reference Clock	8		166	MHz
F_{SSCLK}	SSCLK output frequency, C_{LOAD} = 15 pF	3		200	MHz
F_{REFCLK}	REFCLK output frequency, C_{LOAD} = 15 pF	8		166	MHz
t_{PU}	Power-up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic)	0.05		500	ms

DC Electrical Characteristics

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} – 0.5$, $V_{DD} = 3.3V$ (source)	12	24		mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DD}= 3.3V$ (sink)	12	24		mA
V_{IH}	Input High Voltage	CMOS levels, 70% of V_{DD}	$0.7V_{DD}$			V
V_{IL}	Input Low Voltage	CMOS levels, 30% of V_{DD}			$0.3V_{DD}$	V
I_{IH}	Input High Current, PD#/OE and SSON pins	$V_{in} = V_{DD}$			10	µA
I_{IL}	Input Low Current, PD#/OE and SSON pins	$V_{in} = V_{SS}$			10	µA
I_{OZ}	Output Leakage Current	Three-state output, PD#/OE = 0	–10		10	µA
C_{XIN}/C_{XOUT}[1, 2]	Programmable Capacitance at pin 1 and pin 8	Capacitance at minimum setting		12		pF
		Capacitance at maximum setting		60		pF
C_{IN}[1]	Input Capacitance at pin 3 and pin 7	Input pins excluding XIN and XOUT		5	7	pF
I_{VDD}	Supply Current	$V_{DD} = 3.45V$, Fin = 30 MHz, REFCLK = 30 MHz, SSCLK = 66 MHz, $C_{LOAD} = 15$ pF, PD#/OE = SSON = V_{DD}		25	35	mA
I_{DDS}	Stand by current	$V_{DD} = 3.45V$, Device powered down with PD#/OE = 0V		15	30	µA

AC Electrical Characteristics[1]

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	SSCLK, Measured at $V_{DD}/2$	45	50	55	%
	Output Duty Cycle	REFCLK, Measured at $V_{DD}/2$ Duty Cycle of CLKIN = 50%.	40	50	60	%
SR1	Rising Edge Slew Rate	SSCLK from 3 to 100 MHz; REFCLK from 10 to 100 MHz. 20%–80% of V_{DD}	0.7	1.1	1.5	V/ns
SR2	Falling Edge Slew Rate	SSCLK from 3 to 100 MHz; REFCLK from 10 to 100 MHz. 80%–20% of V_{DD}	0.7	1.1	1.5	V/ns
SR3	Rising Edge Slew Rate	SSCLK from 100 to 200 MHz; REFCLK from 100 to 166 MHz 20%–80% of V_{DD}	1.2	1.6	2.0	V/ns
SR4	Falling Edge Slew Rate	SSCLK from 100 to 200 MHz; REFCLK from 100 to 166 MHz 80%–20% of V_{DD}	1.2	1.6	2.0	V/ns
tj1	Peak Cycle-to-Cycle Jitter. SSCLK pin	SSCLK = 200 MHz. Spread on		100	200	ps
		SSCLK = 66 MHz. Spread on		150	300	ps
		SSCLK = 14.3 MHz. Spread on		200	400	ps
tj2	Peak Cycle-to-Cycle Jitter, REFCLK	REFCLK output only		100	200	ps
t_{STP}	Power-down Time (pin3 = PD#)	Time from falling edge on PD# to stopped outputs (Asynchronous)		150	300	ns
T_{OE1}	Output Disable Time (pin3 = OE)	Time from falling edge on OE to stopped outputs (Asynchronous)		150	300	ns
T_{OE2}	Output Enable Time (pin3 = OE)	Time from rising edge on OE to outputs at a valid frequency (Asynchronous)		150	300	ns
t_{PU1}	Power-up Time, Crystal is used	Time from rising edge on PD# to outputs at valid frequency (Asynchronous)		3	5	ms
t_{PU2}	Power-up Time, Reference clock is used	Time from rising edge on PD# to outputs at valid frequency (Asynchronous)		2	3	ms

Notes:
1. Guaranteed by characterization, not 100% tested.
2. Contact factory for desired crystal load programming.

Table 1.

Pin Function	Input Frequency	C_{XIN} and C_{XOUT}	Output Frequency	Spread Percent	Reference Output	Power-down or Output Enable	Frequency Modulation
Pin Name	XIN and XOUT	XIN and XOUT	SSCLK	SSCLK	REFOUT	PD#/OE	SSCLK
Pin#	1 and 8	1 and 8	5	5	6	3	5
Units	MHz	pF	MHz	%	On or Off	Select PD# or OE	kHz
Program Value	**ENTER DATA**	**ENTER DATA**	**ENTER DATA**	**ENTER DATA**	**ENTER DATA**	**ENTER DATA**	**30**

Programming Description

The customers planning to use the CY25000 need to provide the programming information described as “ENTER DATA” in *Table 1* and should contact local Cypress Sales.

Additional information on the CY25000 can be obtained from the Cypress web site at www.cypress.com.

Product Functions

Input Frequency (XIN, pin 1 and XOUT, pin 8)

The input to the CY25000 can be a crystal or a clock. The input frequency range for crystals is 8 to 30 MHz, and for clock signal is 8 to 166 MHz.

C_{XIN} and C_{XOUT} (pin 1 and pin 8)

The load capacitors at pin 1 (C_{XIN}) and pin 8 (C_{XOUT}) can be programmed from 12 pF to 60 pF with 0.5-pF increments. The programmed value of these on-chip crystal load capacitors are the same (XIN = XOUT = 12 to 60 pF).

The required values of C_{XIN} and C_{XOUT} can be calculated using the following formula:

$C_{XIN} = C_{XOUT} = 2C_L - C_P$

Where C_L is the crystal load capacitor as specified by the crystal manufacturer and C_P is the parasitic PCB capacitance.

For example, if a fundamental 16-MHz crystal with C_L of 16 pF is used and C_P is 2 pF, C_{XIN} and C_{XOUT} can be calculated as:

$C_{XIN} = C_{XOUT} = (2 \times 16) - 2 = 30$ pF.

If using a driven reference, set C_{XIN} and C_{XOUT} to the minimum value 12 pF.

Output Frequency, SSCLK Output (SSCLK, pin 5)

The modulated frequency at the SSCLK output is produced by synthesizing the input reference clock. The modulation can be stopped by SSON digital control input (SSON = LOW, no modulation). If modulation is stopped, the clock frequency is the nominal value of the synthesized frequency without modulation (spread % = 0). The range of synthesized clock is from 3–200 MHz.

Spread Percentage (SSCLK, pin 5)

The SSCLK frequency can be programmed at any percentage value from ±0.25% to ±2.5% for Center Spread and from –0.5% to –5.0% Down Spread.

Reference Output (REFOUT, pin 6)

The reference clock output has the same frequency and the same phase as the input clock. This output can be programmed to be enabled (clock on) or disabled (High-Z, clock off). If this output is not needed, it is recommended that users request the disabled (High-Z, Clock Off) option.

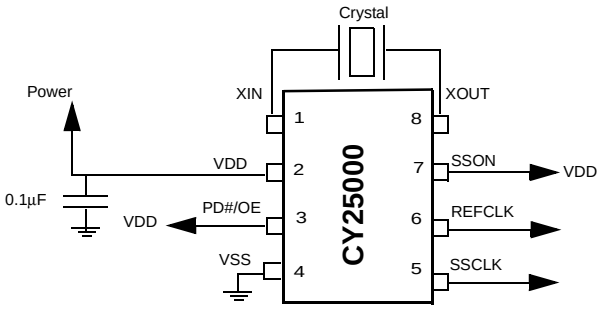
Frequency Modulation

The frequency modulation is programmed at 30 kHz for all SSCLK frequencies from 3 to 200 MHz. Contact the factory if a higher modulation frequency is required.

Power-down or Output Enable (PD# or OE, pin 3):

Users can select either PD# or OE function which are also factory programmable.

Application Circuit[3, 4, 5]

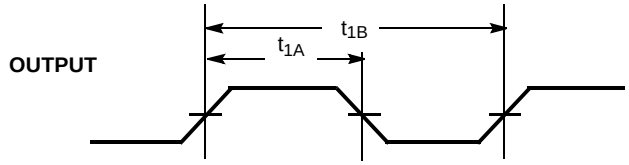


Notes:

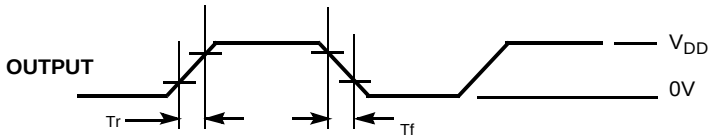
3. Since the load capacitors (C_{XIN} and C_{XOUT}) are provided by the CY25000, no external capacitors are needed on the XIN and XOUT pins to match the crystal load capacitor (C_L). Only a single 0.1-µF bypass capacitor is required on the V_{DD} pin.
4. If an external clock is used, apply the clock to XIN (pin 1) and leave XOUT (pin 8) floating (unconnected).
5. If SSON (pin 7) is LOW (V_{SS}), the frequency modulation will be stopped on SSCLK pin (pin 5).

Switching Waveforms

Duty Cycle Timing (DC = t_{1A}/t_{1B})

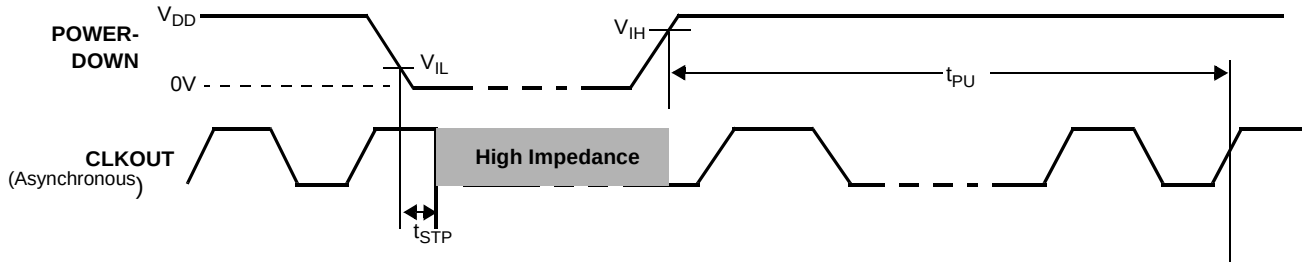


Output Rise/Fall Time (SSCLK and REFCLK)

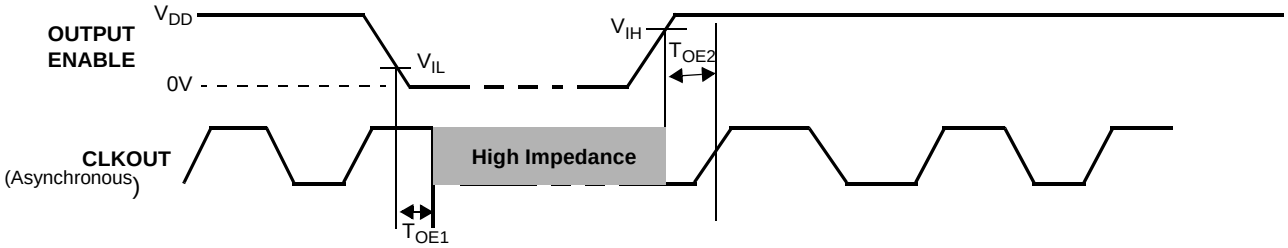


Output Rise time (Tr) = (0.6 x V_{DD})/SR1 (or SR3)
Output Fall time (Tf) = (0.6 x V_{DD})/SR2 (or SR4)
Refer to AC Electrical Characteristics table for SR (Slew Rate) values.

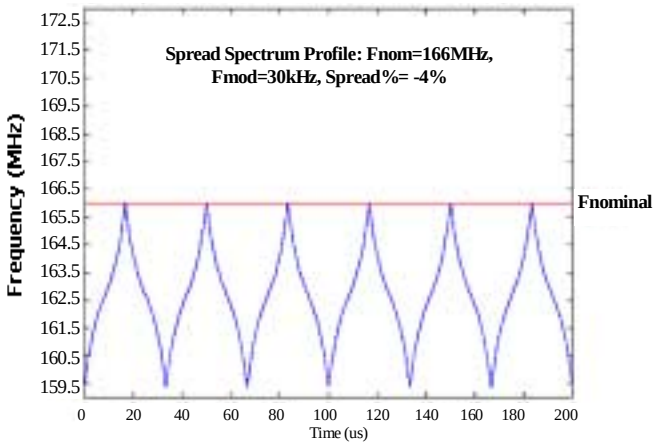
Power-down Timing and Power-up Timing

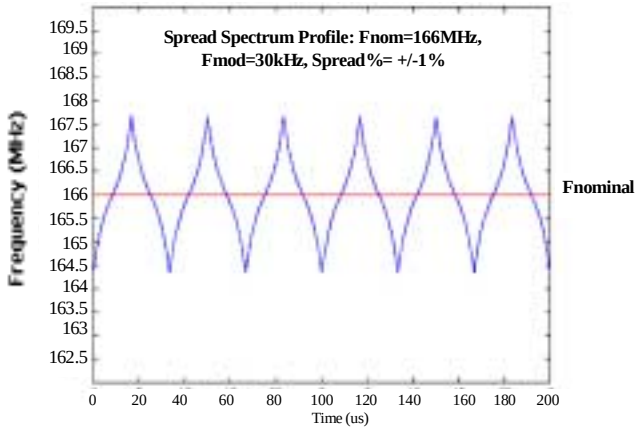


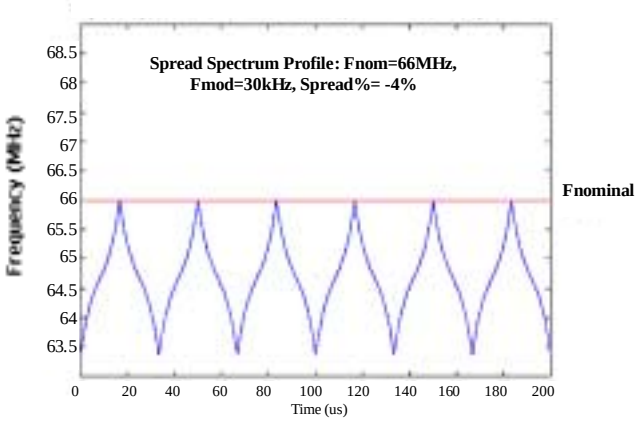
Output Enable/Disable Timing

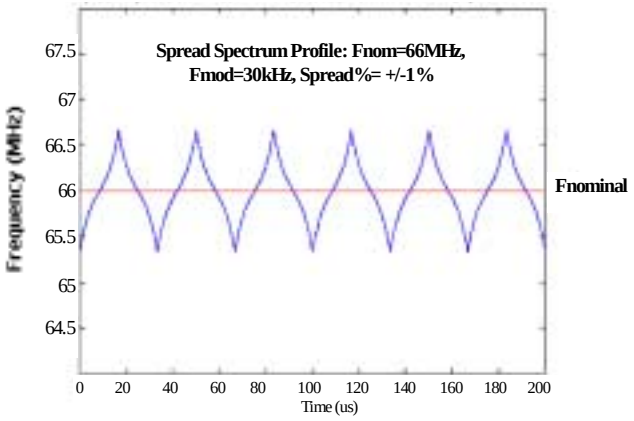


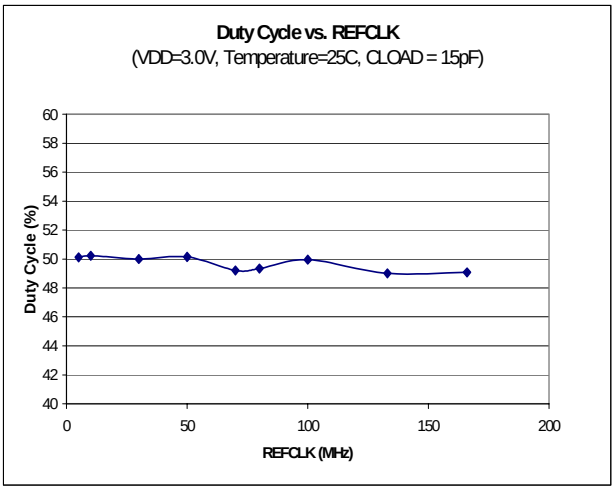
Informational Graphs

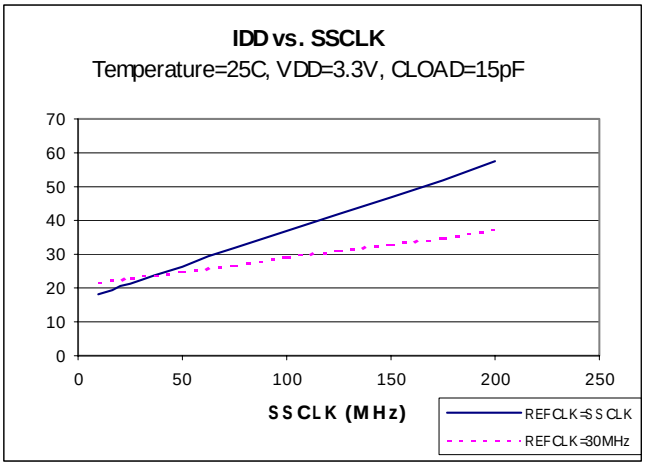




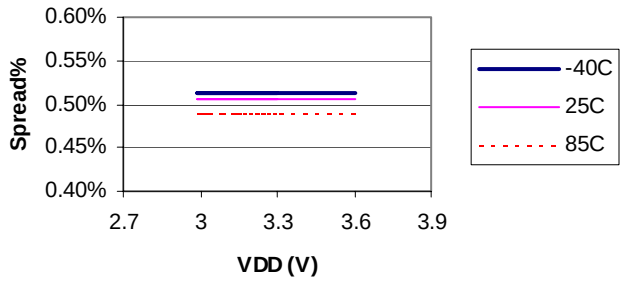




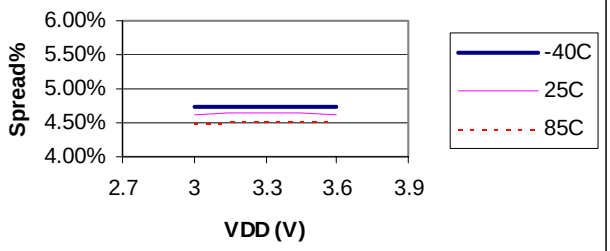




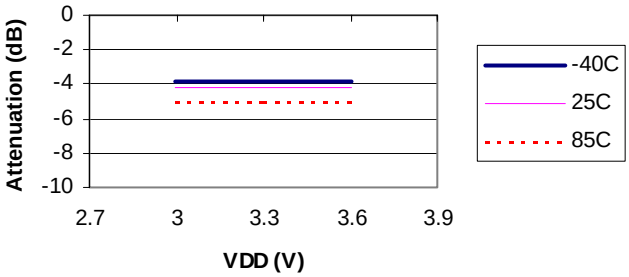
Measured Spread% vs. VDD over Temperature
(Target Spread = 0.5%, Fout=100MHz, C_{LOAD}=15pF)



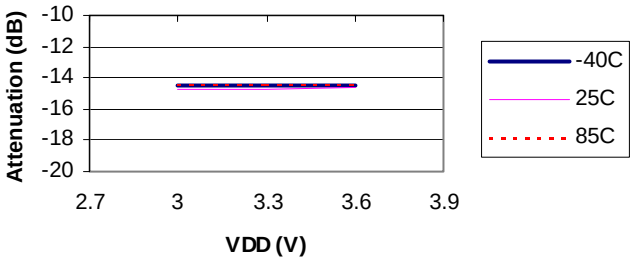
Measured Spread% vs. VDD over Temperature
(Target Spread = 5.0%, Fout=100MHz, C_{LOAD}=15pF)



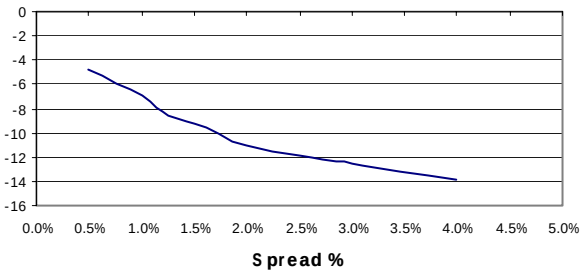
SSCLK Attenduation vs. VDD over Temperature
(Measured at 7th Harmonic with Fnom=100MHz and Spread=0.5%, C_{LOAD}=15pF)



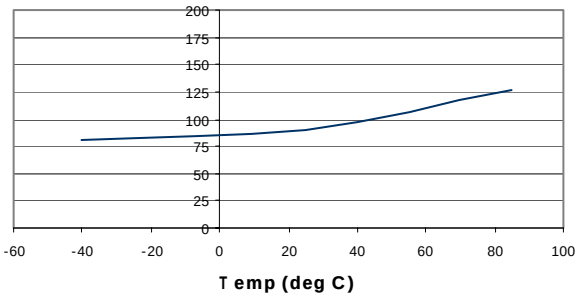
SSCLK Attenduation vs. VDD over Temperature
(Measured at 7th Harmonic with Fnom=100MHz and Spread=5.0%, C_{LOAD}=15pF)



SSCLK Attenuation vs. Spread%
(Temp=25C, VDD=3.3V, SSCLK=100MHz, Measured on Cypress Characterization board with CLOAD=15pF)



Max Cycle-Cycle Jitter on SSCLK vs. Temperature
(SSCLK=100MHz, VDD=3.3V, CLOAD=15pF)



Custom Configuration Request Procedure

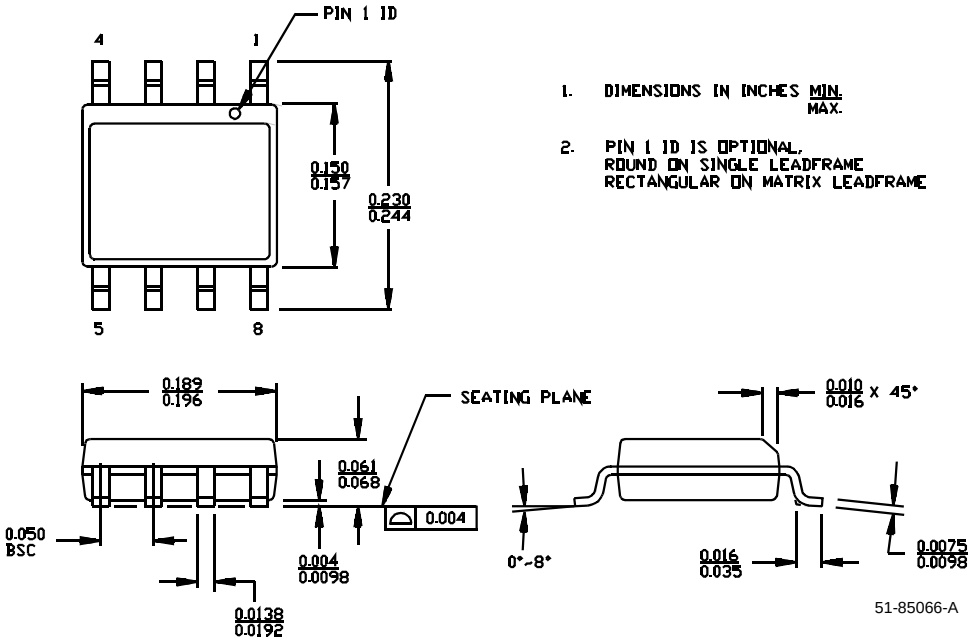
The CY25000 is a memory programmable device that is configured in the factory. All requests must be submitted to the local Cypress Field Application Engineer (FAE) or sales representative. A sample request form (refer to “CY25000 Sample Request Form” at www.cypress.com) must be completed. Once the request has been processed, you will receive a new part number, samples and data sheet with the programmed values. This part number will be used for additional sample requests and production orders.

Ordering Information

Part Number[6]	Package Type	Product Flow
CY25XXXSC-W	8-pin Small Outline Integrated Circuit (SOIC)	Commercial, 0 to 70°C
CY25XXXSC-WT	8-pin Small Outline Integrated Circuit (SOIC)–Tape and Reel	Commercial, 0 to 70°C

Package Drawing and Dimensions

8-lead (150-mil) SOIC S8



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Note:

6. “XXX” denotes the assigned product number. “W” denotes the different programmed spread % values. The user can request different spread % values.

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Document Title: CY25000 Programmable Spread Spectrum Clock Generator for EMI Reduction Document Number: 38-07424				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	115076	06/20/02	CKN	New Data Sheet
*A	121901	12/14/02	RBI	Power up requirements added to Operating Conditions Information