Frequency Multiplying, Peak Reducing EMI Solution

Features

- **Cypress PREMIS™ family offering**
- **Generates an EMI optimized clocking signal at the output**
- **Selectable frequency range and multiplication factor**
- **Single 1.25% or 5% center spread output**
- **Integrated loop filter components**
- **Operates with a 3.3V or 5V supply**
- **Low power CMOS design**
- **Available in 16-pin SOIC**

Key Specifications

Supply Voltages: ..... V_{DD} = 3.3V ±0.3V or V_{DD} = 5V ±10%

Frequency Range: ..... 15 MHz ≤ F_{out} ≤ 120 MHz

Cycle to Cycle Jitter: ..... 150 ps (typ.)

Output Duty Cycle: ..... 40/60% (worst case)

Output Rise and Fall Time ..... 5 ns (max.)

Table 1. Output Frequency Range Selection

OR2	OR1	Output Range (Multiplication Factor Selection)
0	0	reserved
0	1	15 MHz ≤ F_{IN} ≤ 30 MHz
1	0	30 MHz ≤ F_{IN} ≤ 60 MHz
1	1	60 MHz ≤ F_{IN} ≤ 120 MHz

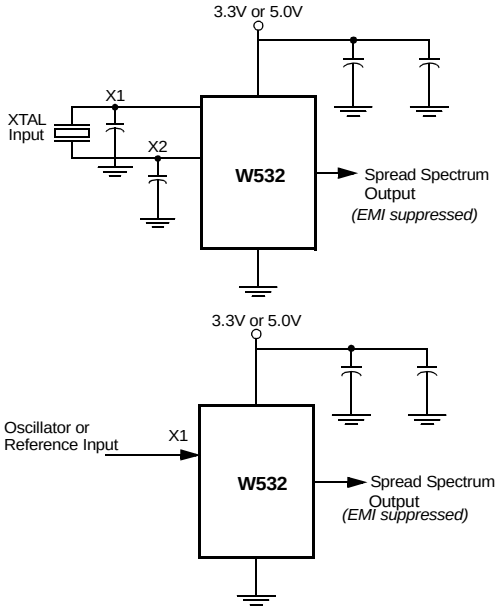
Table 2. Modulation Width Selection

MW	Output
0	$F_{avg} + 0.625\% \geq F_{out} \geq F_{avg} - 0.625\%$
1	$F_{avg} + 2.5\% \geq F_{out} \geq F_{avg} - 2.5\%$

Table 3. Input Frequency Range Selection

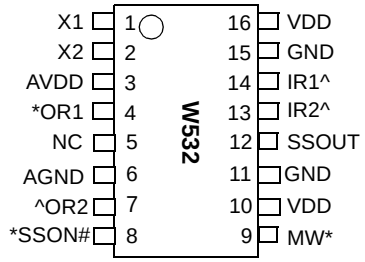
IR2	IR1	Input Range
0	0	reserved
0	1	15 MHz ≤ F_{IN} ≤ 30 MHz
1	0	30 MHz ≤ F_{IN} ≤ 60 MHz
1	1	60 MHz ≤ F_{IN} ≤ 120 MHz

Simplified Block Diagram



Pin Configuration

SOIC



Notes:
1. ^ pins have internal pull-up
2. * pins have internal pull-down

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Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
SSOUT	12	O	***Output Modulated Frequency***: Frequency modulated signal. Frequency of the output is selected as shown in *Table 1*.
CLKIN or X1	1	I	***Crystal Connection or External Reference Frequency Input:*** This pin has dual functions. It may either be connected to an external crystal, or to an external reference clock.
NC or X2	2	I	***Crystal Connection:*** Input connection for an external crystal. If using an external reference signal, this pin must be left unconnected.
SSON#	8	I	***Spread Spectrum Control (Active LOW):*** Asserting this signal (active LOW) turns the internal modulation waveform on. This pin has an internal pull-down resistor.
MW	9	I	***Modulation Width Selection:*** When Spread Spectrum feature is turned on, these pins are used to select the amount of variation and peak EMI reduction that is desired on the output signal (see *Table 2*).
IR1:2	14, 13	I	***Reference Frequency Selector:*** Logic level provided at this input indicates to the internal logic what range the reference frequency is in and determines the factor by which the device multiplies the input frequency. Refer to *Table 3*. These pins have internal pull-up resistors.
OR1:2	4, 7	I	***Output Frequency Selection Bits:*** These pins select the frequency of operation for the output. Refer to *Table 1*. OR1: DOWN - OR2: UP.
VDD	3, 10, 16	P	***Power Connection:*** Connected to 3.3V or 5V power supply.
GND	6, 11, 15	G	***Ground Connection:*** Connect all ground pins to the common ground plane.
NC	5	NC	***No Connect:*** Leave this pin floating.

Overview

The W532 product is one of a series of devices in the Cypress PREMIS family. The PREMIS family incorporates the latest advances in PLL spread spectrum frequency synthesizer techniques. By frequency modulating the output with a low frequency carrier, peak EMI is greatly reduced. Use of this technology allows systems to pass increasingly difficult EMI testing without resorting to costly shielding or redesign.

In a system, not only is EMI reduced in the various clock lines, but also in all signals which are synchronized to the clock. Therefore, the benefits of using this technology increase with the number of address and data lines in the system. The Simplified Block Diagram on page 1 shows a simple implementation.

Functional Description

The W532 uses a phase-locked loop (PLL) to frequency modulate an input clock. The result is an output clock whose frequency is slowly swept over a narrow band near the input signal. The basic circuit topology is shown in *Figure 1*. The input reference signal is divided by Q and fed to the phase detector. A signal from the VCO is divided by P and fed back to the phase detector also. The PLL will force the frequency of the VCO output signal to change until the divided output signal and the divided reference signal match at the phase detector input. The output frequency is then equal to the ratio of P/Q times the reference frequency. The unique feature of the Spread Spectrum Frequency Timing Generator is that a modulating waveform is superimposed at the input to the VCO. This causes the VCO output to be slowly swept across a predetermined frequency band.

Because the modulating frequency is typically 1000 times slower than the fundamental clock, the spread spectrum process has little impact on system performance.

Frequency Selection With SSFTG

In Spread Spectrum Frequency Timing Generation, EMI reduction depends on the shape, modulation percentage, and frequency of the modulating waveform. While the shape and frequency of the modulating waveform are fixed for a given frequency, the modulation percentage may be varied.

Using frequency select bits (IR1:2, OR1:2 pins), the frequency range can be set (see *Table 1* and *Table 3*). Spreading percentage is set with pin MW as shown in *Table 2*.

A larger spreading percentage improves EMI reduction. However, large spread percentages may either exceed system maximum frequency ratings or lower the average frequency to a point where performance is affected. For these reasons, spreading percentages between 0.5% and 2.5% are most common.

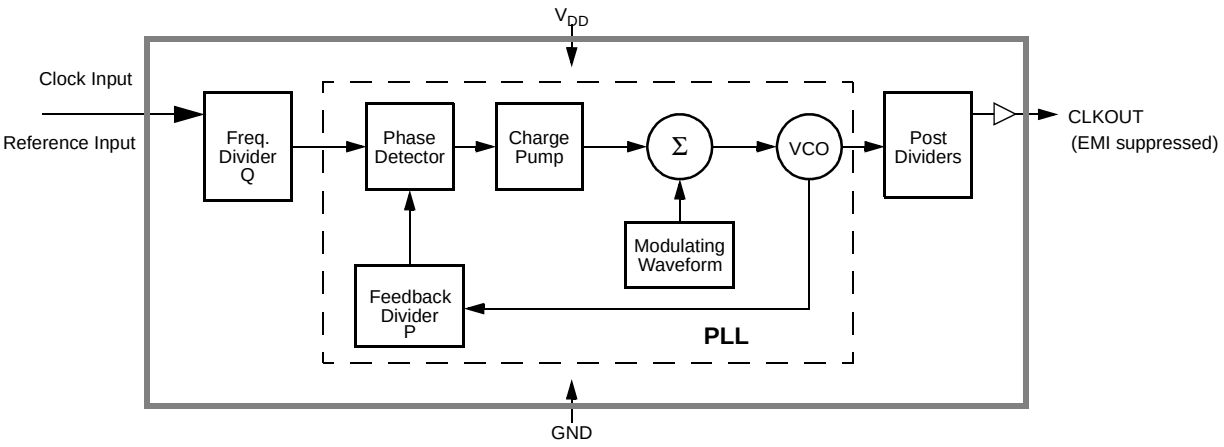


Figure 1. Conceptual Block Diagram

Spread Spectrum Frequency Timing Generation

The benefits of using Spread Spectrum Frequency Timing Generation are depicted in *Figure 2*. An EMI emission profile of a clock harmonic is shown.

Contrast the typical clock EMI with the Cypress Spread Spectrum Frequency Timing Generation EMI. Notice the spike in the typical clock. This spike can make systems fail quasi-peak EMI testing. The FCC and other regulatory agencies test for peak emissions. With spread spectrum enabled, the peak energy is much lower (at least 8 dB) because the energy is spread out across a wider bandwidth.

Modulating Waveform

The shape of the modulating waveform is critical to EMI reduction. The modulation scheme used to accomplish the maximum reduction in EMI is shown in *Figure 3*. The period of the modulation is shown as a percentage of the period length along the X axis. The amount that the frequency is varied is shown along the Y axis, also shown as a percentage of the total frequency spread.

Cypress frequency selection tables express the modulation percentage in two ways. The first method displays the spreading frequency band as a percent of the programmed average output frequency, symmetric about the programmed average frequency. This method is always shown using the expression $f_{Center} \pm X_{MOD}\%$ in the frequency spread selection table.

The second approach is to specify the maximum operating frequency and the spreading band as a percentage of this frequency. The output signal is swept from the lower edge of the band to the maximum frequency. The expression for this approach is $f_{MAX} - X_{MOD}\%$. Whenever this expression is used, Cypress has taken care to ensure that f_{MAX} will never be exceeded. This is important in applications where the clock drives components with tight maximum clock speed specifications.

SSON# Pin

An internal pull-down resistor defaults the chip into spread spectrum mode. When the SSON# pin is asserted (active LOW) the spreading feature is enabled. Spreading feature is disabled when SSON# is set HIGH (V_{DD}).

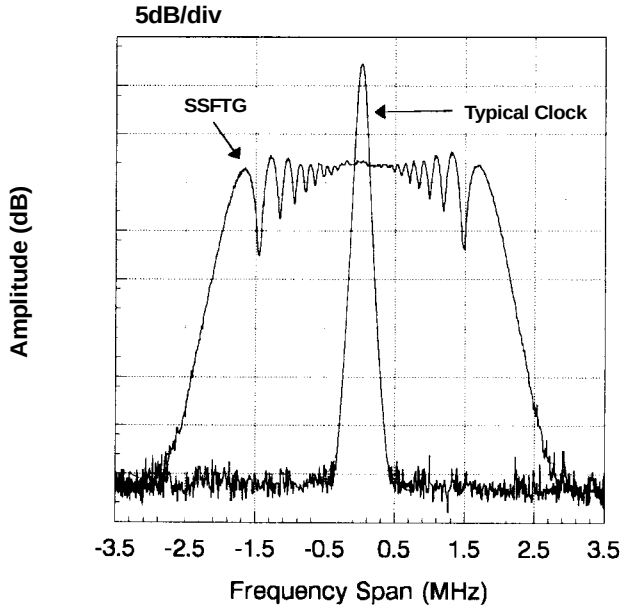


Figure 2. Typical Clock and SSFTG Comparison

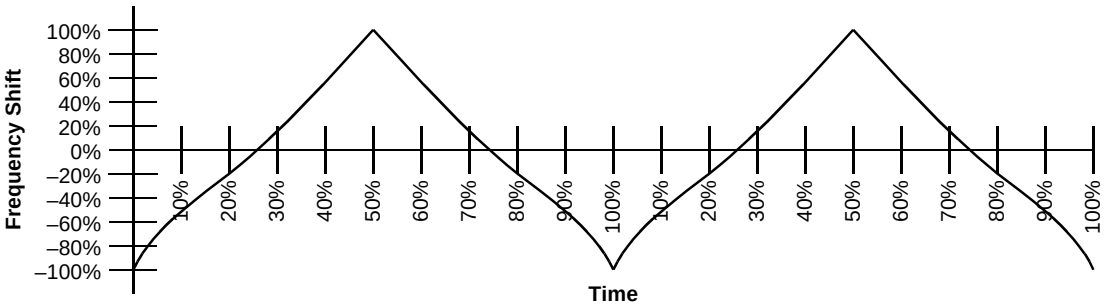


Figure 3. Modulation Waveform Profile

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any Pin with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +70 or –40 to +85	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
P_D	Power Dissipation	0.5	W

DC Electrical Characteristics: 0°C < T_A < 70°C or –40°C to +85°C, V_{DD} = 3.3V ±0.3V

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current			18	32	mA
t_{ON}	Power-Up Time	First locked clock cycle after Power Good			5	ms
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.4			V
V_{OL}	Output Low Voltage				0.4	V
V_{OH}	Output High Voltage		2.4			V
I_{IL}	Input Low Current	Note 3	–50			µA
I_{IH}	Input High Current	Note 3			50	µA
I_{OL}	Output Low Current	@ 0.4V, V_{DD} = 3.3V		15		mA
I_{OH}	Output High Current	@ 2.4V, V_{DD} = 3.3V		15		mA
C_I	Input Capacitance				7	pF
R_P	Input Pull-Up Resistor			150		kΩ
Z_{OUT}	Clock Output Impedance			25		Ω

Note:
3. Inputs OR2 and IR1:2 have a pull-up resistor, Inputs SSON# OR1 and MW have a pull-down resistor.

DC Electrical Characteristics: $0°C < T_A < 70°C$ or –40°C to +85°C, V_{DD} = 5V ±10%

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current			30	50	mA
t_{ON}	Power-Up Time	First locked clock cycle after Power Good			5	ms
V_{IL}	Input Low Voltage				$0.15V_{DD}$	V
V_{IH}	Input High Voltage		$0.7V_{DD}$			V
V_{OL}	Output Low Voltage				0.4	V
V_{OH}	Output High Voltage		2.4			V
I_{IL}	Input Low Current	Note 3	–50			µA
I_{IH}	Input High Current	Note 3			50	µA
I_{OL}	Output Low Current	@ 0.4V, V_{DD} = 5V		24		mA
I_{OH}	Output High Current	@ 2.4V, V_{DD} = 5V		24		mA
C_I	Input Capacitance				7	pF
R_P	Input Pull-Up Resistor			150		kΩ
Z_{OUT}	Clock Output Impedance			25		Ω

AC Electrical Characteristics: T_A = 0°C to +70°C or –40°C to +85°C, V_{DD} = 3.3V ±0.3V or 5V±10%

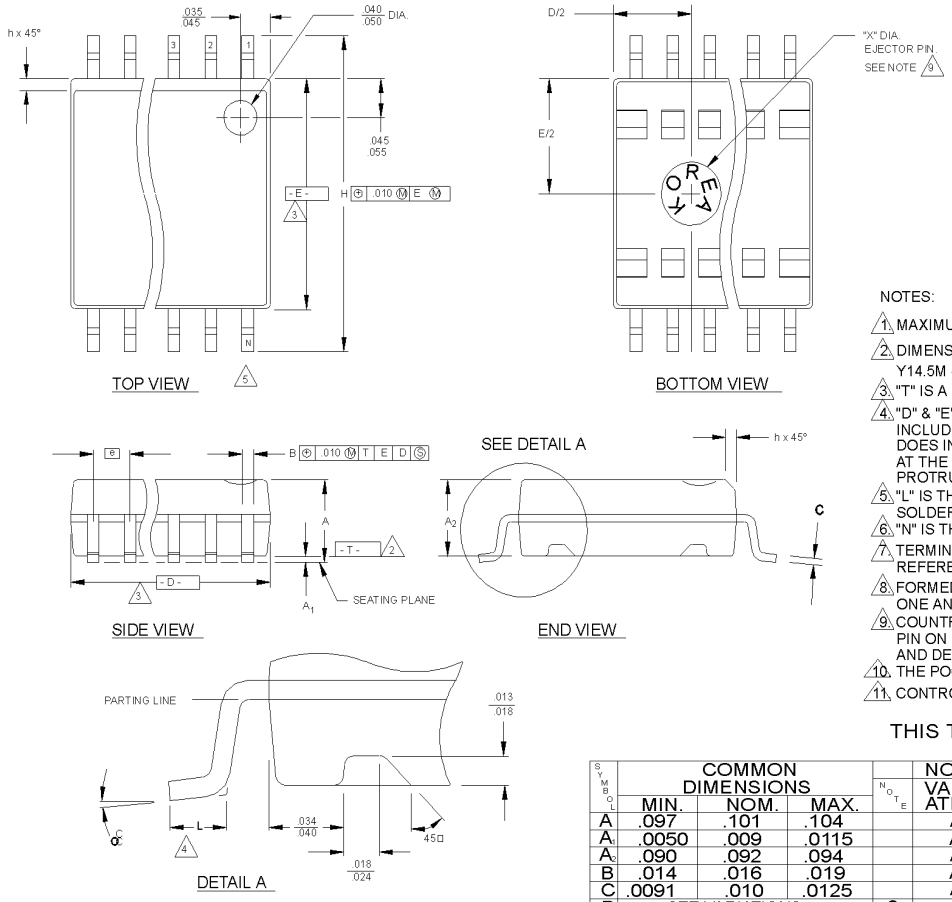
Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
f_{IN}	Input Frequency	Input Clock	14		120	MHz
f_{OUT}	Output Frequency	Spread Off	13		120	MHz
t_R	Output Rise Time	V_{DD}, 15-pF load, 0.8–2.4V		2	5	ns
t_F	Output Fall Time	V_{DD}, 15-pF load, 2.4–0.8V		2	5	ns
t_{OD}	Output Duty Cycle	15-pF load	40		60	%
t_{ID}	Input Duty Cycle		40		60	%
t_{JCYC}	Jitter, Cycle-to-Cycle			150	300	ps

Ordering Information

Ordering Code	Package Name	Package Type	Temperature Range
W532	G	16-Pin Plastic SOIC (300-mil)	Commercial (0° – 70°)
W532	GI	16-Pin Plastic SOIC (300-mil)	Industrial (–40° – 85°)

Package Diagram

16-Pin Small Outline Integrated Circuit (SOIC, 300-mil)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
2. DIMENSIONING & TOLERANCES PER ANSI. Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPEND ON ASSEMBLY LOCATION.
10. THE POCKETS ON THE BOTTOM ARE OPTIONAL.
11. CONTROLLING DIMENSION: INCHES.

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARIATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	.097	.101	.104		AA	.402	.407	.412	16
A_1	.0050	.009	.0115		AB	.451	.456	.461	18
A_2	.090	.092	.094		AC	.500	.505	.510	20
B	.014	.016	.019		AD	.602	.607	.612	24
C	.0091	.010	.0125		AE	.701	.706	.711	28
D	SEE VARIATIONS			3					
E	.292	.296	.299						
e	.050 BSC								
H	.400	.406	.410						
h	.010	.013	.016						
L	.024	.032	.040						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	.085	.093	.100						

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARIATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	2.46	2.56	2.64		AA	10.21	10.34	10.46	16
A_1	0.127	0.22	0.29		AB	11.46	11.58	11.71	18
A_2	2.29	2.34	2.39		AC	12.70	12.83	12.95	20
B	0.35	0.41	0.48		AD	15.29	15.42	15.54	24
C	0.23	0.25	0.32		AE	17.81	17.93	18.06	28
D	SEE VARIATIONS			3					
E	7.42	7.52	7.59						
e	1.27 BSC								
H	10.16	10.31	10.41						
h	0.25	0.33	0.41						
L	0.61	0.81	1.02						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	2.16	2.36	2.54						

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