

## GENERAL DESCRIPTION

EM19101 is a 8-bit CMOS A/D converter for scanner use. The adoption of a 2-step parallel system achieves low consumption at a maximum conversion speed of 7 MSPS.

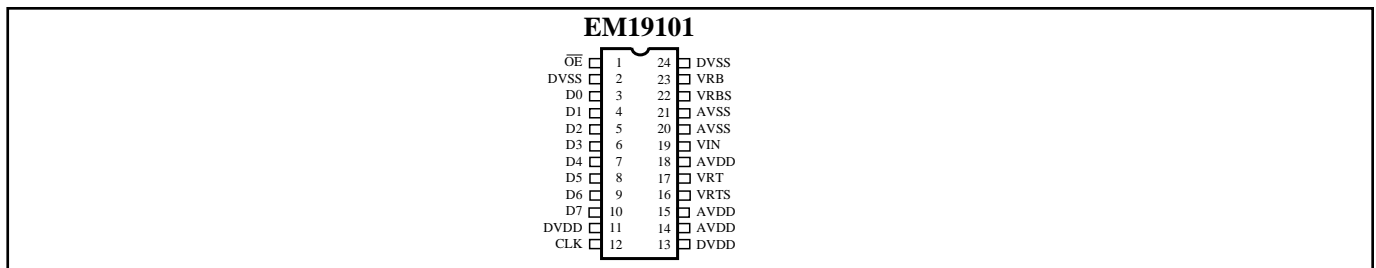
## FEATURES

- 7MSPS maximum conversion speed
- Build-in sampling and hold circuit
- Internal self-bias reference voltage
- 45 mW very low power dissipation at 5MSPS
- +5V single power supply
- Available in 24 pin SOP
- Series
  - EM19101M for 300 mil SOP
  - EM19101S for 209 mil SOP

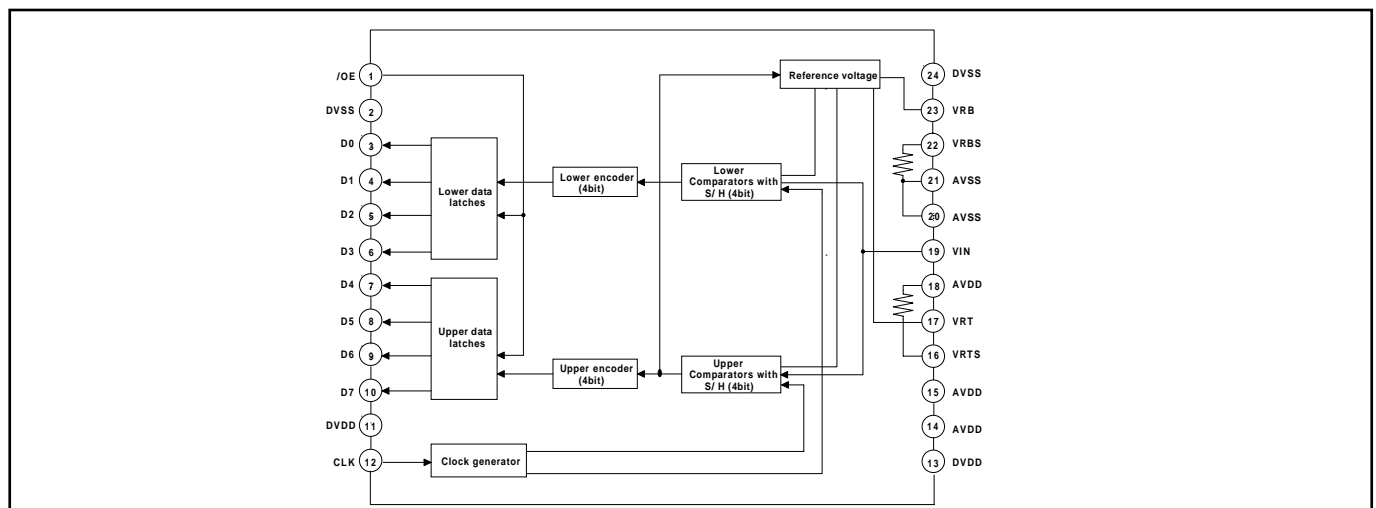
## APPLICATION

Scanner and a wide range of fields where high speed A/D conversion is required in the digital communication.

## PIN ASSIGNMENT



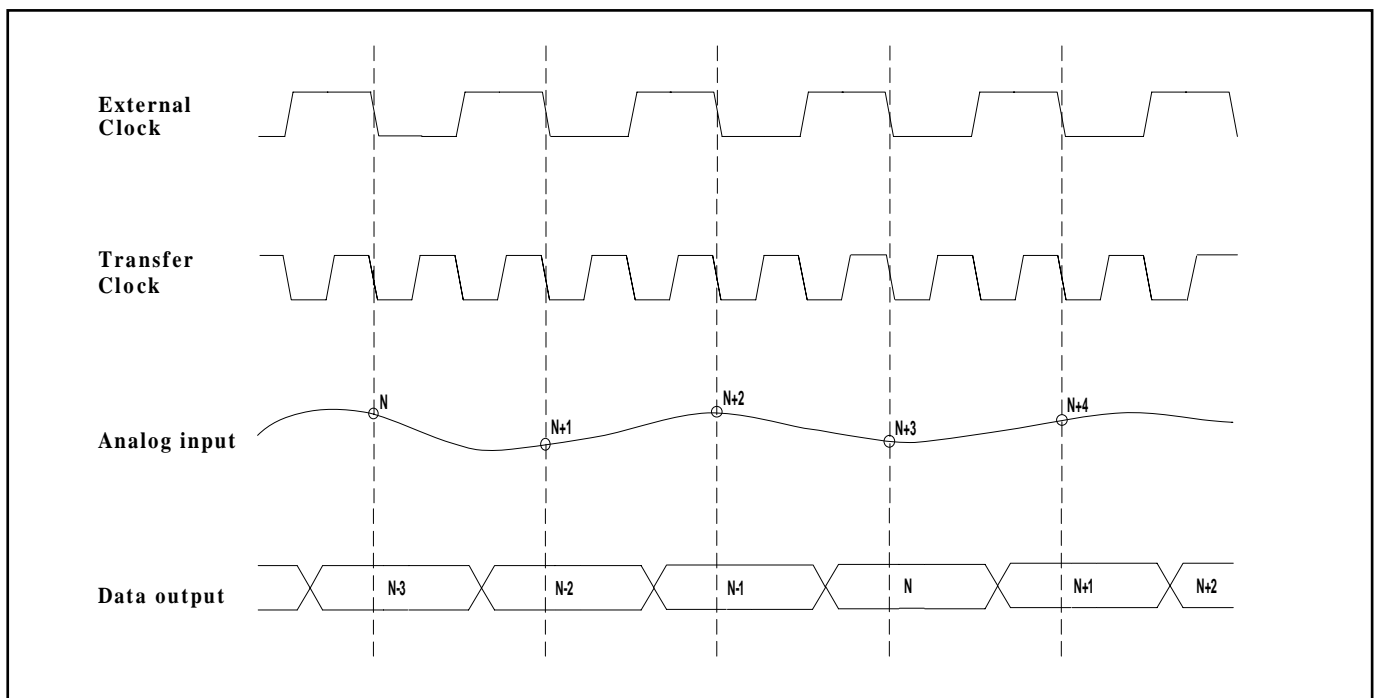
## FUNCTIONAL BLOCK DIAGRAM



### PIN DESCRIPTIONS

| Symbol          | Function                          |
|-----------------|-----------------------------------|
| $\overline{OE}$ | Output enable                     |
| DVSS            | Digital ground                    |
| D0              | Data output bit 0 (LSB)           |
| D1              | Data output bit 1                 |
| D2              | Data output bit 2                 |
| D3              | Data output bit 3                 |
| D4              | Data output bit 4                 |
| D5              | Data output bit 5                 |
| D6              | Data output bit 6                 |
| D7              | Data output bit 7 (MSB)           |
| DVDD            | Digital power supply              |
| CLK             | Clock input                       |
| DVDD            | Digital power supply              |
| AVDD            | Analog power supply               |
| AVDD            | Analog power supply               |
| VRTS            | Top internal reference voltage    |
| VRT             | Top reference voltage             |
| AVDD            | Analog power supply               |
| VIN             | Analog input voltage              |
| AVSS            | Analog ground                     |
| AVSS            | Analog ground                     |
| VRBS            | Bottom internal reference voltage |
| VRB             | Bottom reference voltage          |
| DVSS            | Digital ground                    |

### TIMING DIAGRAM



\* This specification are subject to be changed without notice.



### OUTPUT CODING

| Step | Analog Input (V)    | Digital Output Code | Conditions    |
|------|---------------------|---------------------|---------------|
| 0    | 0.607815            | 00000000            | VRB=0.6V      |
| 1    | 0.607815~0.6156250  | 00000001            | VRT=2.6V      |
| 2    | 0.6156250~0.6234375 | 00000010            | 1LSB=7.8125mV |
| .... | ....                | ....                |               |
| 124  | 1.6000000~1.6078125 | 10000000            |               |
| 125  | 1.6078125~1.6156250 | 10000001            |               |
| .... | ....                | ....                |               |
| 254  | 2.5843750~2.5921875 | 11111110            |               |
| 255  | 2.5921875~          | 11111111            |               |

### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub>=25°C)

| Items                 | Sym.                              | Rating                             | Unit |
|-----------------------|-----------------------------------|------------------------------------|------|
| Supply voltage        | V <sub>DD</sub>                   | 7                                  | V    |
| Operating temperature | T <sub>OPR</sub>                  | -20 to +65                         | °C   |
| Input voltage         | V <sub>IN</sub>                   | V <sub>SS</sub> to V <sub>DD</sub> | V    |
| Ref, Input voltage    | V <sub>RT</sub> , V <sub>RB</sub> | V <sub>SS</sub> to V <sub>DD</sub> | V    |

### Recommended Poerating Conditions

| Items                   | Sym.                                | Rating                             | Unit |
|-------------------------|-------------------------------------|------------------------------------|------|
| Supply voltage          | AV <sub>DD</sub> , AV <sub>SS</sub> | 4.75 TO 5.25                       | V    |
|                         | DV <sub>DD</sub> , DV <sub>SS</sub> |                                    |      |
|                         | DGND-AGND                           | 0 to 100                           | mV   |
| Reference input voltage | V <sub>RB</sub>                     | 0 and above                        | V    |
|                         | V <sub>RT</sub>                     | V <sub>DD</sub> and below          | V    |
|                         | V <sub>RT</sub> - V <sub>RB</sub>   | 1.0 to 3.0                         | V    |
| Analog input voltage    | V <sub>IN</sub>                     | V <sub>RB</sub> to V <sub>RT</sub> | V    |

(F<sub>C</sub>=5MPS, V<sub>DD</sub>=5V, V<sub>RB</sub>=0.5V, V<sub>RT</sub>=2.5V, T<sub>A</sub>=25°C External clock duty=40 to 60%)

| Parameter                | Sym.                             | Conditions                                 | Min. | Typ. | Max. | Unit |
|--------------------------|----------------------------------|--|------|------|------|------|
| Maximum Conversion Speed | F <sub>C</sub>                   | Vin=0.6V to 2.6V fin=1kHz ramp             |      | 5    |      | MSPS |
| Supply current           | I <sub>DD</sub>                  | F <sub>C</sub> =5MSPS NTSC ramp wave input |      | 10   | 15   | mA   |
| Reference pin current    | I <sub>REF</sub>                 |  | 5.7  | 8.0  | 9.1  | mA   |
| Analog input bandwidth   | BW                               |  |      | 1    |      | MHz  |
| Analog input capacitance | C <sub>IN</sub>                  | V <sub>IN</sub> =1.5V+0.07Vrms             |      | 11   |      | pF   |
| Reference resistance     | R <sub>REF</sub>                 |  | 220  | 250  | 350  | Ω    |
| Internal bias            | V <sub>RB</sub>                  | Short V <sub>RB</sub> and V <sub>RBS</sub> | 0.55 | 0.6  | 0.65 | V    |
|                          | V <sub>RT</sub> -V <sub>RB</sub> | Short V <sub>RT</sub> and V <sub>RTS</sub> | 1.9  | 2.0  | 2.1  |      |
| Offset Voltage           | E <sub>OT</sub>                  |  | -10  | -35  | -60  | mV   |
|                          | E <sub>OB</sub>                  |  | 0    | 15   | 45   |      |
| Digital input voltage    | V <sub>IH</sub>                  |  | 4.0  |      |      | V    |
|                          | V <sub>IL</sub>                  |  |      |      | 1.0  |      |
| Digital input current    | I <sub>IH</sub>                  | V <sub>DD</sub> =max.                      |      |      | 5    | uA   |
|                          | I <sub>IL</sub>                  |  |      |      | 5    |      |

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| Parameter                 | Sym.      | Conditions                                       |                      | Min. | Typ.      | Max.      | Unit        |
|---------------------------|-----------|--|----------------------|------|-----------|-----------|-------------|
| Digital output current    | $I_{OH}$  | $OE=V_{SS}$                                      | $V_{OH}=V_{DD}-0.5V$ | -1.1 |           |           | mA          |
|                           | $I_{OL}$  | $V_{DD}=\text{min.}$                             | $V_{OL}=0.4V$        | 3.7  |           |           |             |
| Digital output current    | $I_{OZH}$ | $OE=V_{DD}$                                      | $V_{OH}=V_{DD}$      |      |           | 16        | uA          |
|                           |           |  | $V_{OL}=0V$          |      |           | 16        |             |
| Output data delay         | $T_{DL}$  |  |                      |      | 25        | 40        | ns          |
| Integral nonlinearity     | EL        | $F_C=5\text{MSPS } V_{IN}=0.6V \text{ to } 2.6V$ |                      |      | 0.5       | 1.3       | LSB         |
| Differential nonlinearity | ED        | $F_C=5\text{MSPS } V_{IN}=0.6V \text{ to } 2.6V$ |                      |      | $\pm 0.3$ | $\pm 0.5$ | LSB         |
| Differential gain error   | DG        | NTSC 40 IRE mod ramp,<br>$F_C=14.3\text{MSPS}$   |                      |      | 1.0       |           | %           |
| Differential phase error  | $D_p$     |  |                      |      | 0.5       |           | $^{\circ}C$ |
| Aperture jitter           | $t_{AJ}$  |  |                      |      | 30        |           | ps          |
| Sampling delay            | $t_{DS}$  |  |                      |      | 4         |           | ns          |

### Application Note

$V_{DD}, V_{SS}$

To reduce noise effects, separate the analog and digital systems close to the device. For both the digital and analog  $V_{DD}$  pins, use a ceramic capacitor of about 0.1uF set as close as possible to the pin to bypass to the respective GND's.

#### Analog input

Compared with the flash type A/D converter, the input capacitance of the analog input is rather small. However it is necessary to conduct the drive with an amplifier featuring sufficient band and drive capability. When driving with an amplifier of low output impedance, parasite oscillation may occur. That may be prevented by inserting a resistance of about 100Ω in series between the amplifier output and A/D input.

#### Clock input

The clock line wiring should be as short as possible also, to avoid any interference with other signals, separate it from other circuits

#### Reference input

Voltage between  $V_{RT}$  to  $V_{RB}$  is compatible with the dynamic range of the analog input. Bypassing  $V_{RT}$  and  $V_{RB}$  pins to GND, by means of a capacitor about 0.1uF, stable characteristics are obtained. By shorting  $V_{RT}$  and  $V_{RTS}$ ,  $V_{RB}$  and VRBS, the self bias function that generates  $V_{RT}=2.6V$  and  $V_{RB}=0.6V$ , is activated.

#### Timing

Analog input is sampled with the falling edge of external clock and output as digital data with a delay of 2.5 clocks and with the following rising edge. The delay from the clock rising edge to the data output is about 25ns.

#### $\overline{OE}$ pin

By connecting  $\overline{OE}$  to GND output mode is obtained. By connecting to  $V_{DD}$  high impedance is obtained.

#### About latch up

It is necessary that  $AV_{DD}$  and  $DV_{DD}$  pins be the common source of power supply. This is to avoid latch up due to the voltage difference between  $AV_{DD}$  and  $DV_{DD}$  pins when power is ON.

