PATHFINDER-1

High Performance Vector Processing Chip

Applications:

- Radar/Sonar Signal Processing
- Signal Intelligence/Real Time Spectral Analysis
- Telecommunications
- Medical Electronics
- High Performance Instrumentation

Pathfinder-1 Benefits & Features

- 80 MHz Clock (Commercial Temperature Range 0°C to 70°C)
- 3.3V Operation
- Synchronous System Design
- 0.35 micron CMOS Three Layer Metal Process
- 24-and 32-Bit 2's Complement Block Floating Point (8-bit Exponent) Provides 192 dB Dynamic Range
- Distributed Internal Scaling Minimizes Round Off Errors
- Five Port Device
- Full Crossbar Multiplexing on all Ports
- Free Window or Filter Multiplications with the First Pass or an FFT of IFFT for All Radix Sizes
- Designed in VHDL
- Supported Opcodes Include
  - Radix 2, 4, 16, 32 for Real and Complex Data
  - Complex and Real Multiply
  - Add, Subtract
  - Single Channel Real FFTs
  - Dual Channel Real FFTs
  - Single Channel Real IFFTs
  - Dual Channel Real IFFTs
  - Magnitude Squared
- 500 Pin SBGA Package
- Compatible with CRI's Sojourner Address Generator

Pathfinder-1 Benefits & Features

Pathfinder-1 is a high-performance digital signal processor optimized for computing general-purpose frequency-domain functions such as FFTs, IFFTs, real and complex multiplies, correlations, fast convolutions, and polyphase filters.

Its high precision and handling of internal scaling enables Pathfinder-1 to process large vector sizes (up to 1 million complex samples) with dynamic range unmatched by any other commercially- available FFT processing integrated circuit.

Pathfinder-1 provides a multi-port data flow structure designed to support concurrent I/O and processing, making the chip an excellent match for applications requiring very fast data throughput rates. Multiple Pathfinder-1 DSPs can be pipelined or cascaded for increased performance.

The synchronous features of Pathfinder-1 combined with its five port I/O architecture allows straight forward system design. Performing a 1K complex FFT in 25.6 microseconds (80 MHz clock) makes Pathfinder-1 the fastest 32-bit, commercially-available, FFT processor available today.

Architectural Overview

The Pathfinder-1 integrated circuit is built up from multiple complex multiplication stages, two radix-four cores, and one radix-two core. A unique feature of the Pathfinder-1 processing core is its distributed shift and round stages. This allows an improvement in dynamic range over more traditional block floating point architectures. Combined with its 32-bit precision, Pathfinder-1 offers the most dynamic range of any FFT processing chip currently available.

Data Flow

Pathfinder-1 provides five bidirectional I/O ports (please see the block diagram in Figure 1). The chip allows full cross-bar multiplexing on all five ports, enabling very flexible system designs and algorithm implementation. One benefit of the five port architecture is that cascaded processor designs become straight forward to implement. (Please see "Example System Architectures" for more details.)

Another benefit of the port architecture is that no port needs to be designated exclusively as a coefficient port. Twiddle factors, windows, and filters may be stored in any memory bank connected to any of the five ports, and may be accessed at any time during processing. Additionally, the results from any processing pass may be broadcast simultaneously to up to two separate ports. This feature is fine for implementing algorithms where the intermediate results of a vector operation need to be stored and used later in the process, as it cuts down on the number of processing passes required. For example, previous FFT chip architectures required that results of a process pass flow into specific memories. Additional processing passes were necessary to move an intermediate result to other memory banks so it could be used later in the process.

Since Pathfinder-1 has full cross-bar multiplexing on all five bi-directional ports, the need for extra move passes is eliminated thus increasing the performance of these types of algorithms.

Tables 1 and 2 summarize the data flow function set for Pathfinder-1

Pathfinder-1 System Architectures

DF Code Bit Positions	Read Data Path
DF(9:8)	C port select
DF(9:8)	B2 port select
DF(9:8)	B1 port select
DF(9:8)	A2 port select
DF(9:8)	A1 port select

Table 1: Pathfinder-1 Port Selection

DF Code Bit Encoding	Read Data Path
"00"	data input
"01"	twiddle input
"10"	data output
"11"	port is unused and is tri-state

Table 2: Pathfinder-1 Port Functionality

Example System Architectures

Pathfinder-1 is designed to be used with pipelined sync-burst synchronous SRAM's and external address generators (such as CRI's Sojourner chip). The resulting design is a very flexible, high-performance frequency-domain processing engine that can be applied to a variety of demanding real-time DSP applications. An example system-level block diagram for a recursive architecture is provided in Figure 2. It supports concurrent I/O and processing, and provides a high degree of programmability. Figure 3 shows an example of a cascaded design. It is designed to maximize continuous throughput for a given algorithm

Function Set

Pathfinder-1's function set is optimized for frequency domain processing applications. It is a pass-based processor where a given function opcode operates on an entire data vector. Table 3 summarizes Pathfinder-1's processing functions.

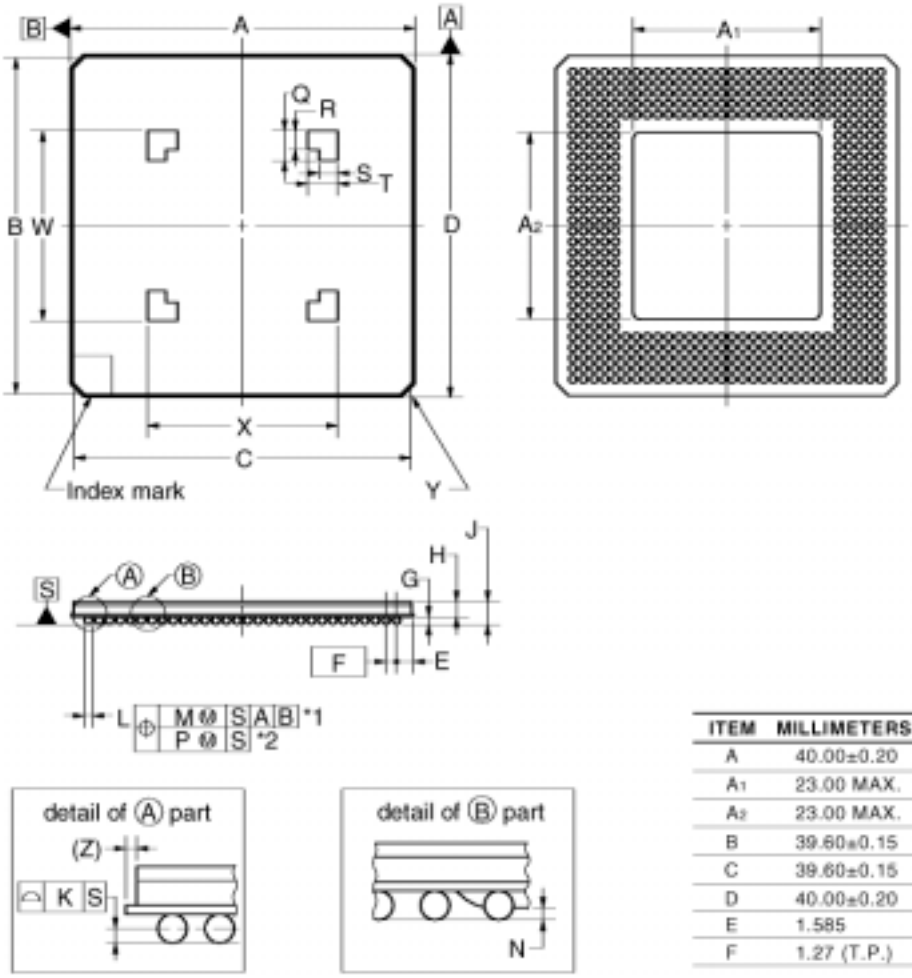
Function	Function Code (binary)	Throughput latency (clks)
RADIX 2	00000	44
RADIX 4	00001	44
RADIX 16	00010	69
RADIX 32	00011	90
DUAL_CHANNEL_ REAL	00100	42
DUAL CHANNEL REAL INVERSE	00101	42
SINGLE_ CHANNEL_REAL	00110	42
SINGLE CHANNEL REAL INVERSE	00111	42
MAGNITUDE _SQUARED	01000	41
COMPLEX _MULTIPLY	01001	41
REAL_MULTIPLY	01010	41
ADD	01011	41
SUBTRACT	01100	41
FLOW	01101	41
RADIX_2R	01110	42
RADIX_4R	01111	44
RADIX_16R	10000	69
RADIX_32R	10001	90

Pathfinder-1 Performance

Table 4 lists the performance of a single Pathfinder-1 DSP running at 80 MHz for FFT sizes from 16 points to 1 million points (complex). The small vectors (64 points and less) are implemented as stacked transforms. Multiple Pathfinder-1 chips may be cascaded to support continuous data rates of 80 million samples per second (MSPS) complex or 160 MSPS real regardless of FFT size.

Complex FFT Size	FFT Time (microseconds) 80 MHz Clock	MSPS (Complex)
16	0.2	80.0
32	0.4	80.0
64	1.6	40.0
128	3.2	40.0
256	6.4	40.0
512	12.8	40.0
1024	25.6	40.0
2048	76.8	26.7
4096	153.6	26.7
8192	307.2	26.7
16384	614.4	26.7
32768	1228.9	26.7
65536	3277.0	20.0
131072	6554.1	20.0
262144	13,108.2	20.0
524288	26,216.5	20.0
1048576	52,433.3	20.0

Pathfinder-1 Packaging Information



ITEM	MILLIMETERS	INCHES
A	40.00±0.20	1.575±0.008
A_1	23.00 MAX.	0.906 MAX.
A_2	23.00 MAX.	0.906 MAX.
B	39.60±0.15	1.559±0.006
C	39.60±0.15	1.559±0.006
D	40.00±0.20	1.575±0.008
E	1.585	0.062
F	1.27 (T.P.)	0.050 (T.P.)
G	0.60±0.10	$0.024^{+0.004}_{-0.005}$
H	$0.80^{+0.20}_{-0.10}$	$0.031^{+0.009}_{-0.004}$
J	$1.40^{+0.30}_{-0.20}$	$0.055^{+0.012}_{-0.008}$
K	0.15	0.006
L	φ0.75±0.15	$\varphi 0.030^{+0.006}_{-0.007}$
M	0.30	0.012
N	0.25 MIN.	0.009 MIN.
P	0.10	0.004
Q	3.0	0.118
R	2.0	0.079
S	2.0	0.079
T	3.0	0.118
W	22.73	0.895
X	22.73	0.895
Y	C 0.40	C 0.016
Z	0.20	0.008

S500N7-H6

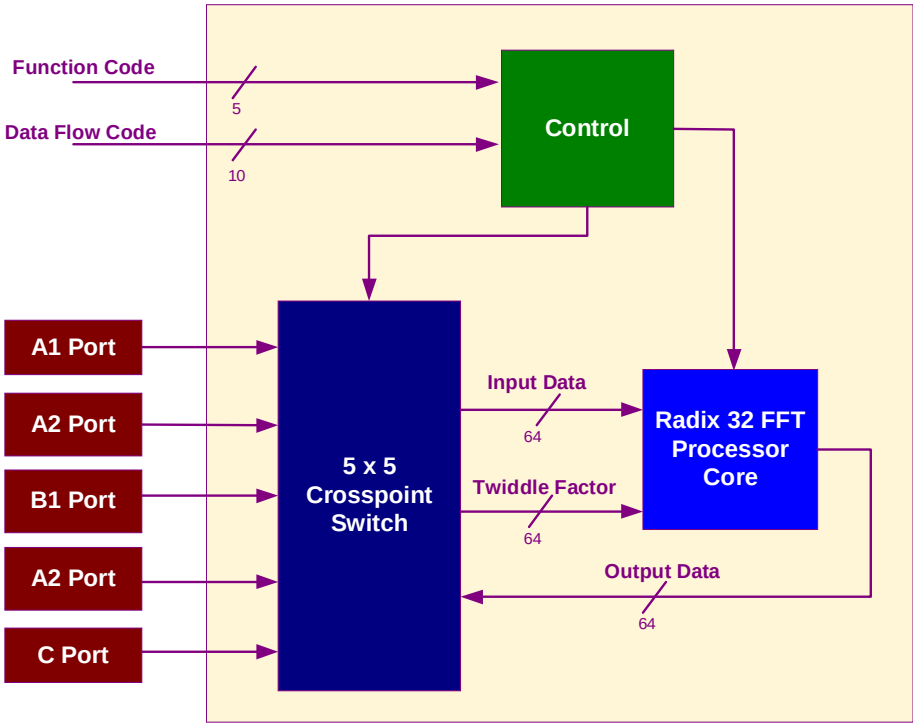
NOTES

*1 Each ball centerline is located within φ0.30 mm (φ0.012 inch) of its true position (T.P.) at maximum material condition.

*2 Each ball centerline is located within φ0.10 mm (φ0.004 inch) of its true position (T.P.) at maximum material condition.

Figure 1: 500 Pin Tape BGA (Heat Spreader Type) 40x40

Pathfinder-1 Block Diagram



About Catalina Research, Inc.

Catalina Research, Inc., based in Colorado Springs, Colorado, is a customer-driven innovative design and marketing company that provides high-bandwidth, low-latency digital signal processing (DSP) solutions for the most demanding commercial and government applications. Focusing on FFTs and digital receivers, product offerings include ASICs, boards, and systems. COTS board-level products include the highest performance FFT processors, digital receivers, reconfigurable computers, and A/D converters. Form factors and buses supported include VME, RACE, 64-bit PCI, and PMC.

Information on this product, along with CRI's entire product line, can be found on CRI's web site at www.catalinaresearch.com.

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Pathfinder-1 Block Diagram

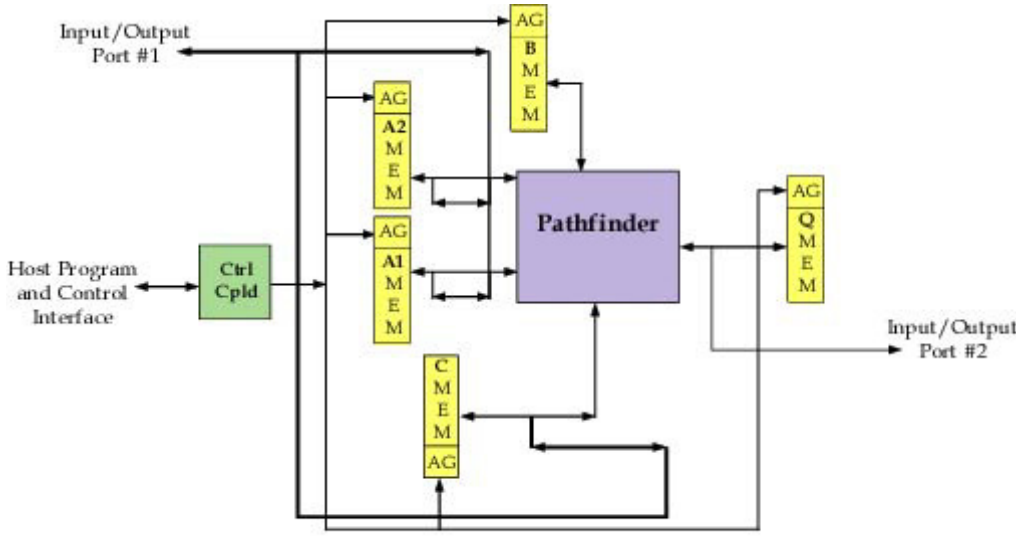
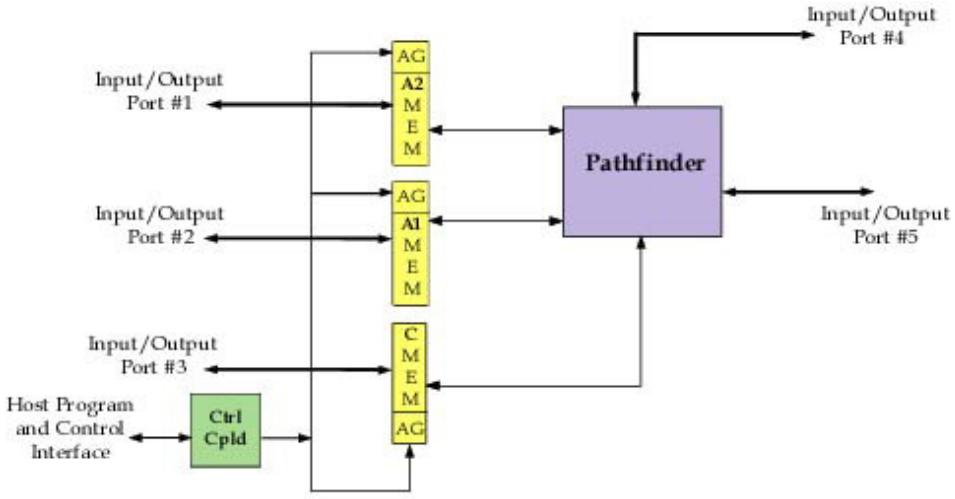


Figure 2: Recursive Architecture Example



Example:

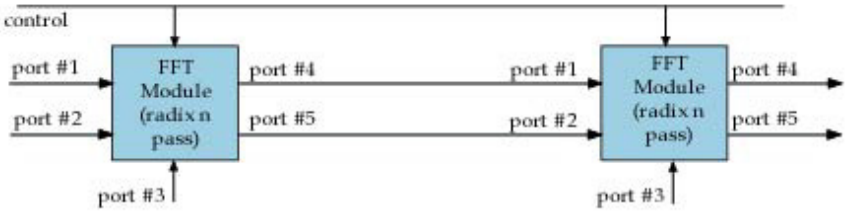


Figure 3: Cascaded Architecture Example