RHDSP24

Radiation Hardened Scalable DSP Chip
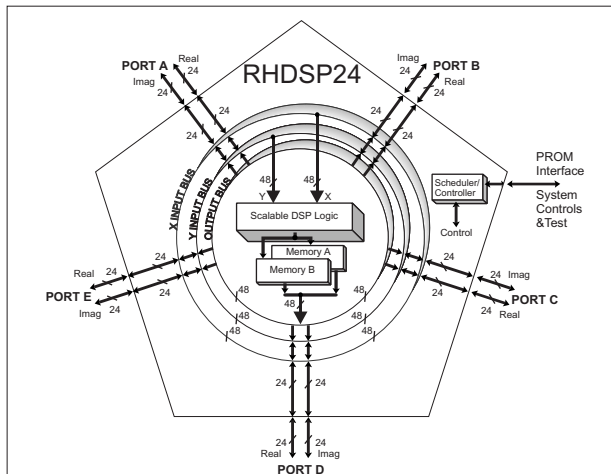
Data Sheet

FEATURES/BENEFITS:

☐ 75 MHz operation on an unlimited array size, with support for 2-D and 3-D signal/image processing.

☐ Supports DSP, Complex math, Matrix math, FIRs, Block Adds, Subtracts, Complex magnitude, etc.

☐ 75 MHz execution speed allows a complex sample rate of 37.5 MHz for a 1K complex FFT, with a window included

☐ Highly scalable architecture allows RHDSP24 chips or die to be cascaded for higher radices and extended functions

☐ Two RHDSP24's cascaded without external memory perform a Radix 1024 at a 75 MHz complex sample rate

☐ 24 bit complex FFT's with no overhead block floating point gives signal/noise greater than floating point

☐ Radix 2, Radix 4, Radix 8, Radix 16, and Radix 32 instructions, perform 1K complex FFT in two passes

☐ On chip ROM for transform coefficients and window functions, window free on all radices

☐ Five complex bi-directional data ports for highly flexible (any port to any port) data routing

☐ Macro functions buried in the chip architecture dramatically reduces software development, on chip program controller

☐ Advanced SOI CMOS, very low power 3.3 volt operation. High Performance BGA Package

☐ Enhanced real only FFT support, FFTNN and FFT2N, plus stacked FFTs to reduce latency

☐ ASIC silicon cores, Macro cells, Super cells, MCMs, and custom constructs available

☐ Commercial, High Reliability, High Temp versions available

DESCRIPTION:

The RHDSP24 breaks the computational bottlenecks associated with real time DSP, with the additional benefit of radically reduced software overhead. Most demanding DSP tasks such as frequency domain digital filtering are reduced to less than a dozen RHDSP24 machine instructions.

The RHDSP24 concentrates on performing DSP algorithms using the efficiencies of the FFT. Applications using time domain techniques such as the DFT and FIR increase in operations by an N squared function. These same applications using FFT techniques increase in operations by N x Log_2 (N), a radical reduction.

Multiple chips can be cascaded for higher radices, two cascaded chips will perform a 1024 radix, this gives a 1 million point transform in two passes at a startling 37.5 MHz complex continuous sample rate.

The RHDSP24 was designed using DSP Architectures Inc macro cells and super cells. The end customer can use the RHDSP24 as a silicon core and surround the chip with proprietary circuitry to further enhance the application and reduce his overall application hardware.

75 MHz, 24-BIT PERFORMANCE:

1024 point complex FFT........................ approx 34.7 sec

32K point complex FFT......................... approx. 1320 sec

Complex 16 x 16 Matrix Multiply .... 55 sec

Real FIR Filter .... 6.7 nsec/tap

Complex Multiply .... 13.3 nsec

Complex FIR Filter .... 13.3 nsec/tap

Figure 1. FFT Based Approach
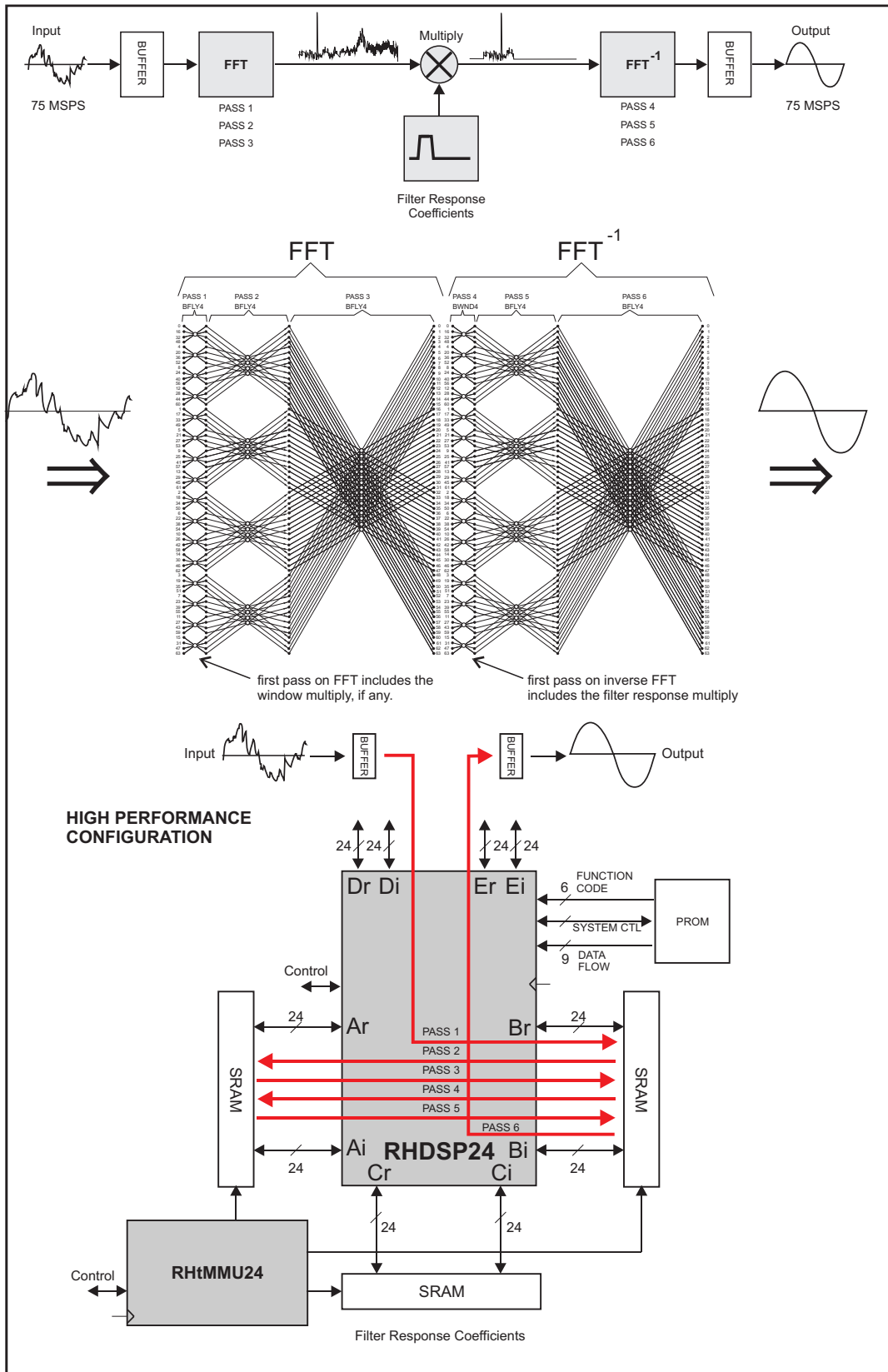
Figure 2. RHDSP24 Block Diagram

RHDSP24

RHtMMU24 CONTROL
- MMU R/$\overline{W}$
- MMU A0
- MMU START
- $\overline{MMU\ CS}$[4:0] (5)
- MMU TCA
- MMU TCB
- MMU TCC
- MMU TCD
- MMU TCE

SYSTEM AND PORT CLOCKS
- SYSCLK
- $\overline{SYSCLKEN}$
- CLKAIN
- CLKBIN
- CLKCIN
- CLKDIN
- CLKEIN

PORT CONTROL
- AOE
- BOE
- COE
- DOE
- EOE
- POUT[2:0] (3)

BI-DIRECTIONAL DATA PORTS
- AR [23:0] (24)
- AI [23:0] (24)
- BR [23:0] (24)
- BI [23:0] (24)
- CR [23:0] (24)
- CI [23:0] (24)
- DR [23:0] (24)
- DI [23:0] (24)
- ER [23:0] (24)
- EI [23:0] (24)

PROM INTERFACE
- SCHSEL
- ADDR[15:0] (16)
- $\overline{ADDREN}$
- SCH_DB[7:0] (8)
- ALG[7:0] (8)

DATA FLOW & FUNCTION CONTROL
- DF[8:0] (9)
- FC[5:0] (6)
- ENA
- ENB

SYSTEM SYNCHRONIZATION
- $\overline{GO}$[1:0] (2)
- START/$\overline{STOP}$
- SYNCOUT[1:0] (2)
- SYNCIN[1:0] (2)
- RESET
- BUSY

TEST/JTAG
- JCK
- JMS
- JDI
- JDO
- $\overline{JRST}$

BLOCK FLOATING POINT CONTROL
- BFPI[5:0] (6)
- BFPO[5:0] (6)
- DSFO[3:0] (4)
- BFPCLR

DATA CONDITIONING SWITCHES
- YSWAP
- XSWAP
- XSFISEL
- XSFI[3:0] (4)
- YSFI[3:0] (4)
- YCR
- XCR
- DOCR
- DOCI
- YCI
- XCI
- YZI
- XZI
- DZO
- PI0
- PI1

Table 1. RHDSP24 Signal-Pin Description

PIN	I/O	SIGNAL DESCRIPTION
DATA BUSES		
AR[23:0]	I/O	Port A real. Bidirectional real data port
AI[23:0]	I/O	Port A imaginary. Bidirectional imaginary data port
BR[23:0]	I/O	Port B real. Bidirectional real data port
BI[23:0]	I/O	Port B imaginary. Bidirectional imaginary data port
CR[23:0]	I/O	Port C real. Bidirectional real data port
CI[23:0]	I/O	Port C imaginary. Bidirectional imaginary data port
DR[23:0]	I/O	Port D real. Bidirectional real data port
DI[23:0]	I/O	Port D imaginary. Bidirectional imaginary data port
ER[23:0]	I/O	Port E real. Bidirectional real data port
EI[23:0]	I/O	Port E imaginary. Bidirectional imaginary data port
CONTROL		
DF[8:0]	I	Data flow control. The data flow opcode (mnemonic) indicates the direction data (read/write) flows through the chip based on the source and destination ports.
FC[5:0]	I	Function control. The function opcode (mnemonic) determines the function the chip is to perform on the data for the current pass.
START/$\overline{\text{STOP}}$	I	Start of Pass. Indicates the start and stop of a pass and qualifies the opcode. START/$\overline{\text{STOP}}$ is set high for the start of a pass and taken low at the end of the pass.
XCR	I	Complement or invert the X input real data. When set high, XCR performs a two's complement or an inversion on the real side data beginning one cycle before execution of the selected function.**
XCI	I	Complement or invert the X input imaginary data. When set high, XCI performs a two's complement or an inversion on the imaginary side data beginning one cycle before execution of the selected function.**
YCR	I	Complement or invert the Y input real data. When set high, YCR performs a two's complement or an inversion on the real side data beginning one cycle before execution of the selected function.**
YCI	I	Complement or invert the Y input imaginary data. When set high, YCI performs a two's complement or an inversion on the imaginary side data beginning one cycle before execution of the selected function.**
DOCR	I	Complement or invert the real output data. When set high, DOCR performs a two's complement or an inversion on the real side data beginning one cycle before the data reaches the output.**
DOCI	I	Complement or invert the imaginary output data. When set high, DOCI performs a two's complement or an inversion on the imaginary side data beginning one cycle before the data reaches the output.**

** Complement or invertion is based on Function Code

Table 1. (cont) RHDSP24 Signal-Pin Description

PIN	I/O	SIGNAL DESCRIPTION
CONTROL (cont.)		
XZI	I	Zero input data, both real and imaginary. When set high, XZI forces the input X data to zero.
YZI	I	Zero input data, both real and imaginary. When set high, YZI forces the input Y data to zero.
DZO	I	Zero output data, both real and imaginary. When set high, DZO forces the output data to zero.
ENA	I	Enable A. Enables FC[5:0], DF[8:0] control signals to be registered into the chip on the next SYSCLK.
ENB	I	Enable B. Enables the control signals BFPI[5:0], XSFI[3:0], XSFISEL, YSFI[3:0] to be registered into the chip on the next SYSCLK.
RESET	I	When set high, clears all internal counters sets registers to defaults
BFPI[5:0]	I	Block floating point input. Inputs the accumulated scale factor from the preceding passes of an algorithm to sum the exponent for a complete FFT.
BFPO[5:0]	O	Block floating point output. Outputs the accumulated scale factor from the preceding passes since START was asserted.
XSFI[3:0]	I	Data scaling factor for X input. Assigns the user supplied scale factor (number of right shifts) to the current input data before execution by up to sixteen (16) shifts. If the user has specified automatic scaling by asserting the DSFISEL control signal low, then the internal radix adjusted shift will be applied, instead of the user supplied scale factor.
YSFI[3:0]	I	Data scaling factor input for Y input. Assigns the user supplied scale factor (number of right shifts) to the current input data before execution by up to sixteen (16) shifts. The automatic scaling, DSFISEL control signal,does not affect the user supplied scale factor.
DSFO[3:0]	O	Data scale factor output. Assigns a worst case automatic scale factor (number of right shifts) to the RHDSP24 output data, which is to be scaled by the system when connected to the XSFI[3:0] on the next pass.
XSFISEL	I	Data scale factor input select. When set low, enables the DSFI automatic block floating point adjustment. When set high, disables the automatic scaling and permits a user defined scale input to be performed.
SCHSEL	I	Internal scheduler/controller selection. When set high the internal scheduler and the internal controllers are used. Note: Certain pins are dependent on this signal for their definition.
XSWAP	I	When active high, exchanges the X imaginary data with the X real data *
YSWAP	I	When active high, exchanges the Y imaginary data with the Y real data *
BFPCLR	I	When active high clears BFPI[5:0] on any cycle (synchronous with SYSCLK)
SYNCIN[1:0]	I	User defined arbitrary input waveform.
SYNCOUT[1:0]	O	Delayed version of SYNCIN[1:0]. Matches the pipeline delay of the data as defined by the function code FC[5:0].

* After conjugation, if conjugation is set
(Precedence is, Zero, Shift, Round/Conjugate, Swap)

Table 1. (cont) RHDSP24 Signal-Pin Description

PIN	I/O	SIGNAL DESCRIPTION
**CLOCKS, ENABLES, FLAGS, & POWER**		
CLKAIN	I	Clock input for port A. Clocks the input data memory to read from port A on the next SYSCLK rising edge. Ground this clock if not used.
CLKBIN	I	Clock input for port B. Clocks the input data memory to read from port B on the next SYSCLK rising edge. Ground this clock if not used.
CLKCIN	I	Clock input for port C. Clocks the input data memory to read from port C on the next SYSCLK rising edge. Ground this clock if not used.
CLKDIN	I	Clock input for port D. Clocks the input data memory to read from port D on the next SYSCLK rising edge. Ground this clock if not used.
CLKEIN	I	Clock input for port E. Clocks the input data memory to read from port E on the next SYSCLK rising edge. Ground this clock if not used.
SYSCLK	I	Chip system clock. Clocks the chip controls and data ports.
$\overline{\text{SYSCLKEN}}$	I	Enables internal system clock (SYSCLK).
AOE	I	A port output enable. When high allows the RHDSP24 to drive the bus.
BOE	I	B port output enable. When high allows the RHDSP24 to drive the bus.
COE	I	C port output enable. When high allows the RHDSP24 to drive the bus.
DOE	I	D port output enable. When high allows the RHDSP24 to drive the bus.
EOE	I	E port output enable. When high allows the RHDSP24 to drive the bus.
POUT[2:0]	O	Encoded port output signal, indicates which data port is outputting data
JCK	I	Input clock for JTAG serial test bus.
JMS	I	Input mode select pin for JTAG serial test bus.
JDI	I	JTAG serial bus input data
JD0	O	JTAG serial bus output data
$\overline{\text{JRST}}$	I	JTAG Reset
VDD	P	Power for the chip
VSS	P	Ground for the chip

SIGNAL-PIN DESCRIPTION

Table 1. lists the RHDSP24 signals and their respective descriptions.

Note: There are several pins that have dual functions depending on the state of the SCHSEL pin.

FUNCTION SET SUMMARY

The function set is organized into five areas: DSP, Complex Arithmetic, Logical, Vector Arithmetic, and General Purpose.

There are thirty-four (34) opcodes for the RHDSP24. The RHDSP24 is a pass based processor where each control function and dataflow instruction is valid for one complete pass as framed by the START/$\overline{STOP}$ signal. Table 2 summarizes the RHDSP24 function set.

Table 1. (cont) RHDSP24 Signal-Pin Description

PIN	I/O	SIGNAL DESCRIPTION
		SCHEDULER/CONTROLLER
SSYNC[1:0]	O	Scheduler output. Not Used..
$\overline{ADDREN}$	I	When active low, enables the RHDSP24 scheduler to drive the external PROM addresses ADDR[15:0].
BUSY	O	When active high, indicates that the internal scheduler is active.
ADDR[15:0]	O	External PROM/Scheduler Memory address lines.
ALG[7:0]	I	Offset bits that are summed with the out going ADDR[15:0] bits. Used for pointing to different routines in the external PROM.
SCH_DB[7:0]	I	Scheduler input bus, used to source control information to the RHDSP24 and to any Memory Management Units (RHtMMU24's) in the system.
GO[1:0]	I	Input signals that tell the internal scheduler to initiate the start of an algorithm.
MMU START	O	Output signal, used by the RHtMMU24's to initiate the beginning of a pass.
MMU R/$\overline{W}$	O	Output signal, used to strobe the SCH_DB[7:0] signals into the RHtMMU24's.
MMU A0	O	Ouput signal, used by the RHtMMU24's in the system to point the SCH_DB[7:0] data to the proper internal address or data register.
MMU TCA	I	Input signal from the RHtMMU24 terminal count signal associated with A port
MMU TCB	I	Input signal from the RHtMMU24 terminal count signal associated with B port
MMU TCC	I	Input signal from the RHtMMU24 terminal count signal associated with C port
MMU TCD	I	Input signal from the RHtMMU24 terminal count signal associated with D port
MMU TCE	I	Input signal from the RHtMMU24 terminal count signal associated with E port
PI[1:0]	I	User supplied signal. Used in scheduler mode to modulate an arbitrary waveform onto two of the following signals; XCR, XCI, DOCR, DOCI, XZI, YZI, or DZO*.
$\overline{MMU\ CS}$[4:0]	O	Output signals, used to select the RHtMMU24's in the system.

* Selection is accomplished in the firmware

DSP
Architectures

Table 2. Function Set Summary

OPCODE	MNE-MONIC	DESCRIPTION
COMPLEX MATH FUNCTIONS		
10	CADD	Complex Add Performs a complex binary add operation with the input data and the coefficient data.
11	CSUB	Complex Subtract Performs a complex binary add operation with the input data and the coefficient data.
0D	CMUL	Complex Multiply Performs a fractional two's complement complex multiplication operation with the input data and the coefficient data.
08	CMAC	Complex Multiply/Accumulate Performs a fractional two's complement complex multiplication and complex accumulation of the result operation with the input data and the coefficient data
0C	CMAG	Complex Magnitude Performs a fractional two's complement square of the real input data added to the fractional two's complement square of the imaginary input data.
LOGIC FUNCTIONS		
18	NAND	Performs a logical NAND of the input data with the coefficient data.
1A	NOR	Performs a logical NOR of the input data with the coefficient data.
1B	XNOR	Performs a logical XNOR of the input data with the coefficient data.
GENERAL PURPOSE FUNCTIONS		
1D	MOVC	No operation, passes the complex data from one port to another
1C	MOV	No operation, passes the complex data from one port to another
1C	MOVD	No operation, passes the complex data from one port to another
19	VPAS	No operation, passes the complex data from one port to another
VECTOR FUNCTIONS		
10	VADD	Vector Add Performs a binary addition operation with the input data and the coefficient data.
11	VSUB	Vector Subtract Performs a binary subtraction operation with the input data and the coefficient data.
12	VMUL	Vector Multiply Performs a fractional two's complement multiplication operation with the input data and the coefficient data.
0A	VMAC	Vector Multiply/Accumulate Performs a fractional two's complement multiplication and accumulation of the result operation with the input data and the coefficient data.

Table 2. Function Set Summary (cont.)

OPCODE	MNE-MONIC	DESCRIPTION
		DSP FUNCTIONS
02	BFLY2	Radix2 Butterfly Performs a radix 2 based butterfly operation on the complex input data.
01	BFLY4	Radix4 Butterfly Performs a radix 4 based butterfly operation on complex input data.
0B	BFLY8	Radix8 Butterfly Performs a radix 8 based butterfly operation on complex input data.
00	BFLY16	Radix16 Butterfly Performs a radix 16 based butterfly operation on complex input data
0F	BFLY32	Radix32 Butterfly Performs a radix 32 based butterfly operation on complex input data
26	BFLY64*	Radix64 Butterfly Performs a radix 64 based butterfly operation on complex input data
27	BFLY128*	Radix128 Butterfly Performs a radix 128 based butterfly operation on complex input data
28	BFLY256*	Radix256 Butterfly Performs a radix 256 based butterfly operation on complex input data
29	BFLY512*	Radix512 Butterfly Performs a radix 512 based butterfly operation on complex input data
2A	BFLY1024*	Radix1024 Butterfly Performs a radix 1024 based butterfly operation on complex input data
17	VWND2	Radix2 Butterfly with Window Function. Performs a radix 2 based butterfly operation on the complex input data, after multiplying the incoming data by a window function.
1F	VWND4	Radix4 Butterfly with Window Function. Performs a radix 4 based butterfly operation on complex input data, after multiplying the incoming data by a window function.
14	VWND8	Radix8 Butterfly with Window Function. Performs a radix 8 based butterfly operation on complex input data, after multiplying the incoming data by a window function.
15	VWND16	Radix16 Butterfly with Window Function. Performs a radix 16 based butterfly operation on complex input data, after multiplying the incoming data by a window function.
16	VWND32	Radix 32 Butterfly with Window Function. Performs a radix 32 based butterfly operation on complex input data, after multiplying the incoming data by a window function.
2B	VWND64*	Radix 64 Butterfly with Window Function. Performs a radix 64 based butterfly operation on complex input data, after multiplying the incoming data by a window function.
2C	VWND128*	Radix128 Butterfly with Window Function. Performs a radix 128 based butterfly operation on complex input data, after multiplying the incoming data by a window function.
2D	VWND256*	Radix256 Butterfly with Window Function. Performs a radix 256 based butterfly operation on complex input data, after multiplying the incoming data by a window function.
2E	VWND512*	Radix512 Butterfly with Window Function. Performs a radix 512 based butterfly operation on complex input data, after multiplying the incoming data by a window function.
2F	VWND1024*	Radix1024 Butterfly with Window Function. Performs a radix 1024 based butterfly operation on complex input data, after multiplying the incoming data by a window function.

* For dual chip, seamless cascading

Table 2. Function Set Summary (cont.)

OPCODE	MNEMONIC	DESCRIPTION
		DSP FUNCTIONS (cont.)
05	BWND2	Radix2 Butterfly with Window Function. Performs a radix 2 based butterfly operation on the complex input data. Also multiplies the incoming data by a *complex* window function.
04	BWND4	Radix4 Butterfly with Window Function. Performs a radix 4 based butterfly operation on complex input data. Also multiplies the incoming data by a *complex* window function.
25	BWND8	Radix8 Butterfly with Window Function. Performs a radix 8 based butterfly operation on complex input data. Also multiplies the incoming data by a *complex* window function.
24	BWND16	Radix16 Butterfly with Window Function. Performs a radix 16 based butterfly operation on complex input data Also multiplies the incoming data by a *complex* window function.
20	BWND32*	Radix 32 Butterfly with Window Function. Performs a radix 32 based butterfly operation on complex input data Also multiplies the incoming data by a *complex* window function.
21	BWND64*	Radix 64 Butterfly with Window Function. Performs a radix 64 based butterfly operation on complex input data Also multiplies the incoming data by a *complex* window function.
22	BWND128*	Radix128 Butterfly with Window Function. Performs a radix 128 based butterfly operation on complex input data Also multiplies the incoming data by a *complex* window function.
23	BWND256*	Radix256 Butterfly with Window Function. Performs a radix 256 based butterfly operation on complex input data Also multiplies the incoming data by a *complex* window function.
03	BWND512*	Radix512 Butterfly with Window Function. Performs a radix 512 based butterfly operation on complex input data Also multiplies the incoming data by a *complex* window function.
07	BRFT	Real Only FFT- Two at a Time. Performs dual FFT's if the input data was real only, i.e. performing a 256 point complex FFT yields two seperate 256 point real results.
06	BFCT	Real Only FFT-Double Length. Performs a double length FFT if the input data was real only, i.e. performing a 256 point complex FFT yields a 256 unique points of 512 result. (N Output)
0E	BFCT2	Real Only FFT-Double Length. Performs a double length FFT if the input data was real only, i.e. performing a 256 point complex FFT yields a 512 point real result. (2N Output)
08	BCFIR	Complex finite impulse response (FIR) filter
09	BDFIR	Double real finite impulse response (FIR) filter
0A	BRFIR	Real finite impulse response (FIR) filter

* For dual chip, seamless cascading

Table 2. Function Set Summary (cont.)

OPCODE	MNE-MONIC	DESCRIPTION
DSP FUNCTIONS (cont.)		
17	FOLD2	Weighted Overlap Add Function (WOA). Performs a vector multiply against an input window followed by a 2 point add. The result is a N/2 size array.
1F	FOLD4	Weighted Overlap Add Function (WOA). Performs a vector multiply against an input window followed by a 4 point add. The result is a N/4 size array.
14	FOLD8	Weighted Overlap Add Function (WOA). Performs a vector multiply against an input window followed by a 8 point add. The result is a N/8 size array.
15	FOLD16	Weighted Overlap Add Function (WOA). Performs a vector multiply against an input window followed by a 16 point add. The result is a N/16 size array.
16	FOLD32	Weighted Overlap Add Function (WOA). Performs a vector multiply against an input window followed by a 32 point add. The result is a N/32 size array.

Table 3. Data Flow Instructions

PORTS AFFECTED	HEX CODE	MNEMONIC	PORTS AFFECTED	HEX CODE	MNEMONIC
READ A READ B WRITE C	053	RA RB WC	READ C READ D WRITE A	0E1	RC RD WA
READ A READ B WRITE D	054	RA RB WD	READ C READ D WRITE B	0E2	RC RD WB
READ A READ B WRITE E	055	RA RB WE	READ C READ D WRITE E	0E5	RC RD WE
READ A READ C WRITE B	05A	RA RC WB	READ C READ E WRITE A	0E9	RC RE WA
READ A READ C WRITE D	05C	RA RC WD	READ C READ E WRITE B	0EA	RC RE WB
READ A READ C WRITE E	05D	RA RC WE	READ C READ E WRITE D	0EC	RC RE WD
READ A READ D WRITE B	062	RA RD WB	READ D READ A WRITE B	10A	RD RA WB
READ A READ D WRITE C	063	RA RD WC	READ D READ A WRITE C	10B	RD RA WC
READ A READ D WRITE E	065	RA RD WE	READ D READ A WRITE E	10D	RD RA WE
READ A READ E WRITE B	06A	RA RE WB	READ D READ B WRITE A	111	RD RB WA
READ A READ E WRITE C	06B	RA RE WC	READ D READ B WRITE C	113	RD RB WC
READ A READ E WRITE D	06C	RA RE WD	READ D READ B WRITE E	115	RD RB WE
READ B READ A WRITE C	08B	RB RA WC	READ D READ C WRITE A	119	RD RC WA
READ B READ A WRITE D	08C	RB RA WD	READ D READ C WRITE B	11A	RD RC WB
READ B READ A WRITE E	08D	RB RA WE	READ D READ C WRITE E	11D	RD RC WE
READ B READ C WRITE A	099	RB RC WA	READ D READ E WRITE A	129	RD RE WA
READ B READ C WRITE D	09C	RB RC WD	READ D READ E WRITE B	12A	RD RE WB
READ B READ C WRITE E	09D	RB RC WE	READ D READ E WRITE C	12B	RD RE WC
READ B READ D WRITE A	0A1	RB RD WA	READ E READ A WRITE B	14A	RE RA WB
READ B READ D WRITE C	0A3	RB RD WC	READ E READ A WRITE C	14B	RE RA WC
READ B READ D WRITE E	0A5	RB RD WE	READ E READ A WRITE D	14C	RE RA WD
READ B READ E WRITE A	0A9	RB RE WA	READ E READ B WRITE A	151	RE RB WA
READ B READ E WRITE C	0AB	RB RE WC	READ E READ B WRITE C	153	RE RB WC
READ B READ E WRITE D	0AC	RB RE WD	READ E READ B WRITE D	154	RE RB WD
READ C READ A WRITE B	0CA	RC RA WB	READ E READ C WRITE A	159	RE RC WA
READ C READ A WRITE D	0CC	RC RA WD	READ E READ C WRITE B	15A	RE RC WB
READ C READ A WRITE E	0CD	RC RA WE	READ E READ C WRITE D	15C	RE RC WD
READ C READ B WRITE A	0D1	RC RB WA	READ E READ D WRITE A	161	RE RD WA
READ C READ B WRITE D	0D4	RC RB WD	READ E READ D WRITE B	162	RE RD WB
READ C READ B WRITE E	0D5	RC RB WE	READ E READ D WRITE C	163	RE RD WC

On all single operand functions like CMAG, the second read port is ignored Example: RAREWD becomes RAWD
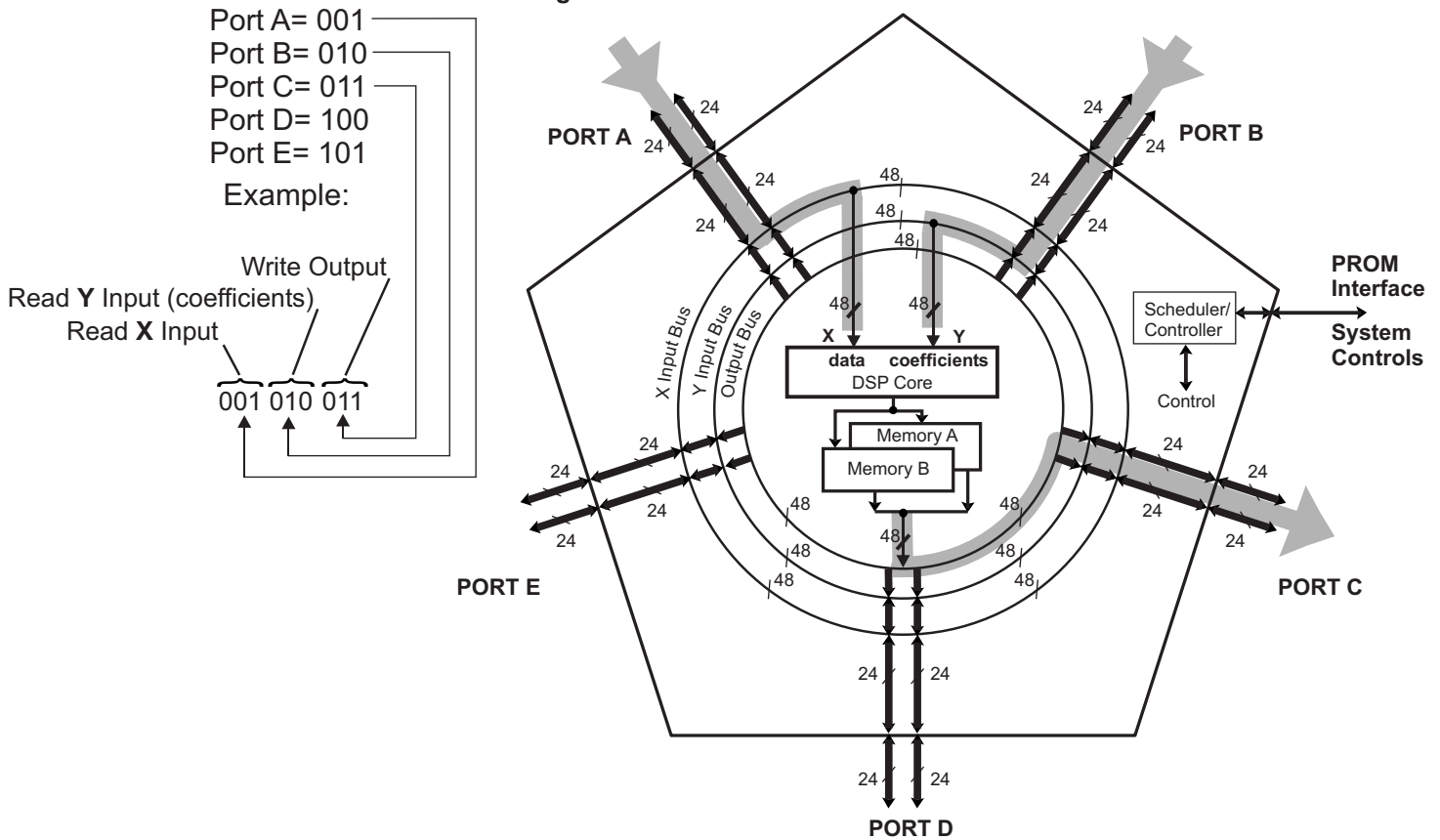
Figure 3. Data Flow Instructions

Port A= 001
Port B= 010
Port C= 011
Port D= 100
Port E= 101

Example:

Write Output
Read **Y** Input (coefficients)
Read **X** Input

001 010 011

Table 4. Function latencies

MNEMONIC	OPCODE	LATENCY	MNEMONIC	OPCODE	LATENCY
BFLY2	2	31	*VWND1K	2F	1301
BFLY4	1	118	*BWND32	20	275
BFLY8	B	171	*BWND64	21	307
BFLY16	0	224	*BWND128	22	371
BFLY32	F	277	*BWND256	23	499
VWND2	17	28	*BWND512	3	755
VWND4	1F	116	BFCT	6	79
VWND8	14	169	BFCT2	E	80
VWND16	15	222	BRFT	7	47
VWND32	16	275	BCFIR	8	47
BWND2	5	48	BDFIR	9	23
BWND4	4	135	BRFIR	A	26
BWND8	25	188	CMAG	C	29
BWND16	24	241	CMUL	D	47
*BFLY64	26	343	VMUL	12	26
*BFLY128	27	407	VADD	10	26
*BFLY256	28	535	VSUB	11	26
*BFLY512	29	791	VNAND	18	12
*BFLY1K	2A	1303	VNOR	1A	12
*VWND64	2B	341	VXNOR	1B	12
*VWND128	2C	405	MOVC	1D	12
*VWND256	2D	533	MOVD	1C	12
*VWND512	2E	789	VPAS	19	12

Latencies vary depending on weather the RHDSP24 is used in parallel or recursive
configurations, see RHDSP24 Users Guide.
*These instructions require two RHDSP24 chips in cascade

DATA FLOW SUMMARY

Each function requires a data flow opcode DF[8:0] that specifies what ports are to be used to input the operands and what port (Or internal memory) the result of the function code is to be written to. Using Table 3, the user selects the input port as the X input and the input port for the Y input, if any.

The example next to Table 3 shows the mnemonic of RARCWB. This means to read port A as the X input data, read port C as the Y input data, and write port B with the result of the function performed.

The user supplied binary code for the RARCWB data flow pattern is 001 for port A, 011 for port C, and 010 for port B. The hex code for 001 011 010 is 05A.

As another example, Figure 3 illustrates the data flow pattern of RARBWC and a function code for a complex multiply (CMUL).

The required operands enter the chip through the A and B ports, appear at the X and Y inputs to the internal core logic, respectively.

The core logic performs a 24-bit complex multiply resulting a complex result of the form X+jY appearing after a latency at the C port.

Table 4 lists the resulting latency for each type of function that the RHDSP24 can perform. When the RHtMMU24 is used in a design, it automatically compensates for the latency for each function code, including any latency generated by using pipelined memories in the system.

FUNCTIONAL DESCRIPTION

The RHDSP24 is the latest generation of real time DSP designed to facilitate the handling of fast real time digital signals with a minimum of software overhead.

The RHDSP24 is organized into five major groups:

• Input and Output Data Ring Buses

• Core Logic

• Internal Memories

• Scheduler/Controller

• Control Inputs

These major groups work in tandem to acquire complex or real data, apply functions on the acquired arrays of data, and store results both internally and externally for further processing, or output.

INPUT AND OUTPUT RING BUSSES

Data enters the RHDSP24 through any of its five complex data ports and exits the RHDSP24 through any of its complex five ports.

The internal ring busses give the user complete control on which port to input operands from and which ports to output the results through. This elaborate internal structure frees the end user from virtually any need to multiplex data external to the RHDSP24.

Additionally the five ports can be used to seamlessly cascade multiple chips as illustrated in the System Configurations section.

CORE LOGIC

The internal data path is designed to execute Fast Fourier Transforms (FFTs) with efficiency and precision.

The core is will execute thirty four high level functions on the incoming data. Functions as sophicated as radix-1024 are performed at the full data rate.

Each input complex pair of data is operated upon by

the core using a super pipelined approach. This approach allows many operations to be performed on each clock cycle.

The core logic reconfigures itself transparent to the user to facilitate unique parallel processing configurations that can command the needed performance to execute a 1024 point by 1024 point complex 2-D FFT at a 75 MHz sample rate sustained, when four chips are used.

INTERNAL MEMORIES

The RHDSP24 contains two banks of internal memory, each organized as 1024 words by 48 bits each. This memory is used to cascade multiple chips.

Cascading of RHDSP24 chips for more performance and higher sampled data rates uses the internal memories to store computed FFT columns before passing the complex data to the next chip connected to the output pins. See the System Configurations section.

Through proper use of the internal memories, complete real time systems may be scaled up or down in performance by adding multiple ASIC silicon RHDSP24 cores on one die, by cascading multiple multiple die in one multi-chip module (MCM), by parallelizing multiple packaged chips on a board, or by parallelizing multiple boards in a unit.

SCHEDULER/CONTROLLER

To enable complete real time systems with minimum effort, the RHDSP24 contains all the circuitry to implement a robust application controller. The SCHEDULER/CONTROLLER maintains the users application by sourcing a series of instructions for the RHDSP24 itself and for any Memory Management Units (MMUs) in the system.

The overall system control is accomplished through a combination of register programming and scheduling of control signals to synchronize the system resources in a timely manner to perform the required operations at maximum system performance. See the RHDSP24 Software Programming Manual for addition details.

SCHEDULER/CONTROLLER (cont.)

The SCHEDULER/CONTROLLER plays a dual role in the overall system operation. Its primary role involves synchronously scheduling the events needed to perform demanding real time signal processing. This scheduling essentially takes the user provided program as it exists in the external PROM/RAM and parses it to both the external RHtMMU24's and the internal DSP controllers.

The SCHEDULER/CONTROLLER's secondary role is to program both the RHDSP24 and any RHtMMU24's that reside in the system. These controllers provide a robust structure for efficient operation of all the resources in a typical real time system, including systems that contain multiple RHDSP24's for increased performance.

Figure 4. illustrates the SCHEDULER, both internal CONTROLLERS, and the required external program PROM.

CONTROL INPUTS

For increased system flexibility, the user may select between using the internal SCHEDULER/ CONTROLLER and supplying the necessary control signals themself. This option is exercised through either grounding the SCHSEL input pin, or connecting the SCHSEL pin to VCC.

If SCHSEL is grounded, the user will be required to manage the signals shown in Figure 5.

Note: Most of the signal pins shown in Figure 5 are dual function pins whose function depend on the state of the SCHSEL pin.

DSP
Architectures

Figure 4. SCHEDULER/CONTROLLER

SCHSEL

GO[1:0]

MMU_TC_A
MMU_TC_B
MMU_TC_C
MMU_TC_D
MMU_TC_E

SCHEDULER

BUSY

Internal
Signals
when
SCHSEL
is active

DSP
CONTROLLER

RESET
START/$\overline{STOP}$
FC[5:0]
DF[8:0]
ENA
ENB
XSFISEL
XSFI[3:0]
YSFI[3:0]
XCI
XCR
DOCR
DOCI
YCI
YCR
XZI
YZI
DZO
XSWAP

MMU
CONTROLLER

MMU_R/$\overline{W}$
MMU_A0
MMU_START
MMU_CS_A
MMU_CS_B
MMU_CS_C
MMU_CS_D
MMU_CS_E

ALG[7:0]

+

$\overline{ADDREN}$

ADDR[15:0]

SCH_DB[7:0]

To Memory Management Units
(RHtMMU24s)

EXTERNAL
PROM

$\overline{CS}$

Figure 5. RHDSP24 Control/ Sync
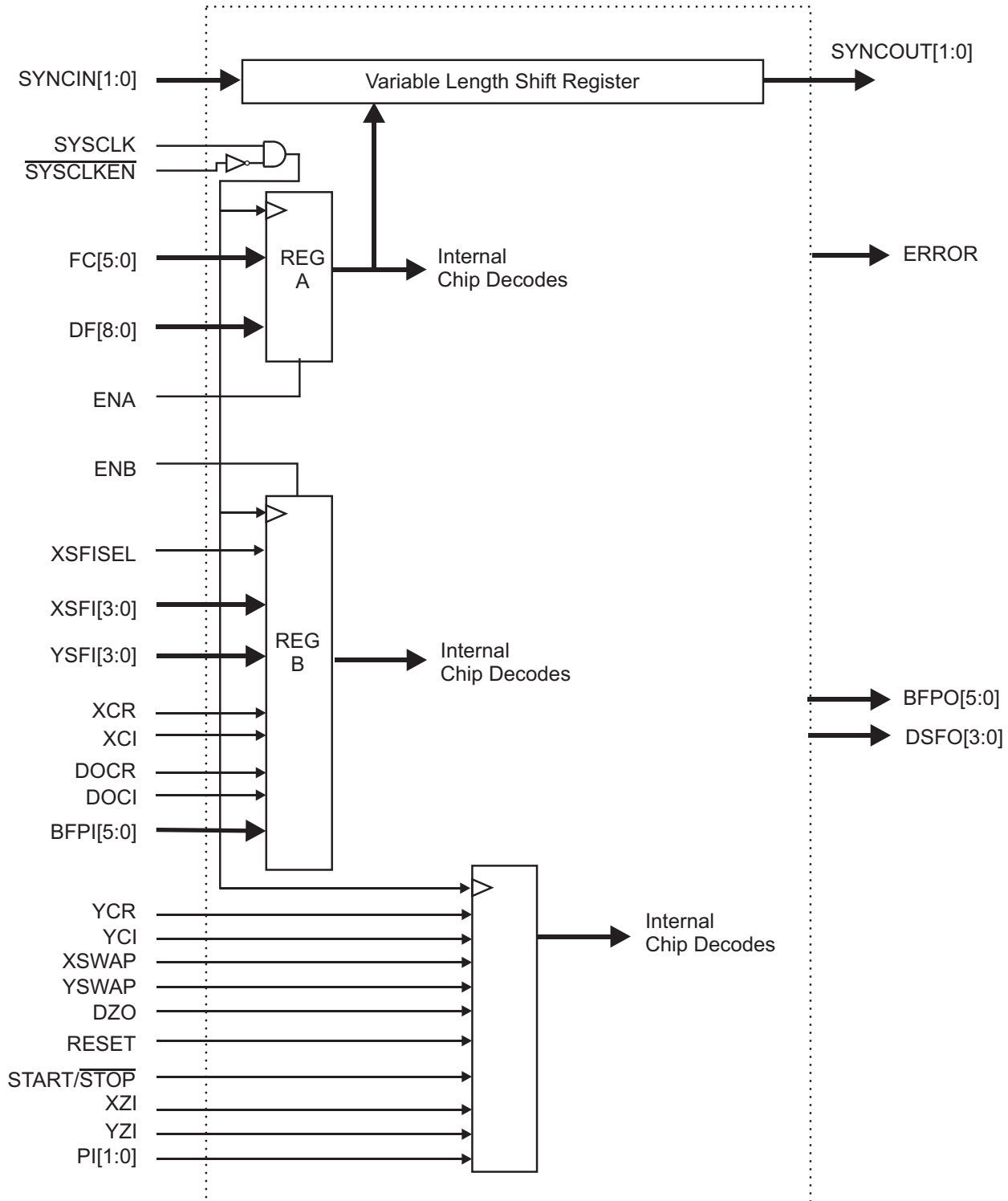
DATA FORMATS

INPUT/OUTPUT DATA FORMATS

The RHDSP24 supports (2) two input data streams: one for real and one for imaginary data. For CMAG and FIR operations, the 26-bit output from each ALU accumulation is rounded to 24 bits and output from the RHDSP24 one on the real side and one on the imaginary side. All other outputs are rounded to 24 bits.

BLOCK FLOATING-POINT

For the radix butterfly transform operations, block floating-point data dependent scaling is provided. This preserves the signal-to-noise ratio by extending the dynamic range of the fixed-point operations.

For each pass of a FFT, or on a separation pass, a scale factor is provided on the DSFO [2:0] pins at the completion of that pass. The scale factor is a binary shift number calculated from the size of the largest complex value output in that pass. Also, it is a worst case prediction of how large the magnitude of the largest complex value could be on the next pass. The magnitude is measured for each complex value output in the pass. The maximum magnitude is compared to many threshold values. If the magnitude is greater, the corresponding shift value (from an internal lookup table) is output on DSFO [3:0]. It is used at the beginning of the next pass on the XSFI [3:0] pins and causes a right shift of the real and imaginary 24-bit inputs to prevent overflow on the pass.

The BFPO [5:0] is the accumulated scale factor for the entire transform and is valid upon the transform's completion. The BFPO and BFPI pins should be connected together for single and parallel chip applications, or connected serially for cascaded operations.

ROUNDING/SHIFTING OPERATION

All data input to the RHDSP24 passes through a shifter and rounder at both the input and output stages. The amount of shifting and rounding is determined by the current instruction. To correctly scale the incoming data, the shifter is capable of shifting up to (16) sixteen bit positions (Defined by XSFI and YSFI) to the right. The rounder trims the data to the necessary 24 bits needed by monitoring the 25th bit (1/2 of the LSB) and adding:

Fractional	XXXXXXX
Rounding	+0000008
	XXXXXX

When bit 25 is set, the output is rounded up, otherwise the data is not rounded.

THEORY OF OPERATION

FUNCTION SET OVERVIEW

The RHDSP24 is a high-performance array processor designed to perform operations on large arrays of data. Accordingly, the RHDSP24 has a powerful function set in the sense that each function opcode accomplishes a substantial task. The following are some key points about the RHDSP24 function set.

- Since the RHDSP24 is a pass-based processor, each function is valid for one complete pass. Each opcode defines a basic flow for the desired operation. This basic data flow is then repeated for multiple pairs of data to complete one pass.

- Each function is qualified by the START/$\overline{STOP}$ signal to indicate the beginning of a pass and end of a pass respectively.

- The Transform functions can also be qualified by XZI, YZI and DZO signals which, when asserted, cause the RHDSP24 to input a string of zeros to the X or Y bus, or force output data to zeros respectively. This feature allows a user to zero fill and zero pad the data on any given pass.

- Functions can also be qualified by XCR/XCI, YCR/YCI, DOCR/DOCI, XSWAP, and YSWAP signals which, when asserted, cause the RHDSP24 to conjugate or swap data on the X, Y, or Output buses. This feature allows a user to perform Inverse transforms, Coefficient compression, or user defined manipulation of input/output data.

- The RHDSP24 function set consists of five functional groupings. A 6-bit opcode is assigned to each function, with a total of thirty-four functions supported. The function code on the pins FC[5:0] must be setup at least three machine cycles ahead of data setup. This allows the automatic scaling factor to be decoded for the next pass. For a typical array processing application, such as FFTs, first a function code is set up (e.g., BFLY32),and then the whole data array is clocked into the RHDSP24. The applied function will then be applied to the whole array.

- There is a latency, given in machine cycles when implementing the RHDSP24 functions (see Table 4.) This latency is automatically compensated for when the RHtMMU24 is used in a system.

THEORY OF OPERATION (cont.)

FUNCTION SET OVERVIEW (cont.)

There are provisions, useful for implementing inverse FFTs, to conjugate the inputs to, and the outputs from, the complex arithmetic functions (pins XCI and DOCI). Similarly, the input and output data values can be complemented for the vector arithmetic and logical functions. The RHDSP24 also includes a PASS/MOVD general purpose function, this function moves data and coefficients between ports and through the execution unit without altering their value.

INPUT/OUTPUT DATA FLOW

Data input to and output from the RHDSP24 depends upon the data flow function given (reference Table 3).

TWO REAL TRANSFORMS (BRFT)

The BRFT function may be used to process two frames of real-data simultaneously and obtain almost twice the performance while still using a complex data FFT.

Given two real sequences, h(n) and g(n), they can be concatenated and represented as a complex sequence, such as: $x(n) = h(n) + jg(n)$. To compute the BRFT do the following:

1. Functions h(k) and g(k) are real

$$k = 0, 1, ..., N - 1$$

2. Form the complex function

$$Y(k) = h(k) + jg(k) \quad k = 0, 1, ..., N - 1$$

3. Compute the FFT

$$Y(n) = \sum_{k=0}^{N-1} y(k)e^{-j2\pi nk/N}$$

$$= R(n) + jI(n) \quad n = 0, 1, ..., N - 1$$

Where R(n) and I(n) are the real and imaginary parts of Y(n), respectively.

4. Compute the separation

$$H(n) = \left[\frac{R(n)}{2} + \frac{R(N-n)}{2} \right] + j \left[\frac{I(n)}{2} - \frac{I(N-n)}{2} \right]$$

$$G(n) = \left[\frac{I(n)}{2} + \frac{I(N-n)}{2} \right] - j \left[\frac{R(n)}{2} - \frac{R(N-n)}{2} \right]$$

$$n = 0, 1, ..., N-1$$

Where H(n) and G(n) are the discrete transforms of h(k) and g(k), respectively.

DOUBLE LENGTH RECOMBINATION OF FFT OUTPUT (BFCT)

This pass performs both a fast cosine transform recombination and a double length separation. Double Length Separation separates a 2N length real FFT from a N length complex FFT as follows:

1. Function x(k) is real

$$k = 0, 1, ..., 2N - 1$$

2. Divide x(k) into two functions

$$h(k) = x(2k)$$

$$g(k) = x(2k + 1) \quad k = 0, 1, ..., N - 1$$

3. Form the complex function

$$Y(k) = h(k) + jg(k) \quad k = 0, 1, ..., N - 1$$

4. Compute the FFT

$$Y(n) = \sum_{k=0}^{N-1} y(k)e^{-j2\pi nk/N}$$

$$= R(n) + jI(n) \quad n = 0, 1, ..., N - 1$$

Where R(n) and I(n) are the real and imaginary parts of Y(n), respectively.

5. Compute the separation

$$Xr(n) = \left[\frac{R(n)}{2} + \frac{R(N-n)}{2} \right] + \cos\frac{\pi n}{N} \left[\frac{I(n)}{2} + \frac{I(N-n)}{2} \right]$$

$$- \sin\frac{\pi n}{N} \left[\frac{R(n)}{2} - \frac{R(N-n)}{2} \right] \quad n = 0, 1, ..., N-1$$

$$Xi(n) = \left[\frac{I(n)}{2} - \frac{I(N-n)}{2} \right] - \sin\frac{\pi n}{N} \left[\frac{I(n)}{2} + \frac{I(N-n)}{2} \right]$$

$$- \cos\frac{\pi n}{N} \left[\frac{R(n)}{2} - \frac{R(N-n)}{2} \right] \quad n = 0, 1, ..., N-1$$

Where $x_r(n)$ and $x_i(n)$ are respectively the real and imaginary parts of the 2N point discrete transform of x(k).

NOTES:

1. Only N points of the complex output are unique since the real only input function produces even real/ odd imaginary output..

2. The RHDSP24 does not perform the division by two in the BRFT, BFCT, and BFCT2 functions. This was done to allow the user to perform the division by two, if so decided.

3. The Sine component of the COS/SIN table is assumed to be stored as an inverse. (Therefore the internal implementation of the above equations multiplies the SIN component by -1.)

SYSTEM OVERVIEW

The RHDSP24 incorporates a unique architecture optimized for extremely high data throughput and minimal hardware/software system development. For example, the digital filter example of Figure 7, is executed using a 4096 point forward FFT, a multiplication, and an inverse FFT, using the following program.

BWND4 +Window Column 1

BFLY32 Column 2

BFLY32 Column 3

Conjugate Input BWND4 + Complex multiply Column 4

BFLY32 Column 5

Conjugate Output BFLY32 Column 6

For a 4K transform, there are three columns using the radix-4 and radix-32 operations. Each column represents one "pass". A "pass" is transferring data from one memory bank (A, B, C, D, or E), through the machine to the other memory bank (A, B, C, D, or E). During each pass the RHDSP24 performs a DSP function on the data using coefficients from the coefficient port, if necessary.

As shown in Figure 7 the data is first input through RHDSP24 and a window function is combined with the first column of the FFT. Next the data is passed a second time through the RHDSP24 performing a radix32 operation, the third pass back through the RHDSP24 performs another radix32 operation. This completes the forward FFT including the window function multiply.

For the forth through sixth passes through the RHDSP24, these same three pass operations are repeated with the window function being replaced with the desired filter coefficients. The data is also conjugated on the input side of the fourth pass and conjugated on the output side on the sixth pass to perform the Inverse FFT.

This approach to real time DSP can be proportionally accelerated by adding multiple RHDSP24's in the data flow, the following section on system configurations illustrates this.

Figure 7
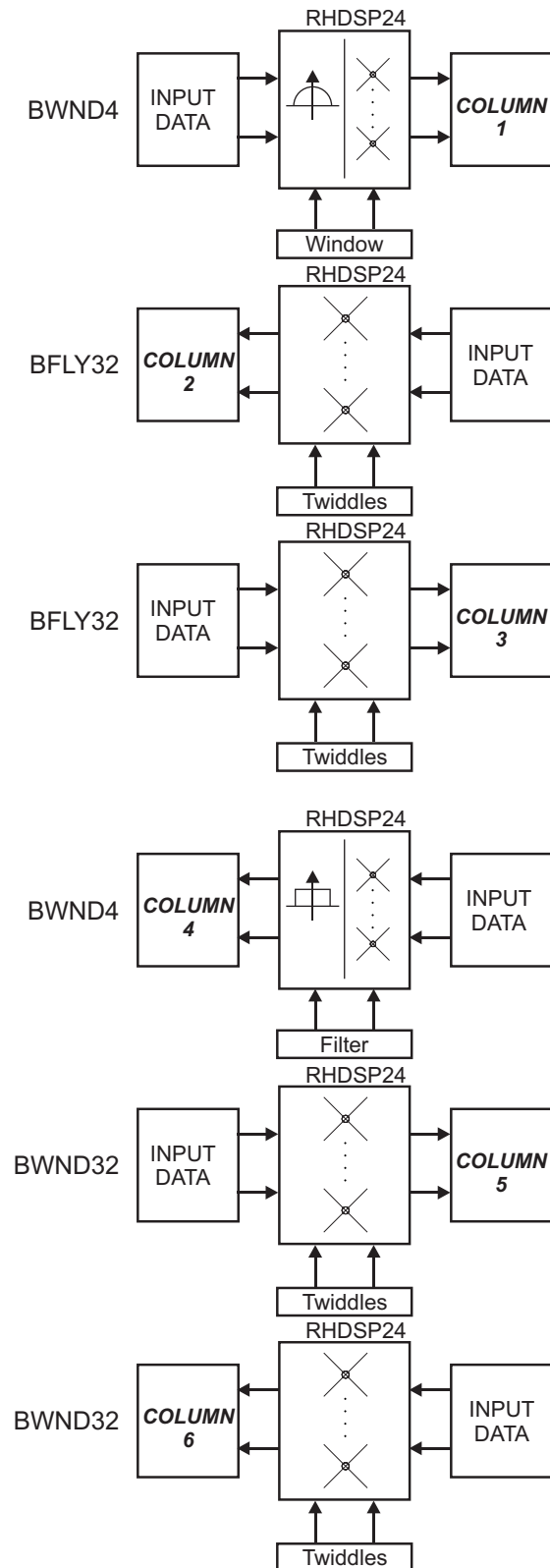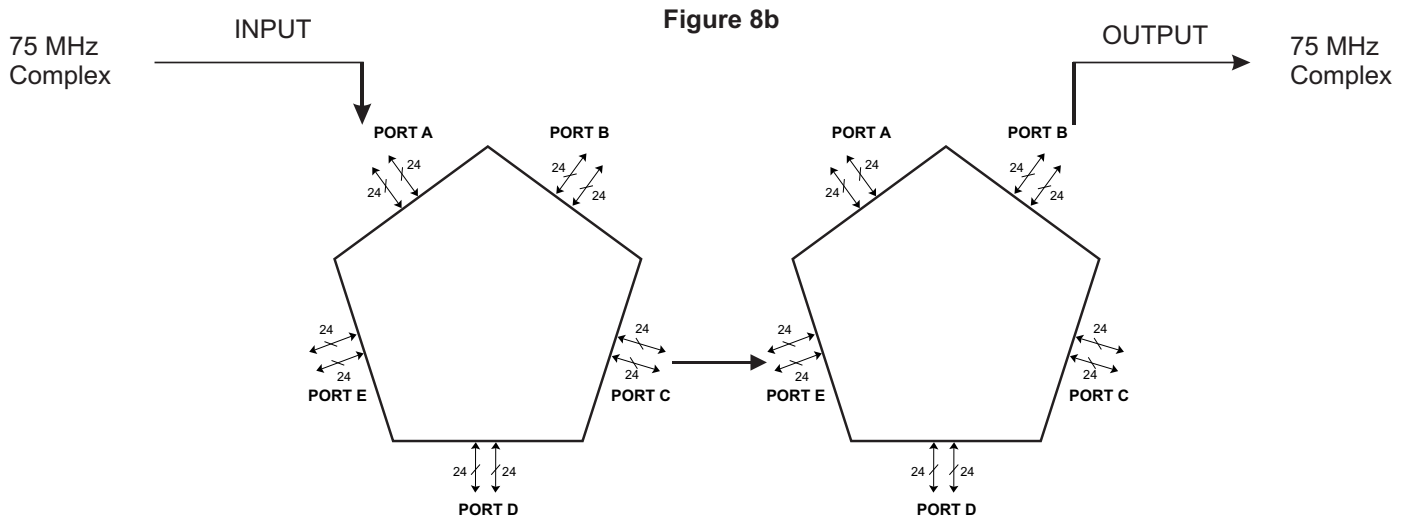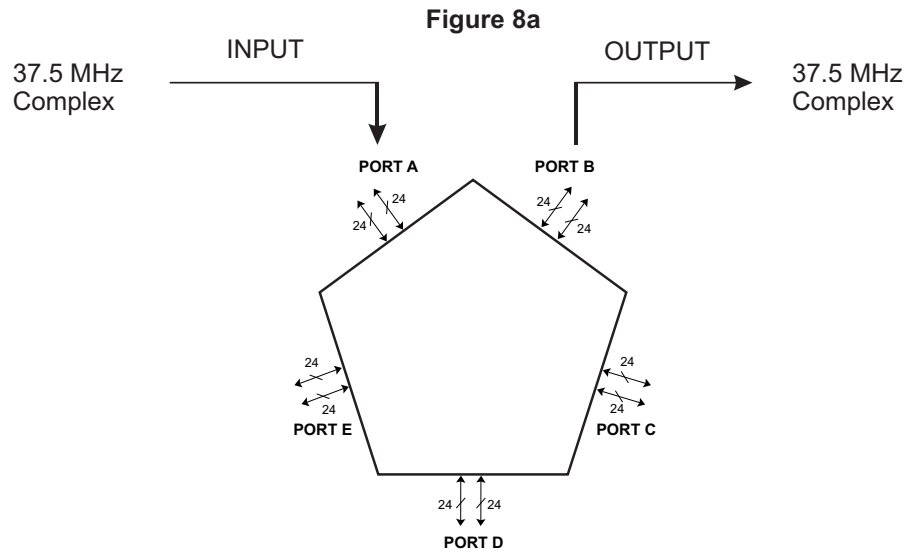
Figure 8a

Figure 8b

SYSTEM CONFIGURATIONS

For several applications, the RHDSP24 may be used alone without external components as shown in Figure 8a. This configuration will perform a 1024 point complex FFT in just two passes, for a continuous sampling rate of 37.5 MHz complex.

The 37.5 MHz performance may be scaled up to 75 MHz by simply adding another RHDSP24 die in the package or two packaged chips back to back, see Figure 8b.

For larger arrays, external memories and external Memory Management Units (RHtMMU24's) may be required, as shown in Figure 9a. The addition of these simple external devices will support arrays up to 1 million complex points.

Again two packaged chips, or two die may be cascaded back to back as shown in Figure 9b to increase performance.

Figure 10 shows the four data flow phases required for two RHDSP24 chips performing a four pass operation such as a 2-D 1024 point complex FFT followed by a 2-D 1024 point inverse complex FFT.

As shown in Figure 10a data enters port A of the first RHDSP24 #1 along with the required twiddle factors through port D. This data is processed through the core logic of RHDSP24 #1 and passes out of port C to the input port E of RHDSP24 #2.

The data then exits RHDSP24 #2 through port C into the memory connected to port C. This completes the first of four passes.

The second, third, and fourth passes of the algorithm are shown in Figure 10b, 10c, and 10d respectfully. The data is ping ponged in this fashion for the total required number of passes.

DSP
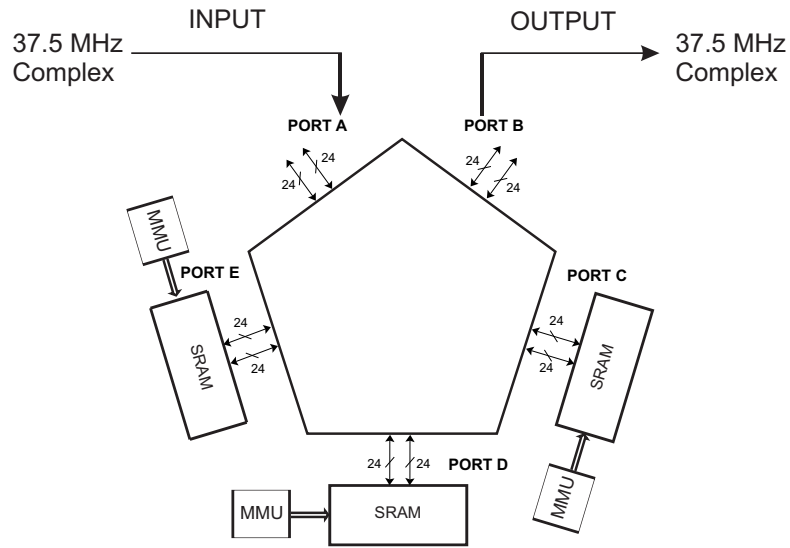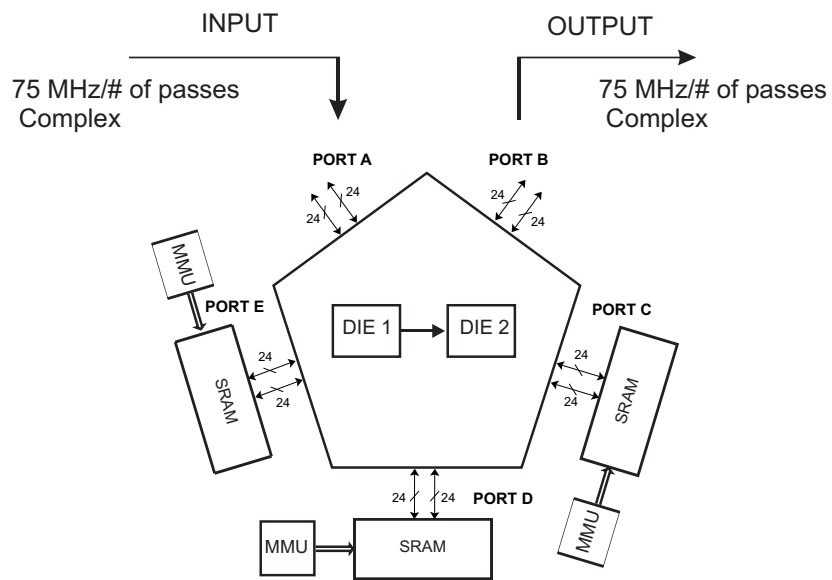Architectures

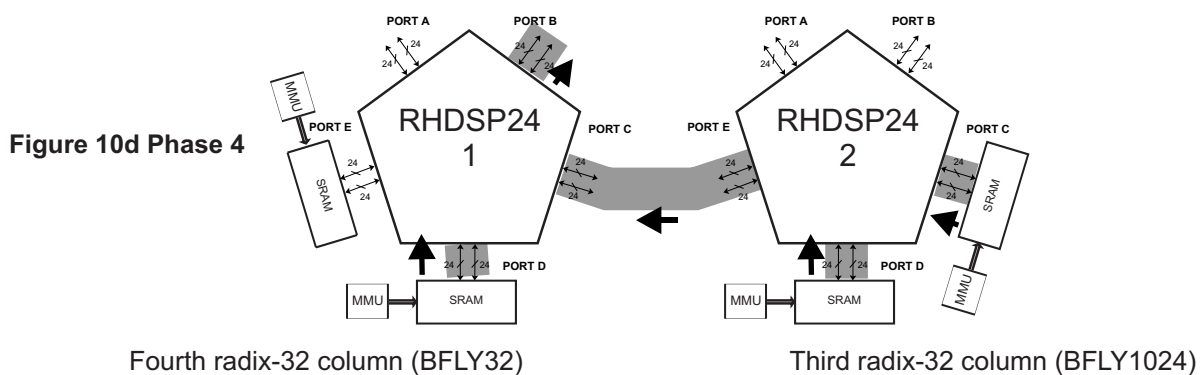## Figure 9a

INPUT   OUTPUT

37.5 MHz
Complex

37.5 MHz
Complex

PORT A   PORT B

24   24

24   24

MMU

PORT E   PORT C

24   24

SRAM   24   24   SRAM

MMU

24   24   PORT D

MMU   SRAM

Figure 9b

INPUT   OUTPUT

75 MHz/# of passes
Complex

75 MHz/# of passes
Complex

PORT A   PORT B

24   24

24   24

MMU

PORT E   PORT C

DIE 1 → DIE 2

24   24

SRAM   24   24   SRAM

MMU

24   24   PORT D

MMU   SRAM

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Figure 10   2-D Complex 1K x 1K Fast Convolution

Figure 10a Phase 1

Window and first radix-32 column (VWND1024*)   Second radix-32 column (BFLY32)

Figure 10b Phase 2

Fourth radix-32 column (BFLY32)   Third radix-32 column (BFLY1024*)

Figure 10c Phase 3

Combined filter multiply and first radix-32 IFFT
(VWND1024*) column   Second radix-32 column (BFLY32)

Figure 10d Phase 4

Fourth radix-32 column (BFLY32)   Third radix-32 column (BFLY1024)

* VWND1024 and BFLY1024 perform VWND32 and BFLY32 respectively, in addition to
enabling the internal 'back-to-back' buffer memory.

SYSTEM CONFIGURATIONS (cont.)

Cascading four RHDSP24's yields an impressive 75 MSPS complex FFT with 1 million complex points of resolution, or a 1024x1024 two-dimension(2-D) transform in 14 milliseconds.

Figure 11 shows a Multi-Chip Module (MCM) with four RHDSP24 die connected back to back.

As illustrated in Figure 11a, phase one runs all four die concurrently with the top two chips performing 1024 of the required 1024 point

complex FFT's and storing the result in an external 1 million point RAM. While this is taking place the bottom two chips in the MCM are taking the results from a previous pass and also performing 1024 of the required 1024 point complex FFT's for the final output.

Figure 11b shows the second phase of this concurrent process with the chip pairs swapping working memories, this allows real time processing in a seamless pipelined fashion.
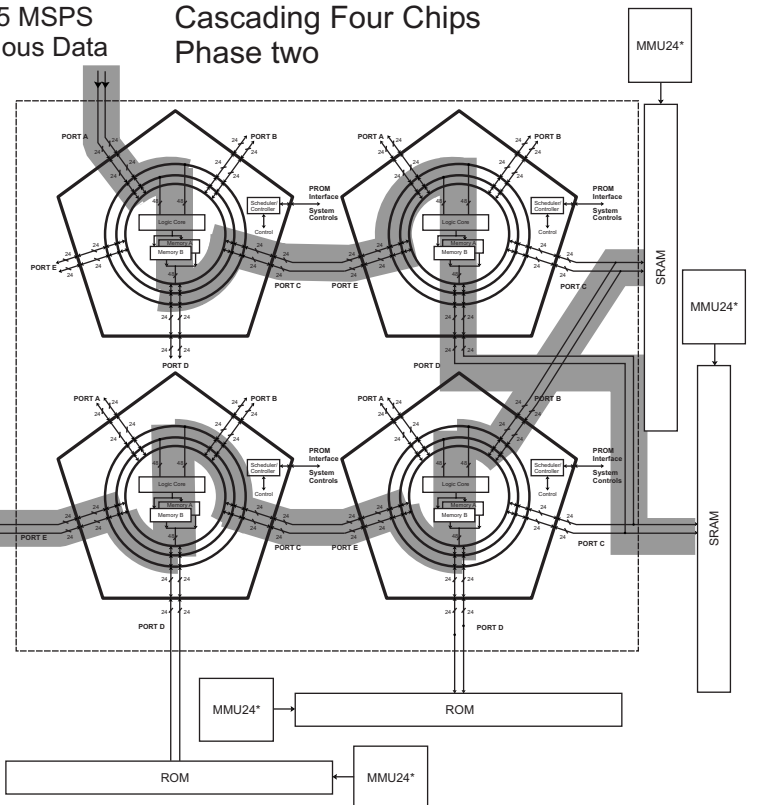
Up tp 75 MSPS
Continuous Data
Input

Up to 75 MSPS
Continuous Data
Output

Figure 11a
Cascading Four Chips
Phase one

Up tp 75 MSPS
Continuous Data
Input
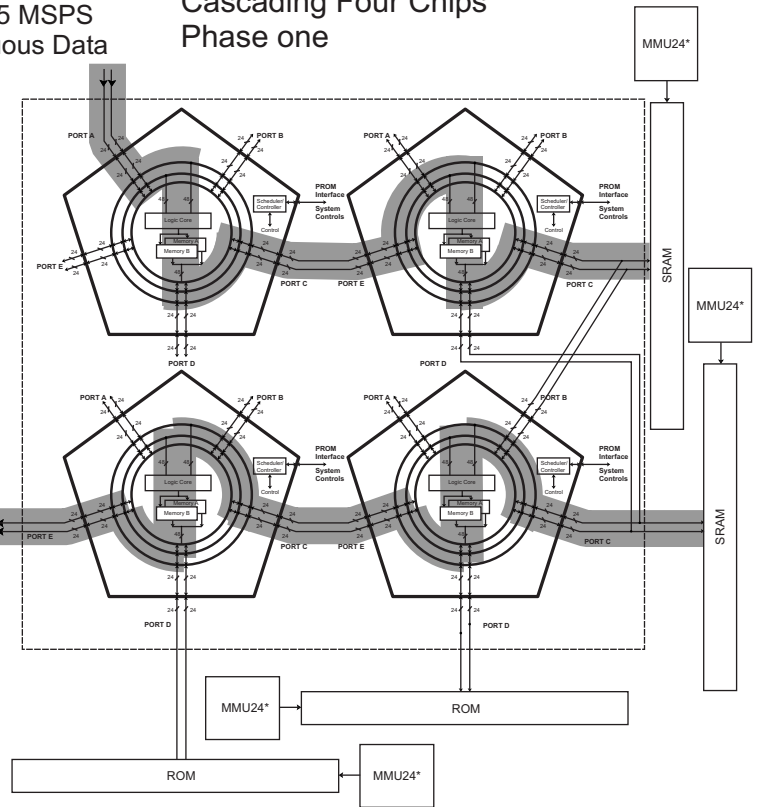
Up to 75 MSPS
Continuous Data
Output

Figure 11b
Cascading Four Chips
Phase two

* One RHtMMU24 incorporates three MMU24's.

ABSOLUTE MAXIMUM RATINGS [1, 2, 3, 4]

	MIN	MAX
DC Supply Voltage (VDD)	-0.5v	4.6v
Input Voltage (VI)	-0.5v	VDD+0.5v (cannot exceed 4.6v)
Output Voltage (VO)	-0.5v	VDD+0.5v (cannot exceed 4.6v)
DC Input Current (II)	-50mA	+50mA
DC Output Current (IOUT)	-50mA	+50mA
Storage Temperature range	-65 C	+150 C
Lead temperature (Soldering, 5 seconds)	—	+270 C
Junction temperature	—	+175 C
Alumina Thermal resistance, junction to case ($_{JC}$)	0.9 C/W	
HITCE Thermal resistance, junction to case ($_{JC}$)	2.0 C/W	
Electrostatic discharge sensitivity (ESDS)	Class 1	
Power Dissipation (Package Limit)	TBD Watts	

OPERATING RANGE [1]

		MIN	MAX	UNIT
TA	Temperature, Ambient	-55	-125	°C
VDD	Supply Voltage	+3.0	+3.6	V
VSS	Supply Voltage	0.0	0.0	V dc
VIL	Logic '0' Input Voltage [7]	0.0 VDD	0.3 VDD	V
VIH	Logic '1' Input High Voltage	0.7 VDD	VDD	V
	Operating frequency	0	75	MHz
	Standby current test frequency	0		Mhz

DC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	TEST CONDITIONS	MIN	MAX	UNIT
I_{LPUI} [8]	Current	VDD=3.13 V, VIN=0 V	TBD	TBD	uA
		VIN=VDD	TBD	TBD	
I_{LPDI} [9]	Pull-Down Input Leakage	VDD=3.13, VIN=VDD	TBD	TBD	
		VIN=VSS	TBD	TDB	
I_{LI}	Input Leakage Current	VDD=3.13 V, VIN= 0 to VDD	TBD	TBD	
V_{LOH}	Output High Voltage	IOH=-6.0 mA	TBD		V
V_{OL}	Output Low Voltage	IOL=6.0 mA		TBD	V
I_{DDI}	Average Supply Current	Measured at tcyc (75MHz)		TBD	mA
I_{DD2}	Average Standby Current	All inputs = VIL (0.3 VDD), Excludes output load current.		TDB	mA
I_{DD3}	Quiescent Standby Current	All inputs = VIL (0.3 VDD), Excludes output load current.		TDB	mA

See notes on Page 26

AC TEST CONDITIONS [1]

PARAMETER	RATING
Input Pulse levels	VSS to TBD VDD
Input Rise & Fall Times (10% to 90%)	TBD ns
Input Timing Reference Levels	(Figure 16a)
Output Reference Levels	TBD VDD
Output Load, Timing Tests	TBD VDD Figure 16b

CAPACITANCE [1,6]

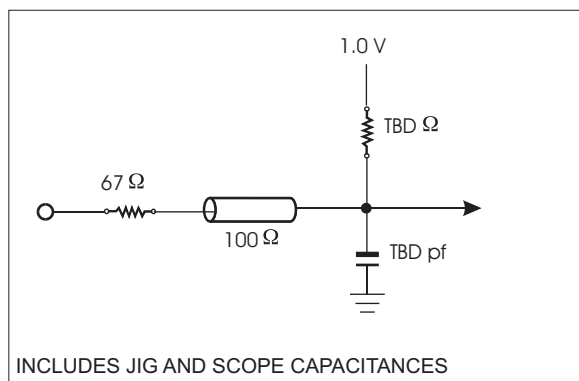| SYMBOL	DESCRIPTION	TEST CONDITIONS	RATING
CIN	Input Capacitance	TA=25 deg C, F=1MHz, VDD=3.13 V	TBD pF
COUT	Output Capacitance	TA=25 deg C, F=1MHz, VDD=3.13 V	TBD pF

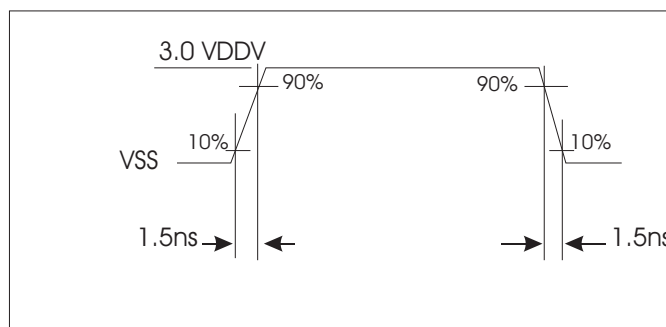**Figure 12a. Output Load Circuit**

Figure 12b. Input Rise and Fall Times

NOTES:

1. All voltages are measured with respect to VSS.

2. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the ' Operating Range' of this specification is not implied.

   Exposure to absolute maximum rating conditions for extended periods may affect reliability.

3. Values are guaranteed but not tested.

4. Storage temperature for Ceramic Dimpled Ball Grid Array Package not to exceed 125°C

5. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

6. Sample tested only

7. The RHDSP24 inputs are able to withstand a -1.0V undershoot for less than 10 ns per cycle.

8. An internal pull-up resistor is attached to all the data bus pins : AR[23:0], AI[23:0], BR[23:0], BI[23:0], CR[23:0], CI[23:0], DR[23:0], DI[23:0], ER[23:0], EI[23:0].

9. An internal resistor is attached to all the non-bus signals to bias them inactive when not physically connected at the board level.

10. IDD is dependent upon actual output loading and cycle rates. Specific values are with outputs open.

DSP
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Radiation Hardening

Total ionizing dose

The Radiation Hardened DSP24 shall meet a Total Ionizing Dose of at least 300 Krad (Si). The Honeywell HX3000 technology has total dose hardness designed in up to 300 Krad. Only requirements above this threshold require further analysis to determine compliance. The total dose requirement for the Radiation Hardened RHDSP24 is met by porting the design to the HX3000 technology.

Single event upset rate

The Radiation Hardened RHDSP24 shall meet two Single Event Upset (SEU) rate requirements. Control logic shall meet 6.7E-6 error/chip-day and Datapath logic shall meet 2.2E-3 error/chip-day. The SEU requirement is met by careful selection of the registers used in the design and by following the guidelines specified in Section 3 and 4 of the Honeywell HX3000 Radiation Design Manual.

Latch-up

The Radiation Hardened RHDSP24 shall be immune to Latch-up. The HX3000 standard cell technology is immune to latch-up by design. The latch-up requirement for the Radiation Hardened RHDSP24 is met by porting the design to the Honeywell HX3000 standard cell technology.

Dose rate

The Radiation Hardened RHDSP24 shall meet a Dose Rate Upset > 1E9 Rad/s. The sizing of the power busses is the main area of concern relating to Dose Rate. Refer to the Honeywell HX3000 Radiation Design Manual for design guidelines.

Radiation hardness/single event phenomena characteristics

Environment	Level	Units	Notes
Total dose	3 E5	rad(Si)	(1)
Soft Error Rate SEU2 (Control Logic) SEU normal (Datapath)	 6,739 x 1 E -9 21,798 x 1 E 7	 error/chip-day error/chip-day	(2) (3)
Dose Rate Upset	> = 1E9	rad(Si)/s	(5)
Transient Dose Rate survivability	> = 1E11	rad(Si)/s	(6)
Neutron Fluence	> = 1E14	N/cm^2	(7)

Notes:
   (1)   Levels up to and including level indicated, TA=25°C
   (2)   No latchup under any recommended operating condition.
   (3)   Equatorial Geosynchronous Environment (Adams 10% worst case), TA=125°C
   (4)   All storage devices
   (5)   Pulse width < 1 us
   (6)   Pulse width < 50 ns, X-ray, VDD= 3.6V, TA =25°C
   (7)   1 MeV equivalent damage in silicon, Unbiased, TA=25°C

Radiation Hardening

For Rad Hard Assurance see:

http://www.dsparchitectures.com/Radiation%20hardness%20Spec%20070803.pdf

DSP
Architectures

AC ELECTRICAL CHARACTERISTICS

SIGNAL	DESCRIPTION	MIN	TYP	MAX
t_{CYC}	SYSCLK Cycle Time	13.4		
t_{CL}	Clock Low Time (SYSCLK)	6.67		
t_{CH}	Clock High Time (SYSCLK)	6.67		
t_{SCLKEN}	SYSCLKEN Setup Time (SYSCLK)	1		
t_{HCLKEN}	SYSCLKEN Hold Time (SYSCLK)	5*		
t_{RESET}	RESET High Time	50*		
t_{SKL}	CLKxIN to SYSCLK, Rising Edge to Rising Edge Skew	14.33		
t_{SKT}	SYSCLK to CLKxIN, Rising Edge to Rising Edge Skew	-2.0*		
t_{DSA}	AR[23:0], AI[23:0] Setup Time (CLKAIN)	6.67		
t_{DHA}	AR[23:0], AI[23:0] Hold Time (CLKAIN)	3		
t_{DODA}	AR[23:0], AI[23:0] Output Delay Time (SYSCLK)			14.5
t_{DOHA}	AR[23:0], AI[23:0] Output Hold Time (SYSCLK)	6.5*		
t_{LZOEA}	AOE High to AR[23:0], AI[23:0] Low-Z			10*
t_{HZOEA}	AOE Low to AR[23:0], AI[23:0] High-Z			10*
t_{DSB}	BR[23:0], BI[23:0] Setup Time (CLKBIN)	6.67		
t_{DHB}	BR[23:0], BI[23:0] Hold Time (CLKBIN)	3		
t_{DODB}	BR[23:0], BI[23:0] Output Delay Time (SYSCLK)			14.5
t_{DOHB}	BR[23:0], BI[23:0] Output Hold Time (SYSCLK)	6.5*		
t_{LZOEB}	BOE High to BR[23:0], BI[23:0] Low-Z			10*
t_{HZOEB}	BOE Low to BR[23:0], BI[23:0] High-Z			10*
t_{DSC}	CR[23:0], CI[23:0] Setup Time (CLKCIN)	6.67		
t_{DHC}	CR[23:0], CI[23:0] Hold Time (CLKCIN)	3		
t_{DODC}	CR[23:0], CI[23:0] Output Delay Time (SYSCLK)			14.5
t_{DOHC}	CR[23:0], CI[23:0] Output Hold Time (SYSCLK)	6.5*		
t_{LZOEC}	COE High to CR[23:0], CI[23:0] Low-Z			10*
t_{HZOEC}	COE Low to CR[23:0], CI[23:0] High-Z			10*
t_{DSD}	DR[23:0], DI[23:0] Setup Time (CLKDIN)	6.67		
t_{DHD}	DR[23:0], DI[23:0] Hold Time (CLKDIN)	3		
t_{DODD}	DR[23:0], DI[23:0] Output Delay Time (SYSCLK)			14.5
t_{DOHD}	DR[23:0], DI[23:0] Output Hold Time (SYSCLK)	6.5*		
t_{LZOED}	DOE High to DR[23:0], DI[23:0] Low-Z			10*
t_{HZOED}	DOE Low to DR[23:0], DI[23:0] High-Z			10*
t_{DSE}	ER[23:0], EI[23:0] Setup Time (CLKEIN)	6.67		
t_{DHE}	ER[23:0], EI[23:0] Hold Time (CLKEIN)	3		
t_{DODE}	ER[23:0], EI[23:0] Output Delay Time (SYSCLK)			14.5
t_{DOHE}	ER[23:0], EI[23:0] Output Hold Time (SYSCLK)	6.5*		
t_{LZOEE}	EOE High to ER[23:0], EI[23:0] Low-Z			10*
t_{HZOEE}	EOE Low to ER[23:0], EI[23:0] High-Z			10*
t_{SA}	ENA Setup Time (SYSCLK)	6.67		
t_{HA}	ENA Hold Time (SYSCLK)	7		
t_{SCTLA}	FC[5:0], DF[8:0] Setup Time (SYSCLK)	6.67		
t_{HCTLA}	FC[5:0], DF[8:0] Hold Time (SYSCLK)	7		
t_{SB}	ENB Setup Time (SYSCLK)	6.67		
t_{HB}	ENB Hold Time (SYSCLK)	7		
t_{SCTLB}	XSFISEL, XSFI[3:0], YSFI[3:0], BFPI[5:0], XCR, XCI, DOCR, DOCI Setup	6.67		
t_{HCTLB}	XSFISEL, XSFI[3:0], YSFI[3:0], BFPI[5:0], XCR, XCI, DOCR, DOCI Hold	7		
t_{SCTLC}	XZI, YZI, DZO, YCR, YCI, YSWAP, XSWAP Setup (SYSCLK)	6.67		
t_{HCTLC}	XZI, YZI, DZO, YCR, YCI, YSWAP, XSWAP Hold (SYSCLK)	7		
t_{ODCTL}	BFPO[5:0], DSFO[3:0] Output Delay Time (SYSCLK)			14.5
t_{SBFPC}	BFPCLR Setup Time (SYSCLK)	6.67		
t_{HBFPC}	BFPCLR Hold Time (SYSCLK)	7		
t_{SSTART}	START/STOP Setup Time (SYSCLK)	6.67		
t_{HSTART}	START/STOP Hold Time (SYSCLK)	7		
t_{SSYNC}	SYNCIN[1:0] Setup Time (SYSCLK)	6.67		
t_{HSYNC}	SYNCIN[1:0] Hold Time (SYSCLK)	7		
$t_{DODSYNC}$	SYNCOUT[1:0] Output Delay Time (SYSCLK)			14.5
$t_{DODPOUT}$	POUT[2:0] Output Delay Time (SYSCLK)			14.5
t_{DODERR}	ERROR Output Delay Time (SYSCLK)			14.5

(heading over MIN/TYP/MAX columns) **75 MHz**

* Estimated worst case timing from static timing analysis

AC ELECTRICAL CHARACTERISTICS

SIGNAL	DESCRIPTION	75 MHz		
		MIN	TYP	MAX
t_{SSCH}	SCHSEL Setup Time (SYSCLK)	6.67		
t_{HSCH}	SCHSEL Hold Time (SYSCLK)	7		
t_{SGO}	GO[1:0] Setup Time (SYSCLK)	6.67		
t_{HGO}	GO[1:0] Hold Time (SYSCLK)	7		
t_{STC}	MMU_TC_A, B, C, D, E Setup Time (SYSCLK)	6.67		
t_{HTC}	MMU_TC_A, B, C, D, E Hold Time (SYSCLK)	7		
t_{HZADDR}	$\overline{ADDREN}$ High to ADDR[15:0] High-Z			9.5*
t_{LZADDR}	$\overline{ADDREN}$ Low to ADDR[15:0] Low-Z			9.5*
t_{ODADDR}	ADDR[15:0] Output Valid Delay Time (SYSCLK)			14.5
t_{SSDB}	SCHDB[7:0] Setup Time (SYSCLK)	6.67		
t_{HSDB}	SCHDB[7:0] Hold Time (SYSCLK)	7		
$t_{ODMRESET}$	MMU_RESET Output Delay Time (SYSCLK)			14.5
t_{ODRW}	MMU_R/$\overline{W}$ Output Delay Time (SYSCLK)			14.5
t_{ODA0}	MMU_A0 Output Delay Time (SYSCLK)			14.5
$t_{ODSTART}$	MMU_START Output Delay Time (SYSCLK)			14.5
t_{ODCS}	MMU_CS_A, B, C, D, E Output Delay Time (SYSCLK)			14.5
t_{ODBUSY}	$\overline{BUSY}$ Output Delay Time (SYSCLK)			14.5
$t_{ODSSYNC}$	SSYNC[1:0] Output Delay Time (SYSCLK)			14.5

Note: *All clocks signals (CLKxIN, SYSCLK) must be driven, or grounded if not used*

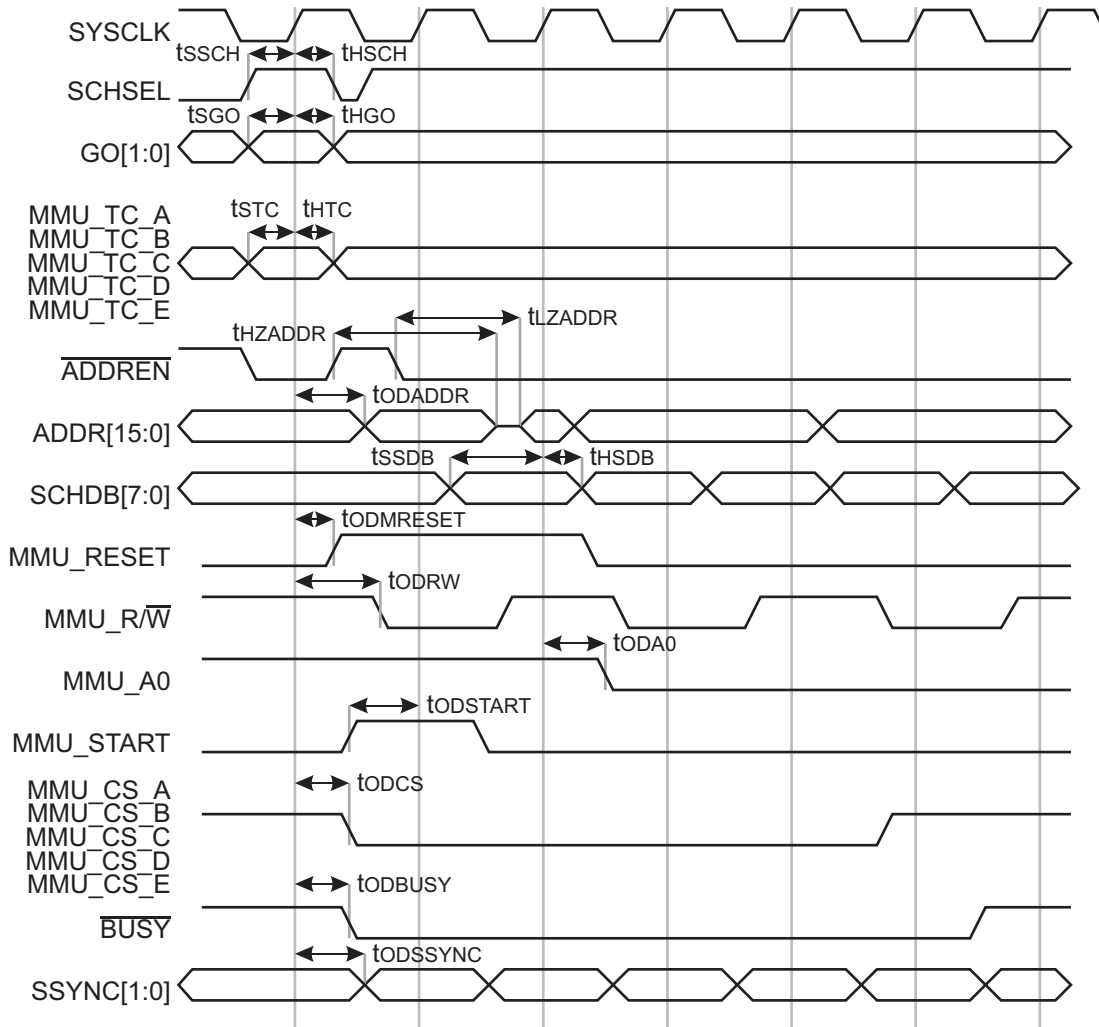** Estimated worst case timing from static timing analysis*

AC ELECTRICAL CHARACTERISTICS

Figure 13. RHDSP24 Timing
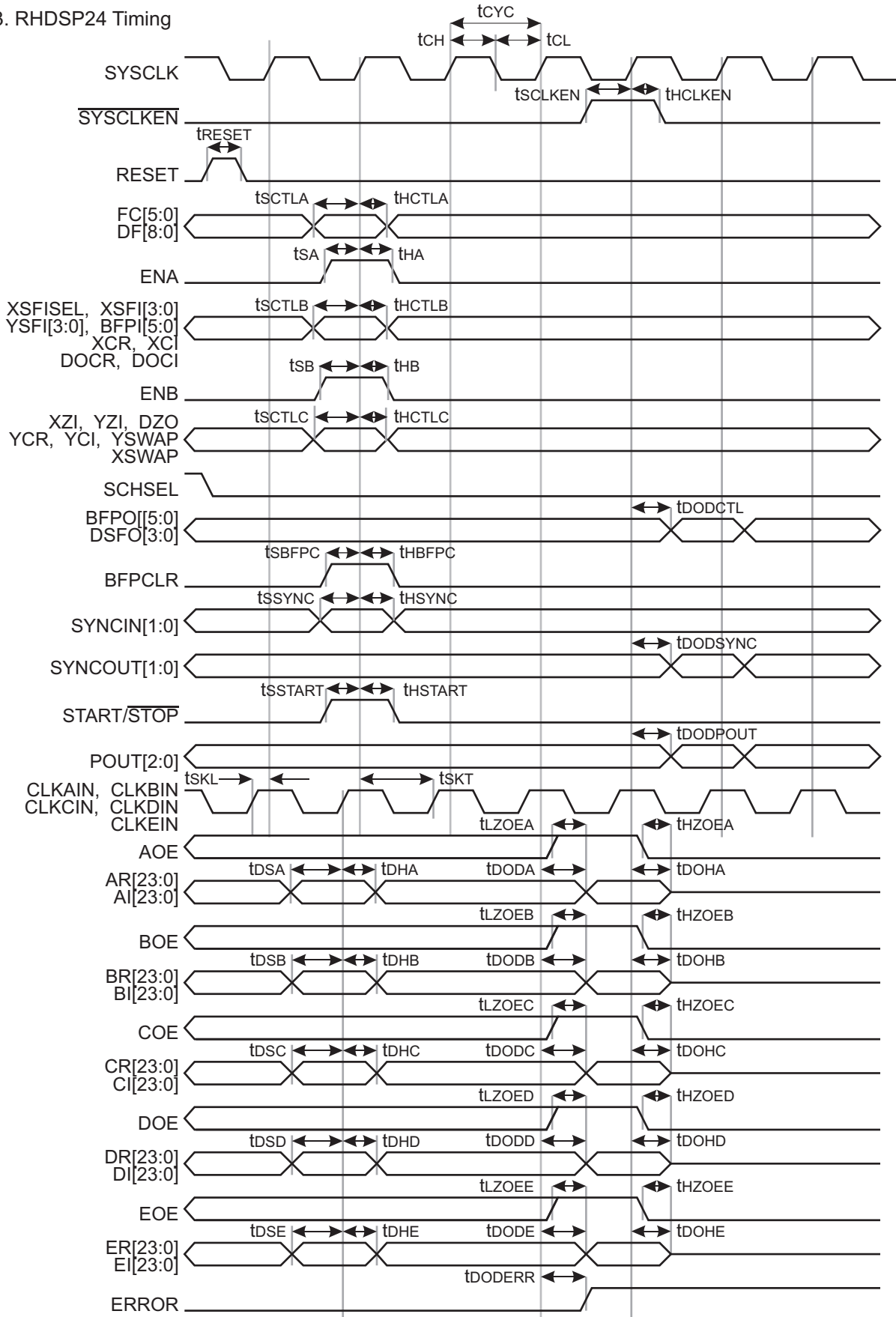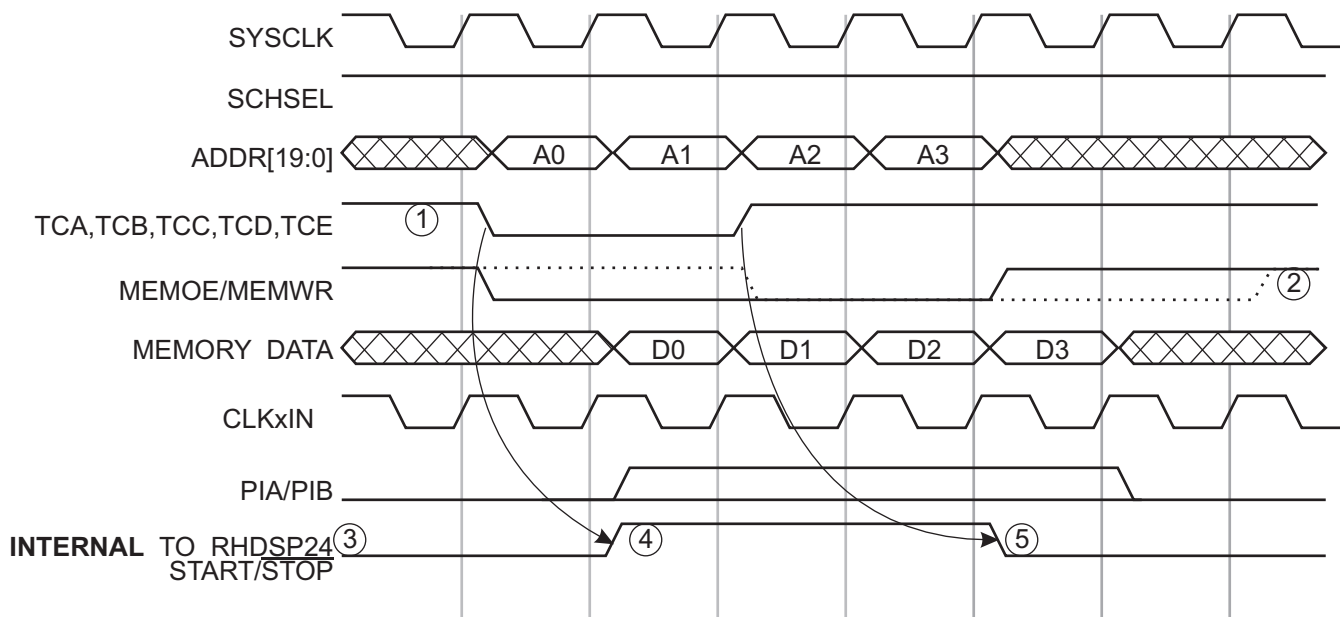
AC ELECTRICAL CHARACTERISTICS

Figure 13. RHDSP24 Timing (Continued)

AC ELECTRICAL CHARACTERISTICS

Figure 14. RHDSP24 Scheduler Mode Timing Diagram

MMU24 to Memory to DSP-24 - Address to Data memory Latency = 1

① Default TC. (SKEW Reg TC Bits 11:9 = 0, MODE Bit 3 = 0)
The TCx used for START/STOP generation is defined by MSB Bits 8:6 of the programed DataFlow.

② Default Showed. Depending on memory type, these signals may need to be skewed.
(SKEW Reg Bits 5:3 move MEMW and Bits 2:0 move MEMOE. 7= -1, 0-6 = 0-6)

③ Internal to DSP-24 the generated START/STOP signal needs to line up with incoming data first point, and go low during the incoming data's last point.

④ The Internal START/STOP rising edge equals Input TC falling edge delayed one clock cycle.

⑤ The Internal START/STOP falling edge equals Input TC rising edge delayed two clock cycles.

System Timing in the Scheduler Mode

When using the RHDSP24's built in Scheduler, the control for specifying the RHDSP24's function, data flow, and various control signals remains the same. However, the source for the contro lsignals has been internally switched to the output of the internal Scheduler.

START/STOP is the most important of these control signals. As shown in Figures14 and15, the internal START/STOP is generated from the TC inputs to the Scheduler.

Since latency of the user SRAM is unknown, a value of 1is used for generating the internal timing, see Figure 14.If another type of external SRAM is used, that has a different latency, then the MMU24 must be programmed to delay its TC output accordingly, see Figure 15.

AC ELECTRICAL CHARACTERISTICS

Figure 15. RHDSP24 Scheduler Mode Timing Diagram (Continued)

MMU24 to Memory to DSP-24 - Address to Data memory Latency = 2
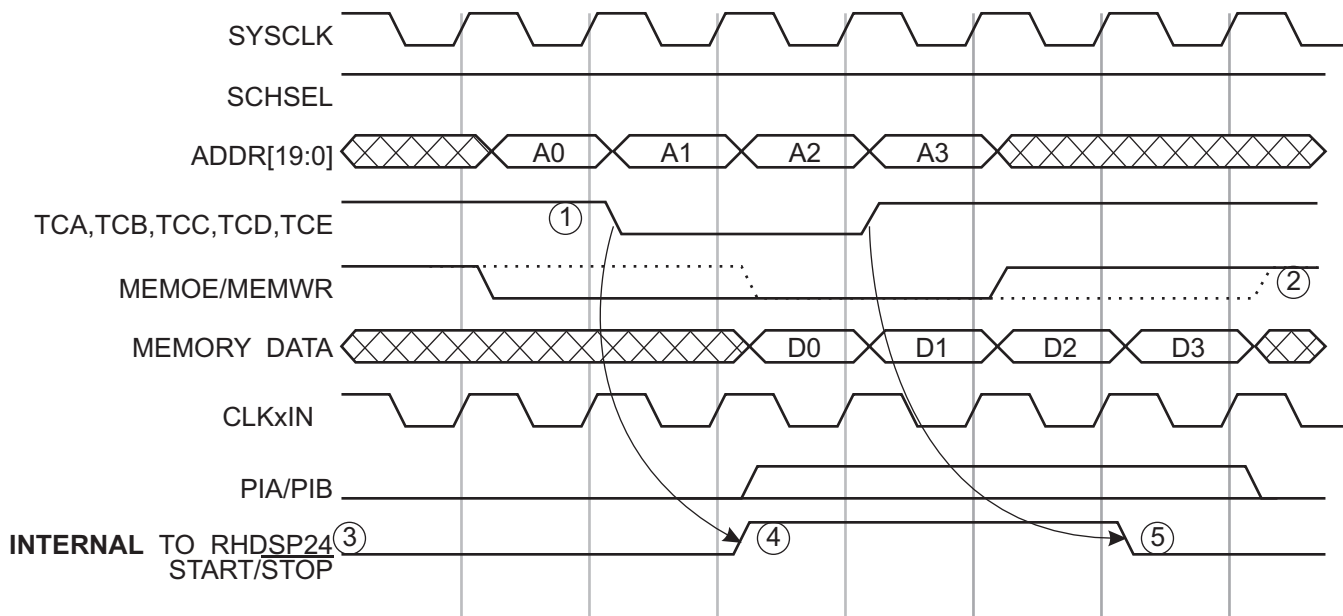
① TC delayed by one cycle. (SKEW Reg TC Bits 11:9 = 1, MODE Bit 3 = 0)
The TCx used for START/STOP generation is defined by MSB Bits 8:6 of the programed DataFlow.

② Default Showed. Depending on memory type, these signals may need to be skewed.
(SKEW Reg Bits 5:3 move MEMW and Bits 2:0 move MEMOE. 7= -1, 0-6 = 0-6)

③ Internal to DSP-24 the generated START/STOP signal needs to line up with incoming data first point, and go low during the incoming data's last point.

④ The Internal START/STOP rising edge equals Input TC falling edge delayed one clock cycle.

⑤ The Internal START/STOP falling edge equals Input TC rising edge delayed two clock cycles.

System Timing in the Scheduler Mode (Continued)

In addition to setting the START/ $\overline{\text{STOP}}$ timing, the MMU24 must also be programmed to skew the $\overline{\text{MEMOE}}$ and $\overline{\text{MEMWR}}$ signals to the SRAM. This frames the active data, according to the SRAM's specification.

DBGA PHYSICAL DEMINSIONS
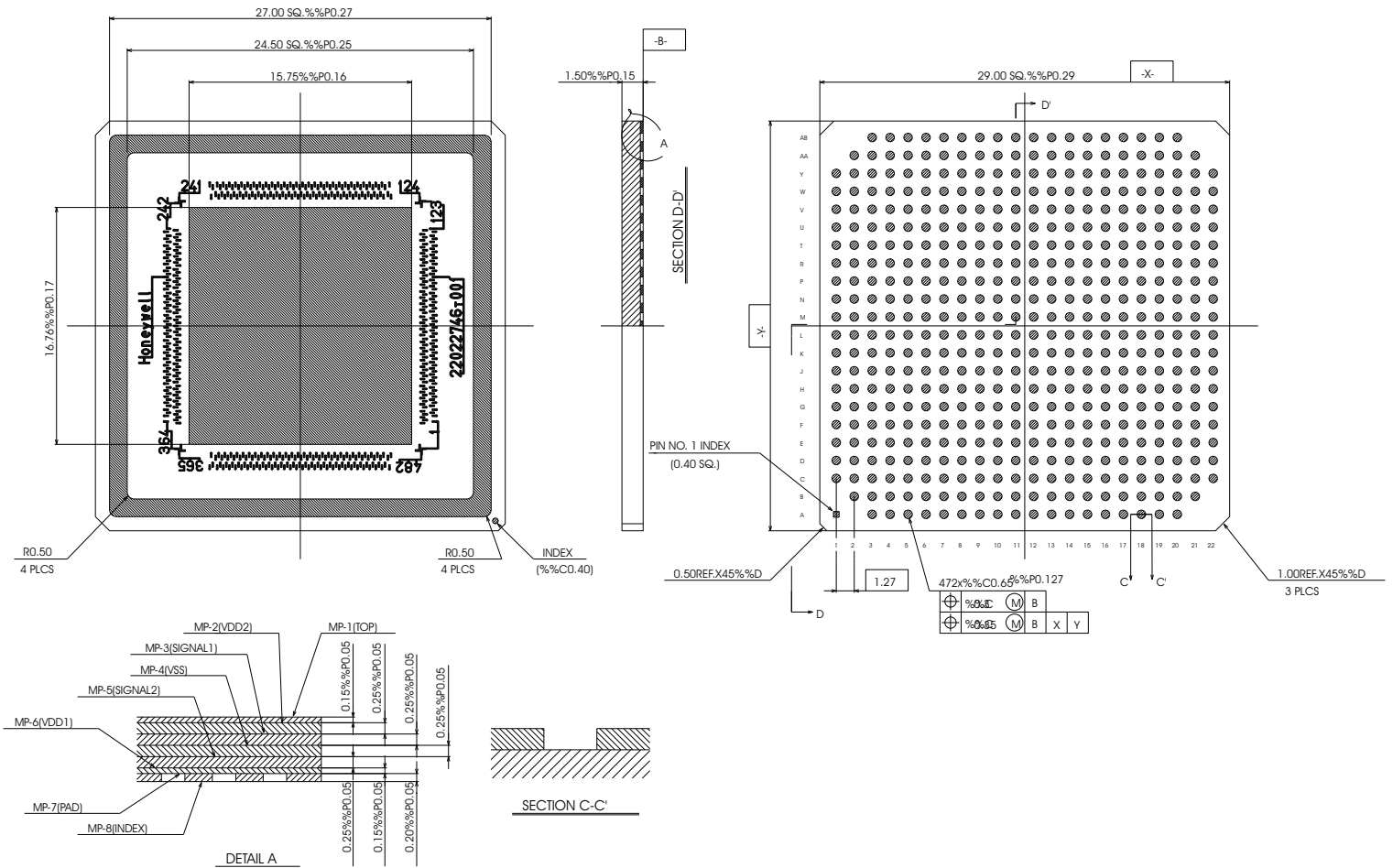
NOTES:

1. ALL METALLIZED AREA SHALL BE GOLD PLATED (ELECTROLESS)
   0.5 um%%P0.30um THK. OVER NICKEL PLATED 2.5 um MINIMUM THK.

2. CAMBER : 0.1 MAX.

3. SEAL AREA SHALL BE CONNECTED TO VSS.

4. DIE ATTACH AREA SHALL BE CONNECTED TO VSS.

5. HONEYWELL NAME, PART NUMBERS, WIREBOND TARGETS
   AND PAD NUMBERS CONNECTED TO VSS.

6. MATERIAL: KYOCERA A-440.

7. KYOCERA PART NUMBER: KD-N99K47.

8. ALL DIMENSIONS ARE IN MILLIMETERS.

9. TOLERANCES: %%P.20mm UNLESS OTHERWISE SEPCIFIED..

PIN LIST :

addr15_fc0	W18	Bi-Dir		er23	M17	Bi-Dir
addr14_fc1	W16	Bi-Dir		er22	M22	Bi-Dir
addr13_fc2	T16	Bi-Dir		er21	M15	Bi-Dir
addr12_fc3	AA20	Bi-Dir		er20	L15	Bi-Dir
addr11_fc4	U17	Bi-Dir		er19	L21	Bi-Dir
addr10_fc5	Y21	Bi-Dir		er18	L17	Bi-Dir
addr9_bfpclr	U19	Bi-Dir		er17	L22	Bi-Dir
addr8_df8	Y22	Bi-Dir		er16	L16	Bi-Dir
addr7_df7	T17	Bi-Dir		er15	L19	Bi-Dir
addr6_df6	V20	Bi-Dir		er14	L18	Bi-Dir
addr5_df5	V19	Bi-Dir		er13	K22	Bi-Dir
addr4_df4	W21	Bi-Dir		er12	K15	Bi-Dir
addr3_df3	T18	Bi-Dir		er11	L20	Bi-Dir
addr2_df2	T19	Bi-Dir		er10	K18	Bi-Dir
addr1_df1	W20	Bi-Dir		er9	K21	Bi-Dir
addr0_df0	W22	Bi-Dir		er8	J22	Bi-Dir
addren	V21	Input		er7	K17	Bi-Dir
mmustart	R17	Output		er6	K19	Bi-Dir
mmua0	R19	Output		er5	F18	Bi-Dir
mmurw	W19	Output		er4	J21	Bi-Dir
schdb7	V22	Input		er3	K16	Bi-Dir
schdb6	R16	Input		er2	K20	Bi-Dir
schdb5	R20	Input		er1	G18	Bi-Dir
schdb4	T20	Input		er0	F22	Bi-Dir
schdb3	U22	Input		clkein	J20	Input
schdb2	P17	Input		ei23	H21	Bi-Dir
schdb1	U20	Input		ei22	G21	Bi-Dir
schdb0	U21	Input		ei21	J16	Bi-Dir
mmutce_dzo	P19	Input		ei20	F21	Bi-Dir
mmutcd_yzi	T21	Input		ei19	H20	Bi-Dir
mmutcc_xzi	P16	Input		ei18	E22	Bi-Dir
mmutcb_xci	P20	Input		ei17	J15	Bi-Dir
mmutca_xswap	R21	Input		ei16	H19	Bi-Dir
schsel	T22	Input		ei15	D21	Bi-Dir
yswap	P15	Input		ei14	E21	Bi-Dir
yci	N20	Input		ei13	H17	Bi-Dir
ycr	P21	Input		ei12	D20	Bi-Dir
startstop	N19	Input		ei11	G20	Bi-Dir
sysclken	N21	Input		ei10	E19	Bi-Dir
sysclk	N15	Input		ei9	D22	Bi-Dir
eoe	M21	Input		ei8	H16	Bi-Dir
mmucse	M19	Output		ei7	G19	Bi-Dir

PIN LIST (cont):

ei6	F20	Bi-Dir	di15	A13	Bi-Dir
ei5	C22	Bi-Dir	di14	F12	Bi-Dir
ei4	G17	Bi-Dir	di13	D12	Bi-Dir
ei3	E20	Bi-Dir	di12	E12	Bi-Dir
ei2	F19	Bi-Dir	di11	A12	Bi-Dir
ei1	C21	Bi-Dir	di10	H12	Bi-Dir
ei0	C18	Bi-Dir	di9	H11	Bi-Dir
doe	B19	Input	di8	C11	Bi-Dir
mmucsd	G16	Output	di7	D11	Bi-Dir
dr23	C17	Bi-Dir	di6	A11	Bi-Dir
dr22	D16	Bi-Dir	di5	F11	Bi-Dir
dr21	A20	Bi-Dir	di4	B5	Bi-Dir
dr20	G15	Bi-Dir	di3	E11	Bi-Dir
dr19	C16	Bi-Dir	di2	A10	Bi-Dir
dr18	C19	Bi-Dir	di1	G11	Bi-Dir
dr17	B18	Bi-Dir	di0	B10	Bi-Dir
dr16	F15	Bi-Dir	bfpo0	E10	Output
dr15	B20	Bi-Dir	bfpo1	H8	Output
dr14	D17	Bi-Dir	bfpo2	A9	Output
dr13	C15	Bi-Dir	bfpo3	F10	Output
dr12	A19	Bi-Dir	bfpo4	C10	Output
dr11	H15	Bi-Dir	bfpo5	G7	Output
dr10	B17	Bi-Dir	syncout0	B9	Output
dr9	D18	Bi-Dir	syncout1	G10	Output
dr8	A18	Bi-Dir	dsfo0	B7	Output
dr7	G14	Bi-Dir	dsfo1	B4	Output
dr6	D14	Bi-Dir	dsfo2	B8	Output
dr5	E15	Bi-Dir	dsfo3	H10	Output
dr4	B16	Bi-Dir			
dr3	F14	Bi-Dir			
dr2	H14	Bi-Dir			
dr1	C14	Bi-Dir			
dr0	E16	Bi-Dir			
clkdin	B15	Input			
di23	H13	Bi-Dir			
di22	C13	Bi-Dir			
di21	D19	Bi-Dir			
di20	F16	Bi-Dir			
di19	B13	Bi-Dir			
di18	G12	Bi-Dir			
di17	B12	Bi-Dir			
di16	F13	Bi-Dir			

PIN LIST (cont):

coe	F9	Input		ci8	H3	Bi-Dir
mmucsc	D9	Output		ci7	J4	Bi-Dir
cr23	E6	Bi-Dir		ci6	K8	Bi-Dir
cr22	A6	Bi-Dir		ci5	F1	Bi-Dir
cr21	G9	Bi-Dir		ci4	D3	Bi-Dir
cr20	B3	Bi-Dir		ci3	J3	Bi-Dir
cr19	C4	Bi-Dir		ci2	K7	Bi-Dir
cr18	A5	Bi-Dir		ci1	G1	Bi-Dir
cr17	H9	Bi-Dir		ci0	K3	Bi-Dir
cr16	C8	Bi-Dir		boe	K4	Input
cr15	E7	Bi-Dir		mmucsb	K6	Output
cr14	D5	Bi-Dir		br23	J2	Bi-Dir
cr13	B6	Bi-Dir		br22	K1	Bi-Dir
cr12	F8	Bi-Dir		br21	K2	Bi-Dir
cr11	C7	Bi-Dir		br20	H2	Bi-Dir
cr10	C6	Bi-Dir		br19	L7	Bi-Dir
cr9	A4	Bi-Dir		br18	L2	Bi-Dir
cr8	G8	Bi-Dir		br17	F2	Bi-Dir
cr7	D7	Bi-Dir		br16	L4	Bi-Dir
cr6	D6	Bi-Dir		br15	L6	Bi-Dir
cr5	A3	Bi-Dir		br14	L1	Bi-Dir
cr4	F7	Bi-Dir		br13	L5	Bi-Dir
cr3	H7	Bi-Dir		br12	L3	Bi-Dir
cr2	D2	Bi-Dir		br11	L8	Bi-Dir
cr1	D4	Bi-Dir		br10	M8	Bi-Dir
cr0	F4	Bi-Dir		br9	M1	Bi-Dir
clkcin	E4	Input		br8	M6	Bi-Dir
ci23	E2	Bi-Dir		br7	M4	Bi-Dir
ci22	G5	Bi-Dir		br6	M7	Bi-Dir
ci21	C2	Bi-Dir		br5	N1	Bi-Dir
ci20	F6	Bi-Dir		br4	M5	Bi-Dir
ci19	J8	Bi-Dir		br3	M3	Bi-Dir
ci18	D1	Bi-Dir		br2	N8	Bi-Dir
ci17	F3	Bi-Dir		br1	N2	Bi-Dir
ci16	H4	Bi-Dir		br0	N5	Bi-Dir
ci15	J7	Bi-Dir		clkbin	N4	Input
ci14	E1	Bi-Dir		bi23	N3	Bi-Dir
ci13	H5	Bi-Dir		bi22	P2	Bi-Dir
ci12	G3	Bi-Dir		bi21	N6	Bi-Dir
ci11	J6	Bi-Dir		bi20	R2	Bi-Dir
ci10	G2	Bi-Dir		bi19	U2	Bi-Dir
ci9	E3	Bi-Dir		bi18	V2	Bi-Dir

PIN LIST (cont):

bi17	P8	Bi-Dir		ar1	T9	Bi-Dir
bi16	T2	Bi-Dir		ar0	AB6	Bi-Dir
bi15	P4	Bi-Dir		clkain	U9	Input
bi14	P3	Bi-Dir		ai23	R10	Bi-Dir
bi13	Y2	Bi-Dir		ai22	AB7	Bi-Dir
bi12	P6	Bi-Dir		ai21	AA5	Bi-Dir
bi11	U1	Bi-Dir		ai20	AA7	Bi-Dir
bi10	W3	Bi-Dir		ai19	T10	Bi-Dir
bi9	R3	Bi-Dir		ai18	AA9	Bi-Dir
bi8	P7	Bi-Dir		ai17	V7	Bi-Dir
bi7	V1	Bi-Dir		ai16	AA8	Bi-Dir
bi6	T5	Bi-Dir		ai15	U10	Bi-Dir
bi5	R4	Bi-Dir		ai14	AA10	Bi-Dir
bi4	R6	Bi-Dir		ai13	U7	Bi-Dir
bi3	W1	Bi-Dir		ai12	V8	Bi-Dir
bi2	Y1	Bi-Dir		ai11	Y10	Bi-Dir
bi1	U5	Bi-Dir		ai10	R11	Bi-Dir
bi0	T3	Bi-Dir		ai9	AB10	Bi-Dir
aoe	R7	Input		ai8	T7	Bi-Dir
mmucsa	W2	Output		ai7	Y11	Bi-Dir
ar23	U3	Bi-Dir		ai6	T11	Bi-Dir
ar22	T4	Bi-Dir		ai5	AB11	Bi-Dir
ar21	T6	Bi-Dir		ai4	V11	Bi-Dir
ar20	V3	Bi-Dir		ai3	W11	Bi-Dir
ar19	Y4	Bi-Dir		ai2	U11	Bi-Dir
ar18	R8	Bi-Dir		ai1	R12	Bi-Dir
ar17	AB3	Bi-Dir		ai0	AB12	Bi-Dir
ar16	W6	Bi-Dir		xsfi3	V12	Input
ar15	W7	Bi-Dir		xsfi2	AA12	Input
ar14	T8	Bi-Dir		xsfi1	U12	Input
ar13	AB4	Bi-Dir		xsfi0	AB13	Input
ar12	Y5	Bi-Dir		bfpi5	V13	Input
ar11	Y6	Bi-Dir		bfpi4	W12	Input
ar10	U8	Bi-Dir		bfpi3	T12	Input
ar9	AA6	Bi-Dir		bfpi2	AB14	Input
ar8	W5	Bi-Dir		bfpi1	V14	Input
ar7	Y7	Bi-Dir		bfpi0	V15	Input
ar6	AA3	Bi-Dir		alg0_xsfisel	Y13	Input
ar5	R9	Bi-Dir		alg1_ysfi0	R13	Input
ar4	AB5	Bi-Dir		alg2_ysfi1	AB17	Input
ar3	Y8	Bi-Dir		alg3_ysfi2	W13	Input
ar2	AA4	Bi-Dir		alg4_ysfi3	AA13	Input

PIN LIST (cont):

alg5_xcr	U13	Input
alg6_docr	AB18	Input
alg7_doci	Y14	Input
pib_enb	AA15	Input
jdo	T13	Output
jms	R14	Input
jck	AA16	Input
jdi	W14	Input
go1	AA18	Input
go0	T14	Input
syncin1	AB19	Input

syncin0	V16	Input
reset	AA17	Input
jrstn	Y18	Input
error	V17	Output
pout2	Y16	Output
pout1	T15	Output
pout0	AB20	Output
ssync1	Y17	Output
ssync0	Y19	Output
busy	U16	Output
pia_ena	AA19	Input

VDD (Connected to package power plane)

A8, A14, B11, B14, C3, C9, C12, C20, D8, D10, D15, E5, E9, E13, E18, H22, J1, J10, J13, J18, K5, K9, K11, K12, K14, L10, L13, L14, M9, M10, M13, N9, N11, N12, N14, N18, P5, P10, P13, P22, R1, U14, V5, V10, V18, W8, W10, W15, Y3, Y9, Y12, Y20, AA11, AA14, AB9, and AB15

VDD (Connected to Individual signal pins)

A16, G4, G6, G13, J19, M18, N7, N22, V6, and Y15

VSS (Connected to package power plane)

A7, A15, B2, B21, E8, E14, E17, F5, G22, H1, H18, J5, J9, J11, J12, J14, K10, K13, L9, L11, L12, M11, M12, M14, N10, N13, P9, P11, P12, P14, P18, R5, R22, T1, U15, U18, V4, V9, AA2, AA21, AB8, and AB16

VSS (Connected to Individual signal pins)

A17, C1, D13, H6, J17, M16, M20, N16, N17, P1, R15, R18, W9, W17,
W4, and U6

DSP
Architectures

Digital Signal Processor
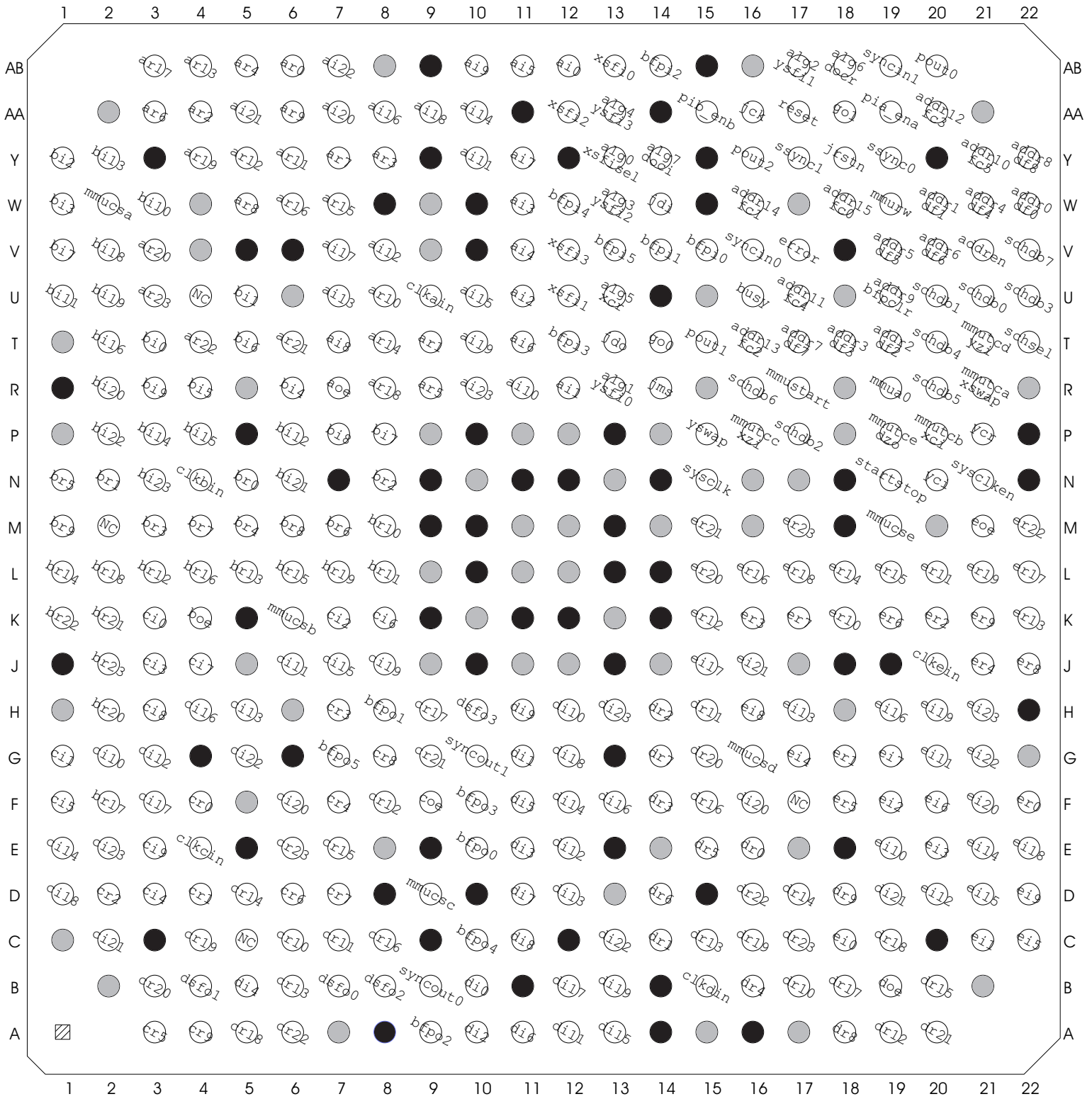
VSS

VDD

BOTTOM VIEW

TYPICAL RECURSIVE SYSTEM:
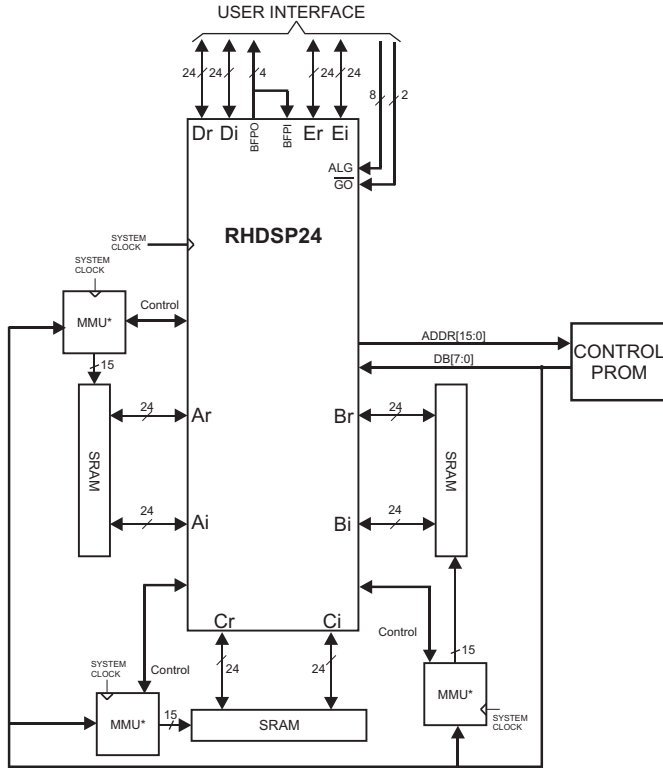
* There are three MMU's per RHtMMU24 or 1 MMU per MMU24

TYPICAL PARALLEL SYSTEM:
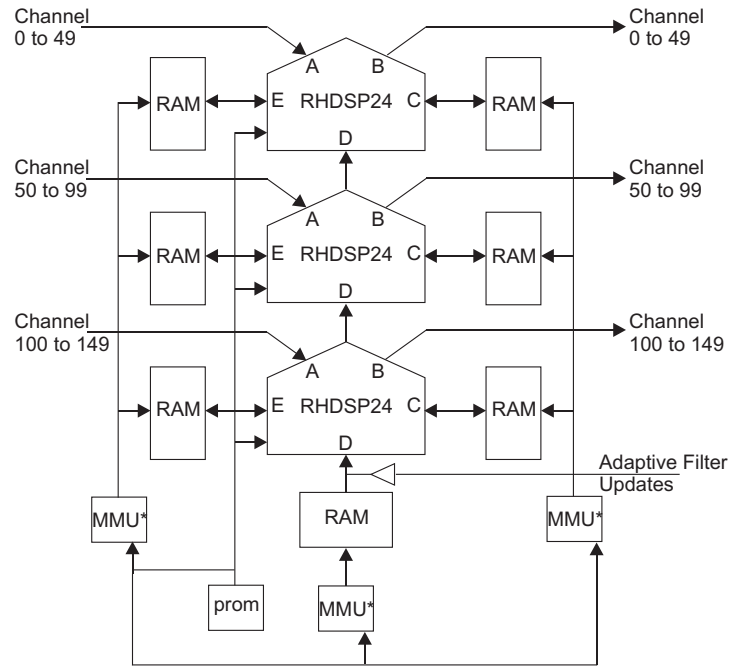
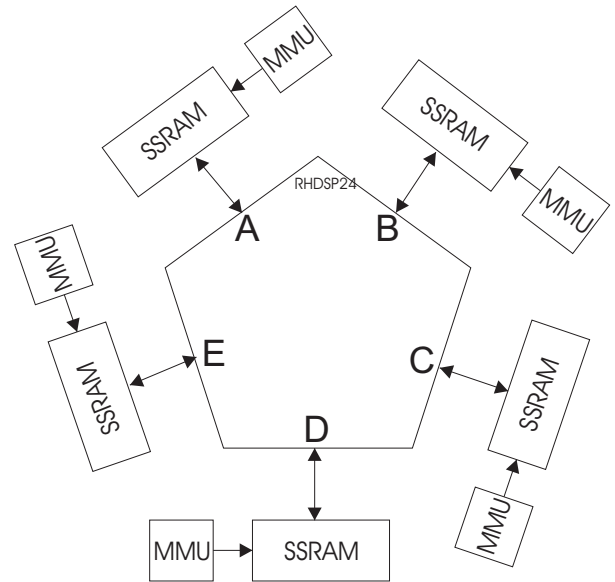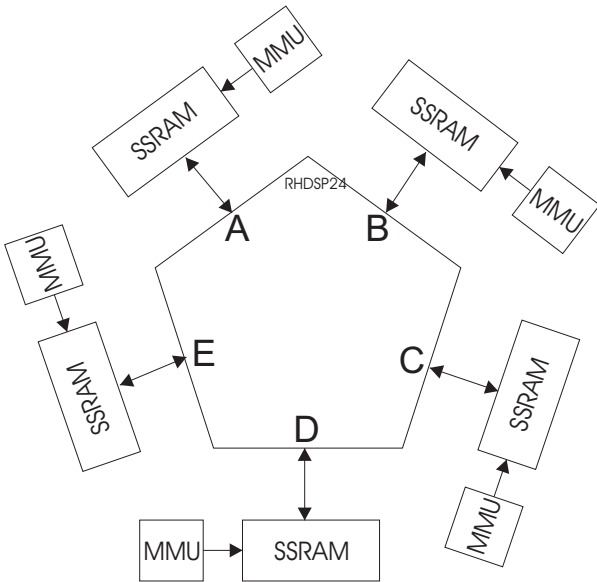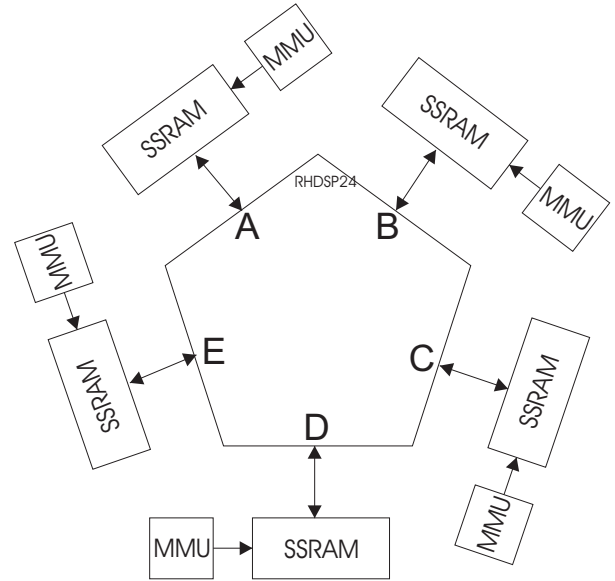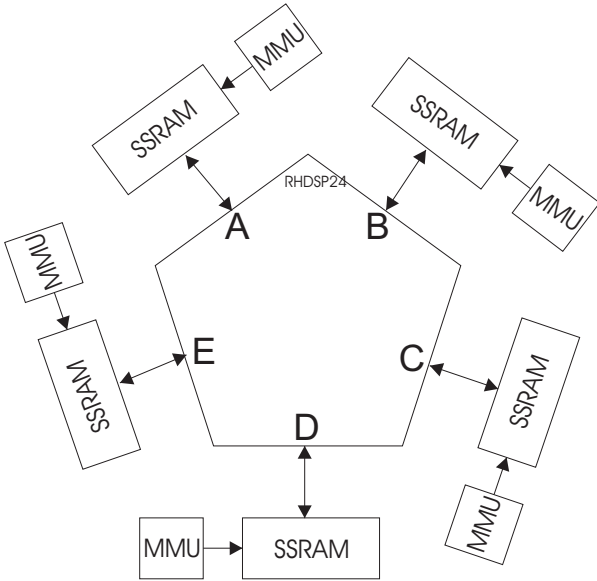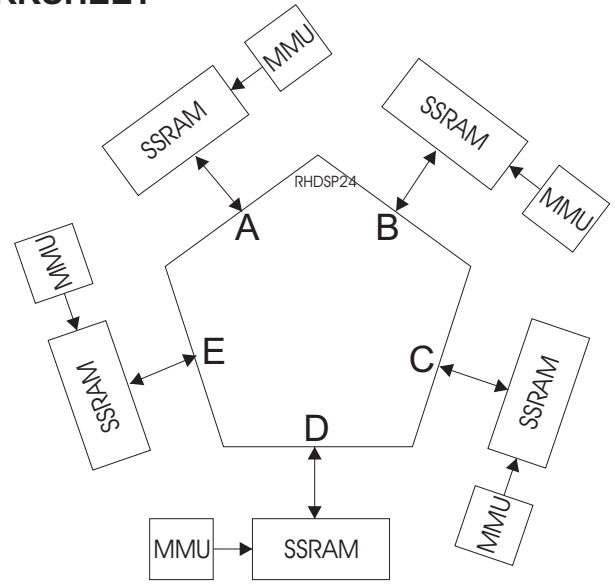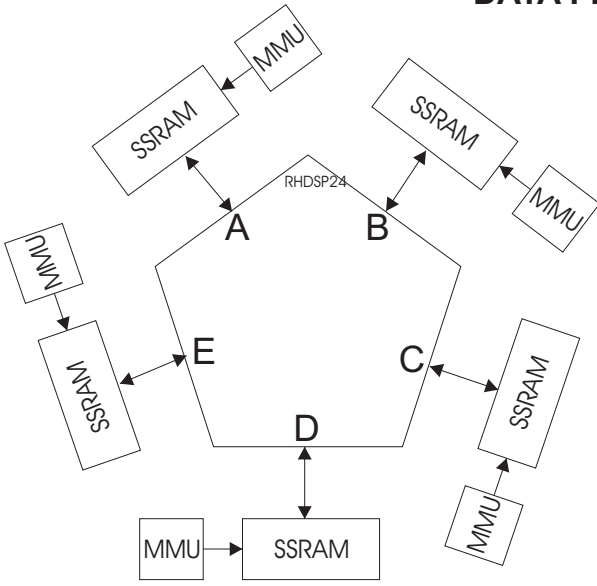* There are three MMU's per RHtMMU24 or 1 MMU per MMU24

The user supplied CONTROL PROM supplies the following:

- •INPUT ZERO FILLING

- •OUTPUT ZERO FILLING

- •INPUT ZERO PADDING

- •OUTPUT ZERO PADDING

- •INPUT DATA SHIFTING

- •INPUT DATA COMPLEMENTING

- •OUTPUT DATA COMPLEMENTING

- •A FUNCTION CODE PER PASS

- •A DATA FLOW CODE PER PASS

- •INITIALIZATION PROGRAMMING FOR UP TO FIVE MMU*'s

- •ADDRESS PATTERNS FOR EACH ONE OF UP TO FIVE MMU*'s

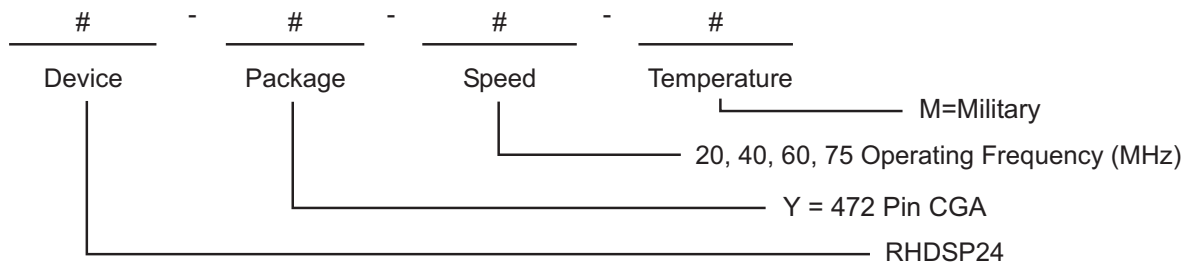- •SYSTEM START/STOP MANAGEMENT

- •SYSTEM SYNCHRONIZATION

* There are three MMU's per RHtMMU24 or 1 MMU per MMU24

DSP
Architectures

DATA FLOW WORKSHEET

ORDERING INFORMATION

```
  #    -    #    -    #    -    #
Device    Package    Speed    Temperature
                                    └───────── M=Military
                              └────── 20, 40, 60, 75 Operating Frequency (MHz)
                    └────── Y = 472 Pin CGA
          └────── RHDSP24
```

Example: RHDSP24-Y-75-M   (472 Pin CGA, 75 MHz Operating Frequency, Military Temperature)

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