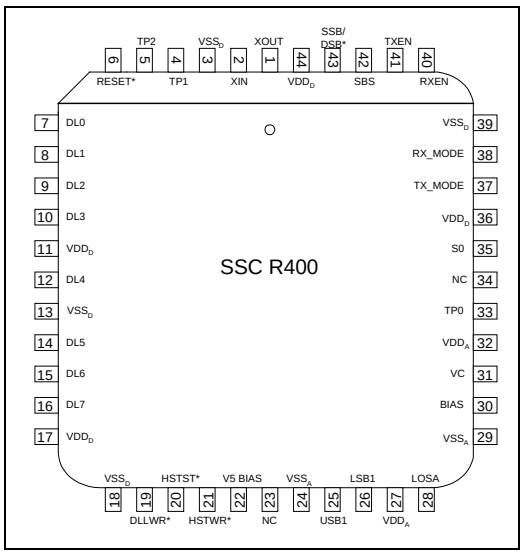
Features

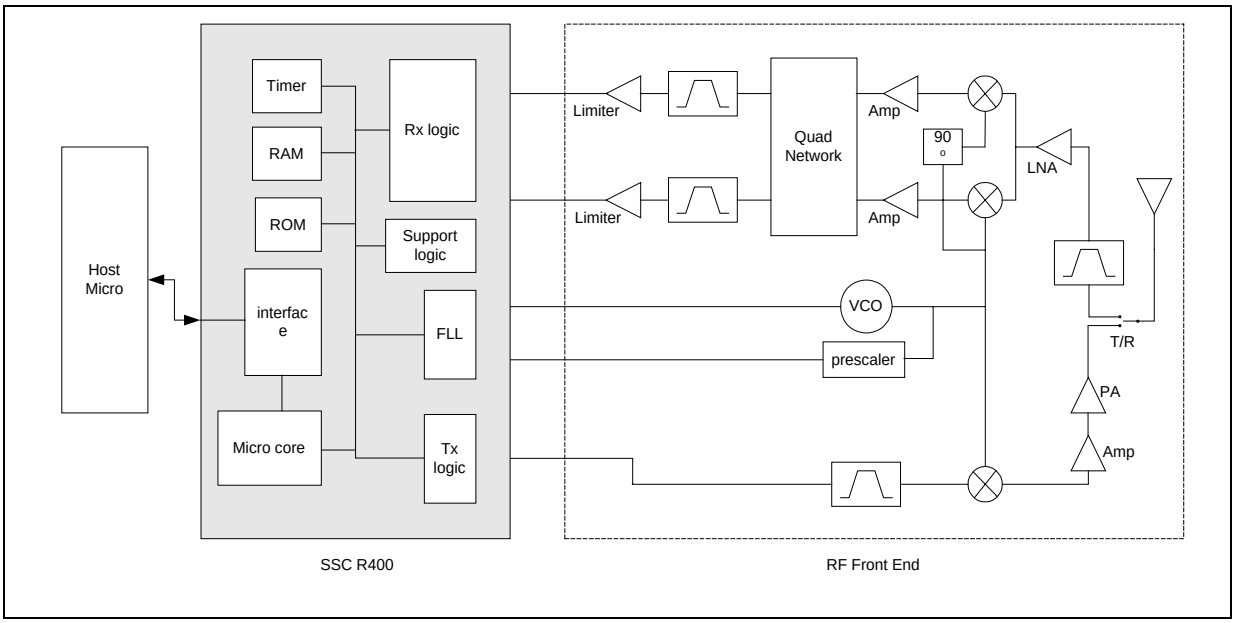
- Implements EIA-600 (CEBus®) Data Link Layer (DLL) and Radio Frequency (RF) Physical Layer
- Advanced Spread Spectrum Carrier™ Technology
- Standard CEBus channel and extended channel operation
- Integrated DLL processor and RF transceiver
- 8-bit parallel host processor interface
- Full 32-bit CEBus node address space supporting device, system and group codes
- Supports all Data Link services: addressed/unaddressed acknowledged /unacknowledged
- Data Link, Controller/Router, and Monitor Modes
- Minimal components required for RF communication interface
- 44 pin PLCC package



Introduction

The Intellon SSC R400 RF Network Interface Controller is a low cost implementation of the EIA CEBus Data Link Layer and Radio Frequency (RF) Physical Layer. The SSC R400 provides the Data Link Layer core controller and Spread Spectrum Carrier (SSC) baseband transceiver. A host controller is used with the SSC R400 to perform high-level application and network management functions.

SSC R400 Node Block Diagram



Overview

A typical RF node using the SSC R400 and an RF front end is illustrated in the block diagram on page 1. The Host Processor interprets commands and data for the User Application and provides the Application and Network layers of the CEBus communication protocol. Data Link and Physical layer services of the protocol are provided by the SSC R400 Network IC. The RF front end performs up conversion and down conversion of the baseband signal to and from the 902-928 MHz ISM band. Other functions performed are output signal amplification, transmit/receive switching, filtering, and base-band phase shifting.

Electrical Characteristics

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.3 to +4.0	V
V_{IN}	Input Voltage	V_{SS} - 0.3 to V_{DD} + 0.3	V
T_L	Lead temperature (soldering, 10 seconds)	300	°C
T_{STG}	Storage Temperature	-65 to +150	°C

Note: This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages.

Recommended Operating Conditions

Rating	Value
DC Supply Voltage	2.7 to 3.6 V DC
Crystal frequency	25.200 MHz, 50 PPM (over time & temperature)
Operating Temperature	-40° C to +85° C
Latchup	150 mA minimum, JEDEC JC-40.2

DC Characteristics

Conditions: V_{DD} = 2.7 to 3.6 V T= -40 to +85°C

Symbol	Parameter	Min	Typ	Max	Units
V_{OH}	Minimum High-level Output Voltage	2.4			V
V_{OL}	Maximum Low-level Output Voltage (1)			0.4	V
V_{IH}	Minimum High-level Input Voltage	2.0			V
V_{IL}	Maximum Low-level Input Voltage			0.8	V
I_{IL}	Maximum Input Leakage Current			+/-10	µA
I_{DD}	Power Supply Current		15	20	mA

Notes:

1. I_{OL} = 2 mA

AC Characteristics for Host Interface

The minimum detection time and the edge speed required by the internal processor on the SSC R400 are shown in Figure 1. This figure defines the parameters necessary for the SSC R400 to recognize individual signals. The timing relationship between signals is given in the signal timing section of this document.

Symbol	Parameter	Min	Max	Units	Notes
	Power on reset to host interface active		40	ms	
t_{RF}, t_{RR}	RESET* Rise and Fall	1	200	ns	1
t_{RL}	RESET* Low Time	1		µs	1, 2
t_{HWF}, t_{HWR}	HSTWR* Rise and Fall	1	200	ns	1, 3
t_{HSF},t_{HSR}	HSTST* Rise and Fall	1	200	ns	1, 3
t_{HSL}	HSTST* Low Time	1		µs	1, 2
t_{LWF}, t_{LWR}	DLLWR* Rise and Fall	1	150	ns	1
t_{LSF},t_{LSR}	DLLST* Rise and Fall	1	150	ns	1
t_{LSL}	DLLST* Low time	4	6	µs	1, 2

Notes:

1. Measured at V_{IH}=2.0V or V_{IL}=0.8V and 10msec maximum rise and fall time.
2. Measured with 50 pF load.
3. Measured at V_{OH}=2.4V or V_{OL}=0.4V.
4. Since the Data is read after the strobe and not clocked, the rise and fall time of the data is not critical as long as the data is stable during and after the strobe.

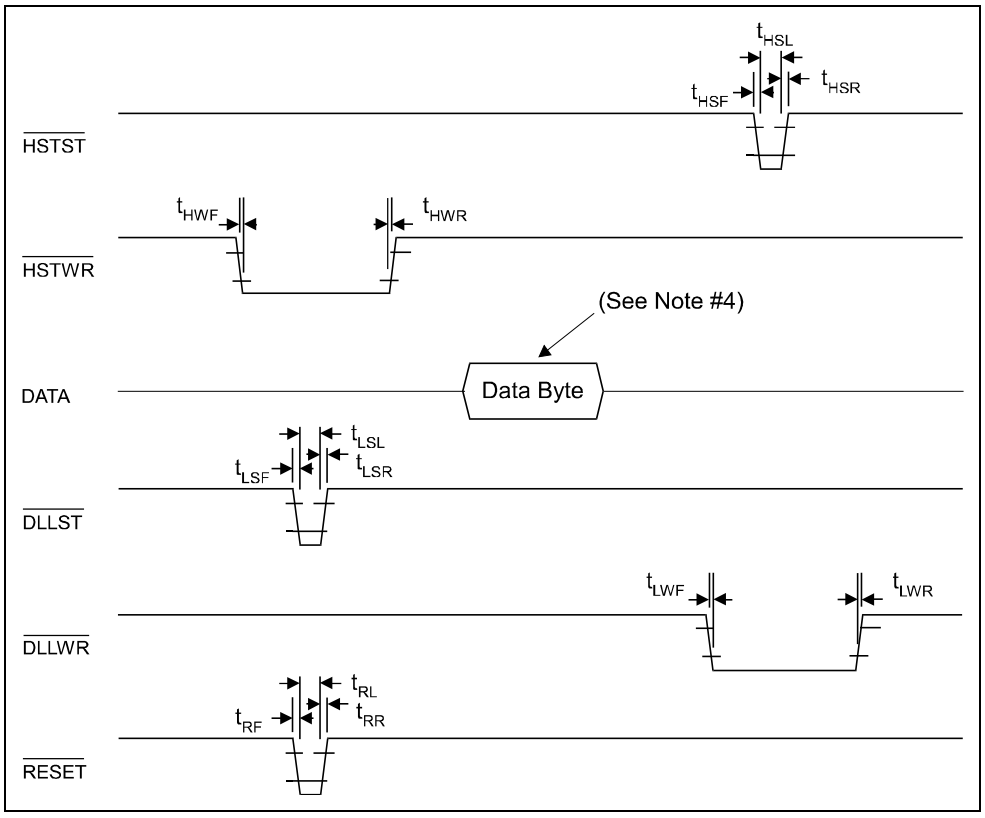


Figure 1. Interface Timing Parameters Diagram

Pin Assignments

Pin	Mnemonic	Name	Description
1	XOUT	Crystal output	Connected to external crystal to excite the internal oscillator and digital clock.
2	XIN	Crystal input	Connected to external crystal to excite the internal oscillator and digital clock.
3	VSS_D	Digital ground	Digital ground reference.
4	TP1		Reserved pin. Connect to VDD_D.
5	TP2		Reserved pin. Connect to VDD_D.
6	RESET*	Reset	Digital input. Internal processor reset invoked by either driving this pin low or by internal watchdog timer. Internally pulled up.
7	DL0	Data link 0	Digital bi-directional data bus 0 (LSB).
8	DL1	Data link 1	Digital bi-directional data bus 1.
9	DL2	Data link 2	Digital bi-directional data bus 2.
10	DL3	Data link 3	Digital bi-directional data bus 3.
11	VDD_D	Digital supply	2.7 VDC to 3.6 VDC analog supply voltage with respect to VSS_D.
12	DL4	Data link 4	Digital bi-directional data bus 4.
13	VSS_D	Digital ground	Digital ground reference.
14	DL5	Data link 5	Digital bi-directional data bus 5.
15	DL6	Data link 6	Digital bi-directional data bus 6.
16	DL7	Data link 7	Digital bi-directional data bus 7.
17	DLLST*	Data link strobe	Active low digital output. Control handshake pin used during transfer of data over the host interface data bus DL0…7.
18	VSS_D	Digital ground	Digital ground reference.
19	DLLWR*	Data link write	Active low digital output. Control handshake pin used during transfer of data over the host interface data bus DL0...7.
20	HSTST*	Host strobe	Active low digital input. Control handshake pin used for host write operation over the DL0…7 data bus.
21	HSTWR*	Host write	Active low digital input. Control handshake pin used for host write operation over the DL0…7 data bus.
22	V5BIAS	5 V bias	5.0 VDC bias input for 5V tolerant inputs.
23	NC	No connect	Reserved pin.
24	VSS_A	Analog ground	Analog ground reference.
25	USBI	Upper SB input	Analog signal input.
26	LSBI	Lower SB input	Analog signal input.
27	VDD_A		2.7 VDC to 3.6 VDC analog supply voltage with respect to VSS_A.
28	LOSA	LO sample	Analog signal input driven from the VCO to allow the frequency-locking loop to maintain the desired frequency. This is usually derived from a prescaler.
29	VSS_A	Analog ground	Analog ground reference.
30	BIAS	Analog bias	External resistor connection to set IC bias current.
31	VC	VCO control	Analog signal output providing digital feedback signal to adjust the center frequency of the VCO.
32	VDD_A	Analog supply	2.7 VDC to 3.6 VDC analog supply voltage with respect to VSS_A.
33	TP0	Test pin 0	Reserved pin. Connect to VDD_D.
34	NC	No connect	Reserved pin.
35	SO	Signal output	Digital baseband signal output. This signal must be gated on and off by TXEN. This is most often accomplished using an AND gate.
36	VDD_D	Digital supply	2.7 VDC to 3.6 VDC digital supply voltage with respect to VSS_D.
37	TX_MODE	TX mode	Digital output enabling a transmit operation from the baseband IC to the RF circuitry.
38	RX_MODE	RX mode	Digital output enabling a receive operation from the baseband IC to the RF circuitry.
39	VSS_D	Digital ground	Digital ground reference.
40	RXEN	RX enable	Digital output to control the external RFPA and T/R switch. Complement of TXEN.
41	TXEN	TX enable	Digital output to control the external RFPA and T/R switch.
42	SBS	Sideband select	Digital signal output. Enables upper or lower sideband transmission.
43	SSB/DSB*	Single/double sideband	Digital signal output. Enables single or double sideband radio transmission.
44	VDD_D	Digital supply	2.7 VDC to 3.6 VDC supply voltage with respect to VSS_D.

Functional Description

Extended Channels

A user selectable extended channel mode is included in the SSC R400. In this mode the radio will be capable of transmitting or receiving on three different carrier frequencies. The frequency spectrum diagram shown in Figure 2 defines the three channels. Channel B is the standard CEBus channel centered around 915 MHz. Channels A and C represent the extended channels centered around 911.5 MHz and 918.5 MHz respectively. Each channel contains two sidebands, an upper sideband and a lower sideband each 2.1 MHz wide. Guardband spacing between all channels is 1.4 MHz. Extended channels can be used to increase aggregate network bandwidth or improve reliability by dramatically increasing frequency diversity.

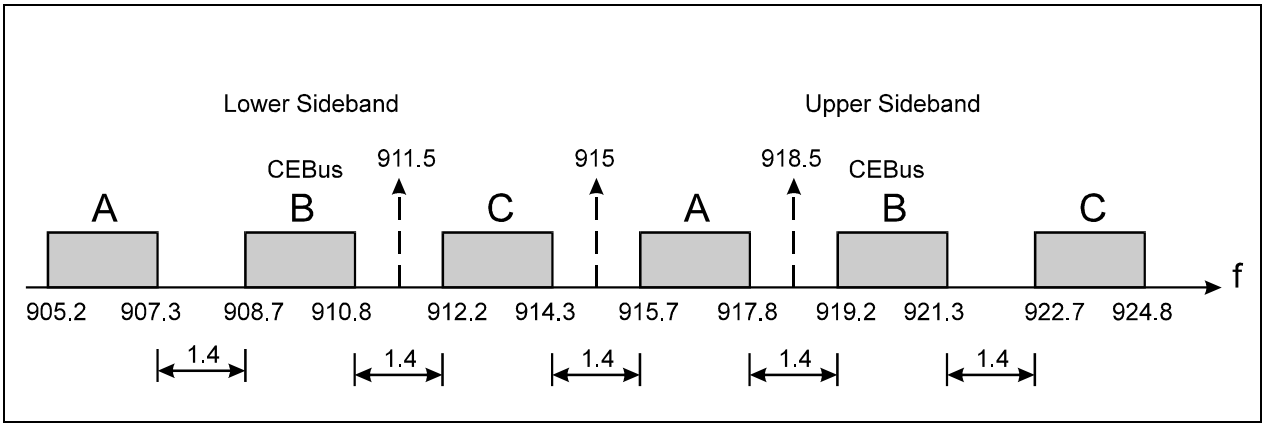


Figure 2. RF Frequency Spectrum

Communication Techniques

The SSC R400 supports three communication techniques. Each communication technique is selected by the values in the *Node_Control* structure. The host provides the SSC R400 with the needed information in the form of host commands. See the sections Host Commands and Data Structures later in this document. The default condition is CEBus operation. The host can select particular communication channels to transmit or receive on or it can enable the SSC R400 to automatically select communication channels using the built-in R400 algorithms. When enabled, the SSC R400 transmit-algorithm uses a simple round-robin method to select the next transmit channels. More sophisticated host algorithms may also be used.

The transceiver supports three communication techniques:

1. CEBus method – When using the CEBus method, the VCO remains stationary at 915 MHz. All communications then occur on the CEBus (channel B) frequencies.
2. Frequency hopping method – When using the frequency hopping method, the VCO frequency hops among 911.5 MHz, 915 MHz, and 918.5 MHz. To configure the SSC R400 to use automatic frequency hopping algorithm, the host processor must enable the *Transmit_Hop* and *Receive_Hop* bit fields in the *Node_Control* structure.
3. Fixed Channel method – When using the fixed channel method, the VCO remains stationary at one frequency, at either 911.5 MHz (channel A) or 918.5 MHz (channel C). To configure the SSC R400 for fixed channel mode, the host processor must disable the *Transmit_Hop* and *Receive_Hop* bit fields in the *Node_Control* structure. It must also set up the *Channel_Select* bit field in the *Node_Control* structure. See the Data Structures section later in this document.

Sideband Selection

The SSC R400 can be configured to transmit and receive double-sideband or single-sideband. In double-sideband mode, the SSC R400 uses a dual correlator that allows for the reception of both sidebands simultaneously. Based on the correlation value, the SSC R400 then decides which one of the sidebands to use. This decision is made each UST (100 μs). Consequently, the receiver can switch between sidebands at a very high rate to build the incoming packet. This sideband diversity, coupled with extended channel operation, enables the development of robust communication systems. The power up default of the SSC R400 is double-sideband operation.

In single-sideband mode, the sideband use is selectable as upper or lower. To select single-sideband operation, the host processor must enable the *Transmit_Single_Sideband* and *Receive_Single_Sideband* bit fields in the *Node_Control* structure. Once single-sideband is selected, the processor must configure the SSC R400 to use the upper or lower sideband. This is done by setting up the *Sideband_Select* bit field in the *Node_Control* structure. See the Data Structures section later in this document.

- Single/Double Sideband Select (SSB/DSB*) pin - This is a digital output. For radios with hardware that supports transmission of either single or double sideband, this control signal can be used to switch between these operating modes. Single sideband transmitters are commonly used to reduce power consumption. Therefore, the added circuitry to allow switching between modes is not added. In which case, the SSB/DSB* control pin is not used.
- Sideband Select (SBS) pin - This is a digital output. This pin is used to select either the lower or upper sideband for reception or transmission. If the hardware supports switching between sidebands, this control line can be connected to both the receiver and transmitter sideband selection switches.

Calibration

There are two calibration states: power-up calibration state and running calibration state. On initial power-up, all 3 channels are calibrated 3 times each. In the running Calibration State, each channel is re-calibrated once every two seconds to compensate for frequency drift in the VCO. Calibration of the frequency-lock loop (FLL) to an accuracy of ± 100 kHz is required for proper operation. If the FLL cannot be calibrated, a physical layer failure is reported via the bit field Phy_Layer_Fail_Status in the *DLL_Rc_Link_Status* data structure. Once calibration fails, the R400 will disable its transmitter. The transmitter will remain disabled until a hardware reset occurs or a host reset command is issued.

Power Management

In power management mode the host may power down the SSC R400 and the RF front end to conserve power. When the host powers up the SSC R400, it should also power up the VCO, prescaler, and VCO buffers to allow these circuits to stabilize while the SSC R400 is starting. The other components of the RF front end may be powered up using the signals from the SSC R400 as described below.

The SSC R400 contains signals that are used to control the activity of different sections of the RF front end. These signals allow the conservation of energy by only powering the circuitry needed for the function to be performed. The SSC R400 supplies four signals that control the RF circuitry; they are TX_Mode, RX_Mode, RXEN and TXEN.

TX_Mode - TX_Mode is a digital output. When TX_Mode is asserted the transceiver is in transmit mode and the transmitter circuits are enabled. The circuits that should be enabled are the upconvert mixers and the transmit buffer.

RX_Mode - RX_Mode is a digital output. When RX_Mode is asserted the transceiver is in receive mode and the receive circuits are enabled. The circuits that should be enabled are the LNA, downconvert mixers, baseband buffers and the limiting amplifiers. During the channel contention phase of a packet both TX_Mode and RX_Mode will be asserted.

RXEN - RXEN is a digital output. It is the logical compliment of TXEN. This signal is used to control the transmit/receive switch. This signal is very dynamic and must change states during the channel contention phase of the packet transmission in less than a microsecond.

TXEN - TXEN is a digital output. It is the logical compliment of RXEN. This signal is used to control the transmit/receive switch, the power amplifier and the local oscillator. This signal is very dynamic and must change states during the channel contention phase of the packet transmission in less than a microsecond.

RF Interface Signals

Signal Output (SO) - This is a digital output. This pin is the TX baseband output from the SSC R400 to the external carrier modulator. The signal ranges from 4.2 to 6.3 MHz. The signal level from the SSC R400 is 3 V logic level into 1kΩ load. The minimum load is 400 ohms. This signal usually passes through a pre-modulation filter before going to the modulator. This filter is used to shape the spectrum and reduce the signal level to provide proper shape and level to the modulator.

LO Signal (LOSA) – This is an analog input that provides the feedback necessary for the frequency locked loop (FLL). The range of this signal should be 14.06 to 14.53 MHz as the VCO tunes from 900 to 930 MHz. This is a divide by 64 prescaler signal. The signal from the prescaler should be 400 to 100 mV peak-to-peak AC coupled with no more than 15 pF stray capacitance.

VCO Control (VC) - This is an analog output used to precisely control the frequency of the external voltage controlled oscillator (VCO), which provides the receive local oscillator and the transmitter carrier generation function. The signal is driven by a digital-to-analog converter inside the R400. The VC signal will increase from 0 V to VDD_D-0.2V as the LOSA signal increases from 14.06 MHz to 14.53 MHz respectively.

Upper Sideband Input (USBI) - This signal is the upper sideband after down conversion to baseband. This signal is typically driven from a limiter. The signal level from the limiter should be between 100 and 400 mV peak-to-peak. The stray capacitance should not exceed 15 pF.

Lower Sideband Input (LSBI) - This signal is the lower sideband after down conversion to baseband. This signal is typically driven from a limiter. The signal level from the limiter should be between 100 and 400 mV peak-to-peak. The stray capacitance should not exceed 15 pF.

Frequency Locked Loop (FLL) Operation

The FLL consist of the following functional blocks:

- Voltage Controlled Oscillator.
- Prescaler, typically a divide by 64.
- Calibration and Control Logic.
- High Speed DAC to generate the required VCO turning voltage.

Voltage Controlled Oscillator - The VCO is the heart of the FLL. It provides the carrier signal for the transmitter and the local oscillator function for the receiver. The VCO characteristics are enumerated below:

1. The nominal tuning voltage range should be 0 to +3 Vdc.
2. The average tuning sensitivity should be 13 MHz/Volt.
3. The tuning sense should be positive. That is, the VCO frequency should increase as the tuning voltage is made more positive.
4. Tuning linearity should be within ±500 kHz of the best-fit straight line across the frequency range.
5. The tuning curve should maintain consistent shape and slope over the operational temperature range of -40 to +85 °C. The VCO must exhibit less than 6 MHz frequency shift form -40 to +85 °C.
6. The VCO frequency must remain stable with changes in the power supply voltage. The VCO must shift less than 2 MHz for changes between 2.7 to 3.6 volts.
7. The output frequency must have a drift rate less than 1 kHz/s under all conditions for the FLL to maintain the required accuracy between calibration cycles.
8. The output frequency must shift less than 25 kHz as the load changes from transmit mode to receive mode.
9. The complete frequency locked loop must slew 7 MHz and settle in less than 2µs. The VCO delay contribution should be a small portion of the 2µs, such as 200 ns.
10. The start-up and settling time should be less than 10 ms.

A commercially available VCO that meets these requirements with proper supply voltage regulation and output buffering is made by Z-Communications Inc., model D915ME01.

Prescaler - This is typically a divide by 64 IC which reduces the frequency for use by the SSC R400.

Calibration and Control - The VCO is calibrated on power-up by applying known tuning voltages and counting the resulting VCO frequency. During extended operation the VCO frequency error is monitored and used to adjust the DAC values. In this manner, long term drift and variations in VCO frequency are managed.

Digital-to Analog Converter - The DAC converter provides the tuning voltage for the VCO. This voltage is adjusted by the calibration routine internal to the SSC R400.

Operating Modes

The SSC R400 can be configured to one of the following three operating modes:

Data Link Mode	The SSC R400 Data Link (DLL) Mode provides CEBus Data Link Layer functionality for general communications systems.
Controller/Router Mode	The SSC R400 Controller/Router (CON) mode allows a host to support controller and router functionality.
Monitor Mode	The SSC R400 Monitor Mode provides capability to capture all traffic on the communication channel and only implements simple, UNACK_DATA services for transmission.

Detailed descriptions of SSC R400 operating modes are presented in the following sections.

Data Link (DLL) Mode

The DLL mode supports the standard CEBus Data Link Layer functionality at the Logical Link Sublayer. Most DLL mode functions directly map to the primitives specified in the CEBus Logical Link Sublayer specification. Detailed control and status information is also provided. The SSC R400 supports all four Data Link services (Unacknowledged, Acknowledged, Addressed Unacknowledged and Addressed Acknowledged services.) The DLL mode is selected by writing a value of 00 to the *Service_Level* field of *Mode_Control* byte in the *Layer_Config_Info* structure. See the section Data Structures later in this document.

Table 1. EIA-600 Device Functionality

EIA-600 Data Link Layer Function Description	SSC R400 Implementation
Transmit and receive all of the Data Link Layer packet types: ACK_DATA, UNACK_DATA, ADRACK_DATA and ADRUNACK_DATA.	One receive and one transmit address sequence number association is maintained.
Maintain and supply system and node addresses and layer system management parameters as requested from a higher layer.	Address and layer management parameters are volatile. Restoration following power loss is the responsibility of the attached host processor.
Recognize own system and node addresses and the broadcast address (destination system and node addresses = 0x0000, or destination system address = own system address and destination node address = 0x0000).	Fully implemented.
Recognize group addresses.	One group address is supported.

Receive Packet Procedure in DLL Mode

The following information assumes a valid correctly addressed packet has been received. The various packet receive conditions are given below. References to Rc_Dest_Address and Rc_Source_Address below refer to the respective four bytes comprising the Rc_Dest_Device_Address and Rc_Dest_House_Code, and the Rc_Source_Device_Address and Rc_Source_House_Code.

Host Interaction for Packet Reception in DLL Mode

Packet acceptance is posted for the host processor by using the *Rc_Attn* and *Rc_Except* flags in the Interface_*Flags* byte. The host uses the *Interface_Flags* to determine what action to take to service the SSC R400. When *Rc_Attn* flag is TRUE, the SSC R400 generates a host processor interface attention signal to asynchronously alert the host that service is required for a received packet. *Rc_Attn* is set to TRUE for all received packets accepted and not discarded due to refusal, overrun or duplicate receipt. The *Rc_Except* flag is also set if an ACK_DATA or ADRACK_DATA packet was refused, an UNACK_DATA or ADRUNACK_DATA packet overrun occurred, or if the current receive packet has a different source and/or destination address than the previous receive packet. *DLL_Rc_Link_Status* data structure may be accessed to determine the cause of the *Rc_Except* flag assertion.

A packet that is accepted and not discarded as a duplicate will cause the buffered *Receive_Header_Info* structure (Control field, Destination address and Source address) to be updated from the corresponding fields of the current *Receive_Header_Info* structure. If no packet is pending, that is, all packets have been read by the host, then the *Receive_NPDU_Field* structure is updated to complete the reception of the packet.

Whether or not discarded as a duplicate, an accepted ADRACK_DATA/ACK_DATA packet results in the SSC R400 sending an ADRIACK/IACK acknowledgment.

Packet Acceptance or Refusal

The following describes the conditions under which a valid correctly addressed packet is accepted or refused/rejected.

Packet Refusal and Overrun

The following describes the conditions under which a valid correctly addressed packet is refused. If the previously received packet has not yet been serviced by the host, any incoming ACK_DATA or ADRACK_DATA packet will be refused and *Rc_Refused* will be posted in *DLL_Rc_Link_Status* structure. Any incoming UNACK_DATA or ADRUNACK_DATA packet will cause an *Rc_Overrun* to be posted in *DLL_Rc_Link_Status* structure. A packet which produces a refuse or overrun condition does not affect the current receive sequence timer. An ADRACK_DATA/ACK_DATA packet that is refused results in an ADRIACK/FAILURE (busy) packet being returned to the source. The source then knows that delivery was unsuccessful and, if able, can retry the transmission.

Receive Sequence Timer Expired

If the receive sequence timer has expired, the packet will be accepted. If the received packet was ACK_DATA or UNACK_DATA, the receive sequence timer is left clear (zero). If the received packet was ADRACK_DATA or ADRUNACK_DATA, the receive sequence timer is reset to approximately 937 ms (1.25 times the Maximum Receive Time-out value of 750 ms).

Receiver Sequence Timer Not Expired

Same Source and Destination Address - If the receive sequence timer is not expired, but the received packet is ADRACK_DATA or ADRUNACK_DATA with a source and destination address that matches the previously received packet, the packet is accepted. The packet is then checked for a duplicate by using the received packet's sequence number. If the received packet sequence number matches the previously received sequence number, the received packet is a duplicate and is discarded. If discarded, the receive sequence timer is not modified. If the packet is not a duplicate and is accepted, the receive sequence timer is reset to 937 msecs.

Different Source or Destination Address - If the received packet was ACK_DATA or UNACK_DATA, and the receive sequence timer is not expired, the packet will be refused (ACK_DATA) or overrun will occur (UNACK_DATA). The appropriate flag (*Rc_Refused* or *Rc_Overrun*) will be posted. If the received packet is ADRACK_DATA or ADRUNACK_DATA and, if the received source address and/or the destination address does not match the previously received packet addresses, the packet will also be refused (ADRACK_DATA) or overrun will occur (ADRUNACK_DATA). The appropriate flag (*Rc_Refused* or *Rc_Overrun*) will be posted.

Transmit Packet Procedure in DLL Mode

The host processor is responsible for determining that no outstanding transmission is in progress before requesting a new packet transfer and transmission (see Posting Packet Transmission Status below). The SSC R400 supports only a single buffered transmit packet, so the previous transmission must be complete before a new packet can be transferred from the host.

Packet transmission can be accomplished by writing a complete packet with the PT command, or by using a combination of the WTH and WTI commands that transfer the *Transmit_Header_Info* structure (LPDU header) and *Transmit_NPDU_Field* structure (NPDU packet body) respectively.

The SSC R400 uses a transmit destination association sequence timer to insure that new packets are not sent to a device whose receive time-out may not yet have expired from a previous transfer from this node. Thus, packets sent to a new or different address may be delayed by the SSC R400 waiting for the expiration of the transmit sequence timer. Successive packets to the same destination address, however, will be sent without incurring possible transmit sequence time-out delays. The SSC R400 determines implicitly from the particular transmit commands used by the host processor if a packet with a (potentially) new destination address is to be transmitted. A command that writes the packet header containing the destination address (i.e., WTH or PT) is assumed to contain a change in the packet destination address. If, however, only the packet body (NPDU) is written by a command (i.e., WTI), then the packet must necessarily be to the same destination address using the same packet header as the last packet transmitted.

The use of WTI commands following an initial WTH or PT command are recommended, especially for ADRACK_DATA or ADRUNACK_DATA type packets. This will allow the maximum transfer rate when sending multiple packets to the same device by using multiple WTI commands following the initial WTH or PT command. ACK_DATA or UNACK_DATA type packets do not set the transmit sequence timers, but the previous transmit sequence timer must be expired before the R400 initiates the ACK_DATA or UNACK_DATA transmission.

The SSC R400 can process two packets; one that is currently transmitting and one in the buffer. A third packet cannot be sent to the SSC R400 until the transmit association timer for the first packet has expired.

Writing a Transmit Header

Packet *Transmit_Header_Info* is written by the host with the WTH command. Both the system and device source address values transferred in the *Transmit_Header_Info* should normally be 0xFFFF, resulting in the SSC R400 substituting its current system and device address as the header packet source address. The SSC R400 assumes that writing a header with the WTH command changes the destination address, therefore, actions are taken to preserve transmit time-outs. When the WTH command is executed the following steps occur:

1. If the transmit sequence timer is not expired, and the transmit service is ADR-type, the failure REMOTE_BUSY_XMIT_LIST status is returned, and the WTH command is ignored.
2. If the transmit sequence timer is expired, or the transmit service is non-ADR-type, completion and acceptance of the command is posted by setting the *Tr_Attn* flag and clearing the *Tr_Except* flag. The host may now transfer the *Transmit_NPDU_Field* and initiate packet transmission via the WTI command (see Transmitting a Packet with an Existing Header below).
3. The data is transferred to the SSC R400, source addresses are substituted as required, and control is returned to the host.

Transmitting a Packet with an Existing Header

To transmit a packet with a valid header previously transferred by a WTH or PT command, the *Transmit_NPDU_Field* is written by the host with the WTI command. The existing *Transmit_Header_Info* contents are used for the header of the packet to be transmitted. Subsequent packets addressed to the same device (i.e., using the same *Transmit_Header_Info*) only require a WTI command to send the new packet body (NPDU) portion of the subsequent packet. When the WTI command is executed the following steps occur:

1. If the transmit sequence timer is non-zero, and the transmit service is ADR-type, the failure REMOTE_BUSY_XMIT_LIST status is returned, and the WTI command is ignored.

2. If the transmit sequence timer is zero, or if the transmit service is non-ADR-type, the transmit header and packet body data are transferred to the SSC R400. Source address substitution is made as required; and control is returned to the host. If the packet is ADRACK_DATA or ADRUNACK_DATA, the *Tr_Seq_#* is incremented, and inserted in the transmit header. The *Tr_Seq_#* is a Data Link parameter and completely maintained by the SSC R400. If the SSC R400 automatically generates duplicate packets based on *CH_ACCESS_NUM* (for ADRUNACK_DATA packets), the same *Tr_Seq_#* value will be used for all subsequent copies of the same packet. Thus, if more than one packet is received at the destination, the duplicates can be eliminated.

3. The *Tr_Except* flag is set to indicate transmission in process.

4. When the packet transmission starts (i.e. the channel access protocol has been satisfied) and if the packet is an ADRACK_DATA or ADRUNACK_DATA type, the transmit sequence timer is loaded with 1125 ms. (1.5 times the Maximum Receive Time-out value of 750 ms.) On any subsequent retransmission of an ADR-type packet, due to ADRIACK (remote busy) or the CH_ACCESS_NUM parameter, the transmit sequence timer is reloaded with 1125 ms.

5. Upon transmission completion, *Tr_Attn* is asserted. *Tr_Except* will reflect the success or failure of the transmit process.

Transmit Complete Packet

To transmit a complete packet with a single command, the *Transmit_Header_Info* and *Transmit_NPDU_Field* are written consecutively by the host with the PT command.[1] When the PT command is executed the following steps occur:

1. The transmit header and packet body data are transferred to the SSC R400, source address substitution is made as required, and control is returned to the host. If the packet is a ADRACK_DATA or ADRUNACK_DATA, the *Tr_Seq_#* is incremented, and inserted in the transmit header. The *Tr_Seq_#* is a Data Link parameter and completely maintained by the SSC R400. If the SSC R400 automatically generates duplicate packets based on *CH_ACCESS_NUM* (for ADRUNACK_DATA packets), the same *Tr_Seq_#* value will be used for all subsequent copies of the same packet. Thus if more than one packet is received at the destination, the duplicates can be eliminated.

2. The *Tr_Except* flag is set to indicate transmission in process.

3. The R400 then waits for the transmit sequence timer to reach zero (the transmit sequence timer may have a residual value due to the previous transmission of an ADRACK_DATA or ADRUNACK_DATA packet), if it has not already done so. When the transmit sequence timer has expired, the transmission process begins.

4. When the packet transmission starts (i.e. the channel access protocol has been satisfied) and if the packet is an ADRACK_DATA or ADRUNACK_DATA type, the transmit sequence timer is loaded with 1125 ms. (1.5 times the Maximum Receive Time-out value of 750 ms.)

5. Upon transmission completion, *Tr_Attn* is asserted. *Tr_Except* will reflect the success or failure of the transmit process.

[1] A null length packet transfer with a PT or WTI command will retransmit the previous packet if transmission is not in process. Note that this is equivalent to transmitting a completely new packet (i.e., data link sequence numbers are incremented), and consequently should not be used for higher level CEBus (e.g. application) transmissions, as the new packet application level sequence information (i.e., Invoke ID number) is not changed.

ACK_DATA or UNACK_DATA Packet Transmission

Use of UNACK_DATA or ACK_DATA packet transmission is generally discouraged. The principal use of such packet types can be for broadcast messages in which sequencing is unimportant, e.g. “hailing”. UNACK_DATA and ACK_DATA packet transmissions do not set the transmit association timer, but transmission of these types still require the expiration of any outstanding transmit association timer value.

Posting Packet Transmission Status

Transmission in progress, completion, and success of a transmission are posted in the *Interface_Flags*, using the *Tr_Attn* and *Tr_Except* flags. The host can interrogate these flags to determine what action is necessary. The *Tr_Attn* flag is set TRUE when the transmit sequence timer becomes zero after a WTH command is executed, or when a packet transmission, including multiple accesses if specified, has completed after a PT or WTI command. The *Tr_Except* flag is always TRUE when a packet transmission is in progress following a PT or WTI command, or the transmit sequence timer has not expired subsequent to a WTH command. *Tr_Except* is also set whenever *Tr_Attn* is set TRUE and a transmit exception condition has occurred.

When the *Tr_Attn* flag indicates a packet transmission is complete, a new packet can immediately be sent to the same destination address by using a WTI command. However, transmitting a packet to a different (new) address may cause the SSC R400 to wait until the current transmit sequence timer has expired. The SSC R400 assumes that executing a WTH command changes the destination address. Consequently, execution of a WTH will set *Tr_Except* to TRUE and *Tr_Attn* to FALSE if the transmit sequence timer has not expired. When the transmit sequence timer expires, *Tr_Attn* will then be posted as TRUE. If the transmit sequence timer has already expired, *Tr_Attn* will be set TRUE immediately. Thus a WTI command should not be executed to send the new packet after a WTH command until *Tr_Attn* is set to TRUE.

If a packet write command (PT, WTI or WTH) is issued while the SSC R400 has an outstanding transmission in progress (*Tr_Attn* is FALSE and *Tr_Except* is TRUE), the command shall be ignored and an *Interface_Error* flag will be posted in the *Interface_Flags* byte.

Host Processor Busy Processing

Host Processor Busy - Indicates the host does not have resources available to service a new SSC R400 packet by setting the *Host_Busy* flag. If the *Host_Busy* flag is set TRUE by the host, the SSC R400 will not generate an attention sequence in response to a *Rc_Attn* or *Tr_Attn* condition. All ongoing Data Link operations continue as normal, including any packet refusals or overrun conditions that may occur during the period in which the host is busy. When the host leaves the busy condition and notifies the SSC R400 by setting the *Host_Busy* flag to FALSE, any pending receive or transmit conditions (*Rc_Attn* or *Tr_Attn*) will cause an immediate attention sequence to be generated.

The Upper Layer Busy - Indicates the host cannot process received packets at this time. No attention requests for received packets are generated (the first received packet is stored—subsequent received packets are refused/ignored). Other attention requests (including transmit complete) are generated normally. If an attention request is generated due to a non-"received packet" reason, but a packet has been received, it is the responsibility of the host to either process the received packet immediately or store the fact and process the received packet later. See description of Interface_Flags pertaining to processing all set flags.

Receive Association Limitation

One receive source association variable is provided by the SSC R400. This limits the attached host to receiving packets from only one source address and one destination address[2] within any given receive time-out period. ADRACK_DATA and ACK_DATA packets received from a different source address or going to a different destination address are given a ADRIACK/FAILURE (busy) if the receive sequence timer has not expired. ADRACK_DATA packets can subsequently (automatically) be retransmitted by the source, and so are not lost. However, the source will not know to retransmit the ADRUNACK_DATA and UNACK_DATA packets when the receive sequence timer or other busy condition is over. Consequently, ADRUNACK_DATA and UNACK_DATA packets may be lost. An occurrence of a potentially "lost" packet is noted by the SSC R400 posting the *Rc_Overrun* flag in *DLL_Rc_Link_Status* structure and by setting the *Rc_Except* flag in Interface_Flags to TRUE.

R400 Timing Constraints

In high traffic situations the real time communication constraints of servicing the SSC R400 must be considered. A worst case condition occurs when a second packet, addressed to the node, is being received before the previous packet has been read by the host. In order to prevent packet overrun, the SSC R400 must be serviced as soon and as quickly as possible. The time that the host microcontroller takes from reception of the attention sequence to copying up the received packet defines the service turn-around time. A typical calculation for the service turn-around time uses the minimum quiet time between packets, a "typical" preamble, an IEOF, and null address fields. Adding up these values yields a service turn-around time of approximately 4ms. This time should be adequate for CEBus compliance cases.

Controller/Router (CON) Mode

In this mode, a host may support communications to multiple devices simultaneously using the ADR-type transmit services. This simultaneous device support requires the maintenance of separate transmit/receive address associations for each device in the host process.

The CON Mode is selected by the value 11 in the *Service_Level* field of the *Mode_Control* byte in the *Layer_Config_Info* structure.

Packet Receive in CON Mode

Received packets are transferred to the host in a manner allowing the host to determine the addressing status of the packet and manage the sequence number and association timers for source and destination addresses. The notification of a received header is via *Rc_Except* in *Interface_Flags*. After receiving the header via the RRH command and processing the *Received_Header_Info* structure, and prior to the receipt of the CRC, the host will make a determination if the packet can be accepted, needs to be rejected or failed busy or should be ignored, based on the state of the received service, sequence number and receive association timer. The host must notify the SSC R400 controller via *Rcv_Disposition* in *Node_Control* structure as to the appropriate disposition of the packet such that appropriate action at the end of the packet can be performed, including sending an IACK packet. If a *Rcv_Disposition* response is not received in time, the packet will be ignored. If the packet has been accepted, information regarding the time of the receipt of the completed CRC (end of packet) will be passed to the host to assist in receive association timer management. The received NPDU is conveyed via the RRI (preferred) or PR command. The host is responsible for logging the received NPDU event for association timer purposes.

[2] Four different destination addresses exist in this DLL: 1) system address/node address, 2) system address/group address, 3) system address/broadcast node address, and 4) broadcast system address/broadcast node address.

Packet Transmit in CON Mode

The host sets up the address information for transmission, including the state of the sequence number, and manages the transmit association timers. Information regarding actual channel access (beginning of packet) will be passed to the host to assist in transmit association timer management via *Tx_Except*. Re-transmission (immediate and multiple ADR-type accesses) are handled by the SSC R400 controller, based on the transmit packet source address fields. Transmission completion is handled as described for the DLL mode.

WTH and WTI are not recommended commands for transmitting in this mode, because WTI will retransmit without changing the sequence number.

CON Timing Constraints

When a data packet is received, the host is responsible for determining the acceptance or rejection of the packet before the NPDU is completely received. The worst case occurs when the ID packet is received. In this case the NPDU contains only one byte. This yields 1.2 ms for the host to acknowledge the received packet after the attention sequence.

Monitor (MON) Mode

The MON Mode is selected by writing a value 10 in the *Service_Level* field of *Mode_Control* byte in the *Layer_Config_Info* structure.

Packet Receive in MON Mode

In this mode, the SSC R400 will receive and forward to the host all packets on the channel. A packet must have a legitimate start (IEOF), valid header, valid end (EOP) and valid CRC. No address or type checking is done and packets addressed to this device will not be acknowledged or sequence number checked. Further, all packets have the end of packet time (the time of the last UST of the CRC) logged, which is readable by the host. This time is posted in internal clock cycles (1.5625 usec per count) and is in a free-running 32-bit format.

Packet Transmit in MON Mode

Any packets transmitted in the MON mode will not be checked for type and will be transmitted as if they were UNACK_DATA packets. The time of the last UST of the transmitted packet is also logged so that all channel packet traffic timing is available to the host. If a packet type is transmitted that generates an acknowledge from the receiver, the acknowledgment will be logged and forwarded to the host just like any other packet received in the MON Mode. NOTE: Transmitting in MON mode is not recommended.

Timing Constraints

The host must service the received monitor packets before the next packet on the channel is received in order to avoid an overrun. Worst case this means that in the monitor mode, the host must respond to an attention sequence within about 1 millisecond and must be able to support the packet transfer protocol at or near the maximum rate (see the section Signal Timing). If the response time requirements cannot be met or the maximum transfer rate cannot be supported, received packets may be lost and/or overwritten.

Software Interface

The SSC R400 is designed to provide CEBus services to an attached host processor. The services provided allow a host processor to optimally implement a CEBus application, relying on the SSC R400 for real-time network processing. All SSC R400 system information (Node Addresses, etc.) is loaded by the host processor per the following description. Note that all downloaded information is volatile and must be reloaded in the event of a power failure.

Host Commands

The Host interface supports the commands given below. The data structures and actions of these Host commands are given in subsequent sections.

Table 2. Host Commands

Cmd Value (hex)	Cmd Code	Command Name	Use
00	FIE	Force Interface Error	Can be used to force interface error. Used internally for interface error indication.
01	RST	Reset	Host interface reset. Disables all functions and I/O except host interface. (Reset signal line is more reliable as it does not require that host interface be operational.) An LW command is necessary to initiate any activity subsequent to a reset.
02	LR	Layer Mgmt Read	Layer management read of Layer_Config_Info configuration information.
03	LW	Layer Mgmt Write	Layer management write of Layer_Config_Info configuration information, followed by initialization and enabling of functionality.
04	IR	Interface Read	Host read of Interface_Flags. These flags are generally sufficient to control states and transfers between host and SSC R400. Interface flags are cleared by the IR command.
05	CW	Control Write	Host write to Node_Control (Data Link control parameters).
06	SR	Status Read	Host read of Status_Info (transmit, receive and statistics status) that may be required as a result of host query of Interface_Flags. Status overflow flags read are cleared by the SR command.
07	--	Reserved	Reserved.
08	PR	Packet Receive	Host read of received CEBus_Packet. (Received IACK_type packets for transmitted packets can be read via the RRH command.) In Data Link mode accesses buffered Data Link header (Control field, Destination Address and Source Address) and NPDU field. In Monitor mode accesses non-buffered Data Link header and NPDU field.
09	PT	Packet Transmit	Host write of CEBus_Packet.
0A	RRI	Read Receive Information	Host read of buffered received packet NPDU_Field (Data Link Information).
0B	WTI	Write Transmit Invoke	Host write of transmit NPDU_Field (Data Link information).
0C	RRH	Read Receive Header	Host read of Data Link Receive_Header_Info from received packet (Control field, Destination Address, Source Address). Command accesses the unbuffered header and is primarily for diagnostic use (e.g. Monitor mode and reading IACK responses).
0D	WTH	Write Transmit Header	Host write of the Transmit_Header_Info for subsequent transmit packets.
0E-45	--	Reserved	Reserved
46	WRS-46	Write Register 46	Host write of DLL_Access_Control (Data Link communications access control parameters).
47-83	--	Reserved	Reserved
84	RRS-4	Read Register 4	Host read of DLL_Rc_Link_Status (receive status flags).
85-FF	--	Reserved	Reserved

Data Structures

The following data structures allow the SSC R400 to: be configured for network operations, control which features are active, buffer transmit and receive packets, and determine status and error conditions.

Table 3. Layer_Config_Info Structure

Byte	Name		Use	Reset State
0	Mode_Control		Defines operating mode.	
	Bits	**Field**	**Use**	
	0-1	Service_Level	00 - Data Link 01 - Reserved 10 - Monitor 11 - Controller/Router	00
	2	Enhanced Protocol	Enables use of host protocol enhancement which acknowledges end-of-command. 0 - Normal protocol 1 - Enhanced protocol	0
	3-6	Max_Restart	Maximum number of restarts allowed (x8) due to collisions and aborts in a transmission attempt.	0000
	7	Reserved	Reserved	0
1[3]	Group_Address_LSB / (Mon_Time_Log_LSB)		DLL mode: Group Address. MON mode: Contains time log of the end of last received packet - LSB. CON mode: Not used.	0x00
2[3]	Group_Address_MSB / (Mon_Time_Log_2LSB)		DLL mode: Group Address - MSB MON mode: 2nd LSB of time log value CON mode: Not used.	0x00
3[3]	Device_Address_LSB / (Mon_Time_Log_3LSB)		DLL mode: Device Address - LSB MON mode: 3rd LSB of time log value CON mode: Not used.	0x00
4[3]	Device_Address_MSB / (Mon_Time_Log_MSB)		DLL mode: Device Address - MSB MON mode: MSB of time log value CON mode: Not used.	0x00
5	System_Address_LSB		DLL mode: HC/Zone Address - LSB MON mode: HC/Zone Address - LSB CON mode: Not used.	0x00
6	System_Address_MSB		DLL mode: HC/Zone Address - MSB MON mode: HC/Zone Address - MSB CON mode: Not used.	0x00

[3] In the Monitor Mode, the group and device addresses hold the time stamp logged at the end of the last received or transmitted packet. The timer is a 32-bit number in units of microprocessor clock cycles (a period of ~1.86 hours).

Table 4. Interface_Flags Structure

Flag Name	Bit	Attn	Use	Reset State
IC_Reset	0	No	Indicates the SSC R400 is in a reset condition. An LW command is required to initialize and activate. 0 - Not reset 1 - Reset	1
Link_Status_Condition	1	Programmable	Indicates Link statistics counter register overflow or other condition occurred that merits host attention. Attention occurs only when the Link_Status_Enable flag is set. 0 - No overflow occurred 1 - Overflow occurred	0
Interface_Error	2	No	Indicates an error on the last attempted host command sequence. (Does not cause an attention as this may cause a “lock-up” on the interface.) 0 - No error 1 - Error detected	0
Physical_Layer_Failure	3	Yes	An error was detected in the physical layer. Read DLL_Rc_Link_Status to determine cause for failure. 0 - No error 1 - Failure occurred	0
Rc_Except	4	No/ Yes[4] (CON mode)	DLL mode: If Rc_Attn is asserted along with Rc_Except, a receive condition other than successful reception of a valid packet has occurred. CON mode: Indicates that a complete header has been received. 0 - No exception 1 - Exception occurred	0
Tr_Except	5	No/ Yes[4] (CON mode)	All modes: If Tr_Attn is asserted along with Tr_Except, a transmit condition other than a successful completion of the last packet has occurred. If Tr_Attn is not asserted, Tr_Except asserted indicates that a packet transmission is pending or in progress. CON mode: Indicates that the IEOF of a transmit attempt has been successfully transmitted to the medium. 0 - No exception 1 - Exception occurred	0
Tr_Attn	6	Yes	Indicates that a pending packet transmission is complete. If Tr_Except is also asserted, the Transmit Status must be read to determine the exceptional transmit condition. 0 - No completion 1 - Transmit completed	0
Rc_Attn	7	Yes	Indicates that a valid CEBus packet has been received. DLL mode: If Rc_Except is asserted, the Receive Status must be read to determine the receive condition. 0 - No receipt 1 - Packet received	0

[4] In the controller/router mode an attention sequence is generated when these flags are set. In DLL mode no attention sequence is generated by these flags.

Table 5. Node_Control Structure

Byte	Field	Bit	Use	Reset State
0	Link_Status_Enable	0	Enables the generation of an Attention sequence on the host interface when any link statistics counters or other non-transfer conclusion link status condition occurs. 0 - No attention generated 1 - Attention generated on overflow	0
	Upper_Layer_Busy	1	DLL mode: Indicates host cannot process received packets at this time. No attention requests for received packets are generated (the first received packet is stored—subsequent received packets are refused/ignored). Other attention requests (including transmit complete) are generated normally. If an attention request is generated due to a non-"received packet" reason, but a packet has been received, it is the responsibility of the host to either process the received packet immediately or store the fact and process the received packet later. See description of Interface_Flags pertaining to processing all set flags. 0 - All attentions generated 1 - No attention for received packets	0
	Abort_Transmission	2	Aborts current packet transmission (if not already completed). Abort occurs prior to channel access or after transmit complete (i.e. fragments will not be produced). 0 - No abort 1 - Abort the current transmission	0
	Host_Busy	3	Indicates host cannot service a packet at this time. Disables host interface attention requests. 0 - All attentions generated 1 - No attentions generated	0
	Reserved	4		0
	Rcv_Disposition	5-7	CON mode: Determines the response to a received packet. 000 - Ignore packet—no response 001 - Accept packet—generate proper IACK or ADR_IACK response 010 - Default Remote Busy—generate proper FAILURE or ADR_IACK response 011 – Default Remote Reject—generate proper FAILURE or ADR_IACK response 100 - Remote Reject Extended (Remote_Reject_Ext)--generate proper FAILURE or ADR_IACK response 101 - Remote Busy Receive List (Remote_Busy_Rcv_List)--generate proper FAILURE or ADR_IACK response 110 - Reserved 111 - Reserved	000
1	Rcv_ExtSvc_Accept	0	DLL mode: Determines whether packets with EXTENDED service class are accepted or ignored. 0 = Ignore extended packets 1 = Accept extended packets	0
	Rcv_SeqNo_Ignore	1	DLL and CON modes: Determines whether the sequence number in the received ADRIACK is compared with the transmitted packet's sequence number. 0 = Compare the sequence numbers 1 = Ignore the received sequence number	0
	Reserved	2-7	Reserved	00000
2	Reserved	0-2	Reserved	000
	Sideband_Select	3	Determines whether packets are transmitted or received on the lower or upper sideband if Transmit_Single_Sideband or Receive_Single_Sideband is active. 0 = Lower sideband 1 = Upper sideband	0
	Channel_Select	4-5	Determines which transmit channel is active if Transmit_Hop is inactive. Determines the fixed receive channel, when Receive_Hop is inactive. 00 = Channel A 01 = Channel B (CEBus compatible) 10 = Channel C 11 = Reserved	00

Byte	Field	Bit	Use	Reset State
	Transmit_Single_Sideband	6	Determines whether packets are transmitted on a single sideband or both sidebands. If single sideband is selected, Transmit_Sideband_Select determines the active sideband. 0 = Transmit on both sidebands 1 = Transmit on single sideband	0
	Transmit_Hop	7	Determines whether extended channel transmit hop mode is active. 0 = Inactive (transmit hopping disabled) 1 = Active	0
3	Reserved	0-2	Reserved	000
	Receive_Single_Sideband	3	Determines whether receive correlators on both sidebands are active or only a single sideband is active. If a single sideband is active, Receive_Sideband_Select determines the active sideband. 0 = Active (automatic sideband selection) 1 = Inactive (fixed single sideband)	0
	Receive_Hop	4	Determines whether extended channel receive hop mode is active. 0 = Inactive (receive hopping disabled) 1 = Active	0
	Reserved	5-7	Reserved	000

Table 6. Status_Info Structure

Byte	Name		Use	Reset State
0	Status_Flags		Contains various flags regarding transmit completion and statistics counter overflow conditions.	
	Bit	**Field**	**Use**	
	0-3	Tx_Status_Code	Contains the transmit completion status code: 0 - Success: Transmission of packet was successful. 1 - Remote_Busy: Tr FAIL ack—remote busy. Details in FAILURE/ADR_IACK packet information field in Receive Header Buffer. 2 - Remote_Reject/Other: Tr FAIL ack—remote reject or other. Destination cannot accept. Details in FAILURE/ADR_IACK packet information field in Receive Header Buffer. 3 - Excessive_Retries: Tr Aborted—No (ADR)IACK in Max_Retrans time. 4 - Excessive_Collisions: Tr Aborted—exceeded Max_Restart attempts. 5 - No_IACK: No IACK received in time expected. 6 - Bad_IACK: Bad IACK received—frag or bad CRC in expected IACK time. 7 - Wrong_IACK: Illegal type code or sequence number received for IACK type. 8 - Unknown 9 - Physical_Failure: Physical layer failure. A - Transmit_Aborted: Transmit aborted by host. B - Max_Retrans_Exceeded: No transmission in Max_Retrans time. C - Local_Busy_Xmit_List: Local transmit association timer has not expired. D - Reserved E - Reserved F - Reserved	0000
	4	Retry_Abort_Ovfl	Indicates transmit Retry Abort Counter Overflow. 0 - No overflow 1 - Overflow	0
	5	Backoff_Ovfl	Indicates transmit Backoff Counter Overflow. 0 - No overflow 1 - Overflow	0
	6	Bad_CRC_Ovfl	Indicates receive Bad CRC Counter Overflow 0 - No overflow 1 - Overflow	0
	7	Frag_Ovfl	Indicates receive Frag Counter Overflow 0 - No overflow 1 - Overflow	0

Byte	Name		Use	Reset State
1[5]	Rc_Frag_Counter		Contains the number of packet fragments received. To be counted as a fragment, an initial packet IEOF must have been received, followed by a packet fragment terminated with an EOP.	0
2	Rc_Bad_CRC_Counter		Contains the number of packets received with CRC errors.	0
3	Tr_Backoff_Counter		Contains the number of transmission attempts that backed off due to excessive contentions/collisions or abort deferrals	0
4	Tr_Retry_Counter		Contains the total number of retry ADRACK_DATA and ACK_DATA packets transmitted beyond the first attempts.	0
5	Device_ID		Contains device identifier and version control information.	
	Bit	**Field**	**Use**	
	0-3	Device_Type	Type of device: 0000 – CEThinx 0001 – SSC P400 0010 – SSC R400 0011-1111 – Reserved	
	4-7	Device_Version	Version of device	

Table 7. Transmit_Header_Info Structure

Field Name	Byte	Comments
Tr_Control_Field	0	The transmitted packet control field. (See DLL_Control_Field description)
Tr_Dest_Device_Code	1-2	The transmitted packet destination address. This address must be a legal device code (e.g., group, device, or broadcast address - “0”). The address field is stored least significant byte first.
Tr_Dest_House_Code	3-4	The transmitted packet destination house code. This house code must be a legal house codes (e.g., a system address, zone address, or universal house code - “0”). The destination house code is stored least significant byte first.
Tr_Source_Device_Code	5-6	The transmitted packet source device code is stored least significant byte first. If zero is sent, a null address will be transmitted. A value of 0xFFFF will cause the Tr_Source_Device_Code to be replaced with the Device_Address in the Layer_Config_Info structure and the Tr_Source_House_Code to be replaced with the System address in the Layer_Config_Info structure.
Tr_Source_House_Code	7-8	The transmitted packet source house code is transferred least significant byte first. If zero, a null address will be transmitted. See above if Tr_Source_Device_Code is 0xFFFF. For ADRUNACK_DATA and ADRACK_DATA this should be the Zone_Address or House_Code/System_Address.

[5] All of the Statistic Counters are free-running 8 bit counters and start at zero after a Reset. When any of the counters overflow, their respective overflow flag is set in the Status_Flags. All overflow flags are cleared by reading Status_Info with an SR command.

Table 8. Receive_Header_Info Structure

Field Name	Byte	Comments
Rc_Control_Field	0	The received packet control field. (See DLL_Control_Field description.)
Rc_Dest_Device_Code Alternate Use: IACK / FAILURE Info	1-2	The received packet destination address. The address field is stored least significant byte first. Alternate Use: Information Field from an IACK / FAILURE packets.
Rc_Dest_House_Code	3-4	The received packet destination house code. The destination house code is stored least significant byte first.
Rc_Source_Device_Code Alternate Use: ADR_IACK Info	5-6	The received packet source address is stored least significant byte first. If a null address was received, the field is set to zero. Alternate Use: The Information Field from ADR_IACK packet
Rc_Source_House Code	7-8	The received packet source house code is stored least significant byte first. If a null address was received, the field is set to zero.

Table 9. DLL_Control_Field Structure

Field	Bit	Use
DLL_Type	0-2	Indicates Type field value of the current receive packet.
DLL_Priority	3-4	Indicates the Priority field value of the current receive packet.
Reserved	5	Reserved
DLL_Class	6	Indicates the Service Class bit value of the current receive packet. Packets received with a Service Class of “EXTENDED” or ‘1’ will be accepted or ignored based on Rcv_ExtSvc_Accept.
Seq_#	7	Indicates the Sequence Number value of the current receive packet.

Table 10. Transmit_NPDU_Field Structure

Field Name	Bytes	Comments
Tr_NPDU	Variable	The Network Protocol Data Unit (Data Link Information Field) is stored in the order received from the host via the PT command. The maximum length of an NPDU is 32 bytes.

Table 11. Receive_NPDU_Field Structure

Field Name	Bytes	Comments
Rc_NPDU	Variable	The Network Protocol Data Unit (Data Link Information Field) is stored in the order received from the communication link. The maximum length of an NPDU is 32 bytes.

Table 12. DLL_Access_Control Structure

Field	Bit	Use	Reset State
CH_ACCESS_NUM	0-1	Specifies the number of ADRUNACK_DATA packets and channel accesses for each Data Link ADRUNACK_DATA transmit requested. 00 - 1 Access 01 - 2 Accesses 10 - 4 Accesses 11 - 8 Accesses	00
Reserved	2-3	Reserved	00
CH_ACCESS_PERIOD	4-5	Specifies the minimum required time in 100 ms intervals between attempted transmit channel accesses. 00 - 0 ms 01 - 100 ms 10 - 200 ms 11 - 300 ms	00
NUM_RETRIES	6	Enables immediate retry for ACK_DATA and ADRACK_DATA packets. 0 - No immediate retry 1 - Immediate retry	1
Auto_Retry	7	Enables multiple channel access retries for ADRACK_DATA and ADRUNACK_DATA packets. 0 - No multiple access retries 1 - Multiple access retries	0

Table 13. DLL_Rc_Link_Status Structure

Byte	Field	Bit	Use	Reset State
0	Rc_Refused	0	DLL mode: If Rc_Except is TRUE, indicates that a valid correctly addressed ACK_DATA or ADRACK_DATA packet was refused and discarded due to previous packet not being serviced by host, or refused based on unexpired receive sequence timer. 0 - Packet not refused 1 - Packet refused	0
	Rc_Overrun	1	DLL mode: If Rc_Except is TRUE, indicates that a valid correctly addressed UNACK_DATA or ADRUNACK_DATA packet was discarded due to previous packet not being serviced by host, or based on unexpired receive sequence timer. 0 - No packet overrun 1 - Packet overrun occurred	0
	Reserved	2	Reserved	0
	Phy_Layer_Fail_Status	3-5	If Physical_Layer_Failure is TRUE, indicates cause of physical layer failure if reported in Interface_Flags. 000 - An unexpected end-of-packet was detected. 001 - Transceiver interface error. 010 - Could not calibrate between $VCOf_{min}$ (830MHz) and $VCOf_{max}$ (1000MHz). 011 - Could not calibrate to $\pm$ 100 kHz of target channel frequency. 100 - Reserved 101 - Reserved 110 - Reserved 111 - Reserved	000
	Reserved	6-7	Reserved	00
1	Received_Channel	0-1	When accessed immediately following a packet read operation (with Rc_Refused and Rc_Overrun both FALSE), indicates the active received packet channel. 00 - Channel A 01 - Channel B 10 - Channel C 11 - Reserved	00
	Received_Sideband	2	When accessed immediately following a packet read operation (with Rc_Refused and Rc_Overrun both FALSE), indicates the active received packet sideband. 0 - Lower sideband 1 - Upper sideband	0
	Reserved	3-7	Reserved	00000

Host Physical Interface

Signal Descriptions

The Port Mode logical interface between the Host and SSC R400 uses 12 I/O lines. Eight are bi-directional data lines and four are handshake lines. An additional interface line is Reset.

Table 14. Port Mode Pin Descriptions

Mnemonic	Name	Direction	Use
DL0-DL7	Data pins	Input/Output	Bi-directional data lines. In high-impedance state when not in use for a transfer.
HSTST*	Host Strobe	Input	Falling edge active strobe from host. Used by host to initiate transfer of command in conjunction with HSTWR* signal, and used to indicate data byte available in host write mode, and to acknowledge data byte transfer in host read mode.
HSTWR*	Host Write	Input	Active low. Used to indicate a host write mode in conjunction with a Host Strobe signal. HSTWR* inactive (high) with HSTST* indicates end of host write mode, and end of any write command transfer.
DLLST*	DL Strobe	Output	Falling edge active strobe from SSC R400. (Falling edge active interrupt or latched flag at host). Used in conjunction with DLLWR* to get host attention and request a command sequence. Also used to indicate data available to host during a host read mode (with DLLWR* active), and to acknowledge the data byte transfer in host write mode.
DLLWR*	DL Write	Output	Active low. Used to indicate an attention request to the host in conjunction with a DLLST* signal if no transfer in progress. DLLWR* inactive (high) with DLLST* indicates the end of read command data transfer.
RESET*	Reset	Input	Reset Signal line. The host may assert this signal low (open collector drive) to provide a hardware reset.

Signal Timing

The interface timing is designed to support programmable transfers during which the transfer operation may have to be interrupted to service other activities. Accordingly the time allowed to service a DLLST* signal with a HSTST* signal from the host is up to 1000 µs before the SSC R400 will time-out the interface. The exception to the 1000 µs rule is the initial assertion of the DLLST* in an Attention sequence, in which case the HSTST* response can be delayed indefinitely without an interface time-out. However, an excessive delay in servicing an Attention sequence can cause a service overrun.

Because the host interface is a background task for the SSC R400, the host must allow up to 500 µs between its HSTST* signal and the DLLST* response. This gives the maximum time needed by the SSC R400 to process incoming packets. Typically, a command transfer will not have to wait more than 300 µs over an 800 µs period. These numbers are based on the incoming packet rate.

The DLLST* itself is a fixed length pulse of approximately 2.8 µs duration.

The maximum transfer rate is approximately 40k bytes per second.

Enhanced Protocol

The Enhanced Protocol interface timing is designed to improve the robustness of the host interface protocol. When Enhanced Protocol is turned on or off in the layer management write, the SSC R400 will respond to the end of the write using the newly selected protocol. A reset of the SSC R400 will turn Enhanced Protocol off. Enhanced Protocol consists of an additional DLLST* signal in response to the end of a host-write sequence and an additional HSTST* signal in response to the end of a host-read sequence. The extra strobes provided by the Enhanced Protocol are indicated in the timing diagrams by the label “END ACK” and allow the interface to run as fast as possible without fixed time delays. Refer to the additional Enhanced Read Sequence and Enhanced Write sequence timing diagrams (Figures 5 and 6) for details.

Command Sequence

A host may be “forced” to initiate a command sequence by an attention sequence (the command sequence is presumably an Interface_Flags read), or the host may issue a command independently and asynchronously. In either case, the host starts a command sequence by putting the command on DL0-DL7 and asserting HSTWR*. If the host is not responding to an Attention DLLST*, the host must, in a non-interruptible sequence lasting not more than 15 μs, check that DLLWR* is not asserted before asserting HSTST*. If DLLWR* is asserted the host must wait for the Attention DLLST*, then acknowledge with a HSTST* and indicate a command on DL0-DL7 and continue with the command sequence.

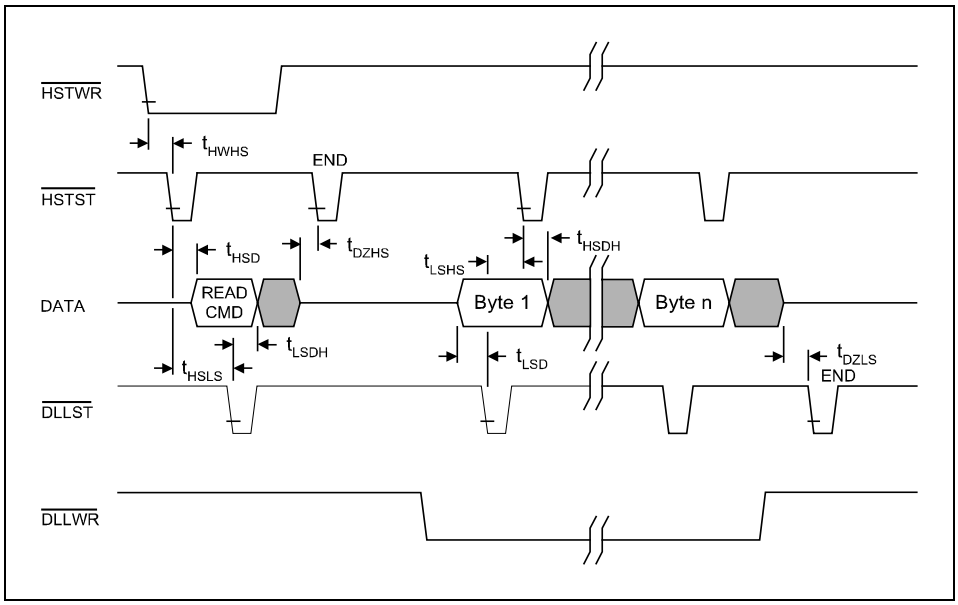


Figure 3. Host Read Command Sequence Diagram

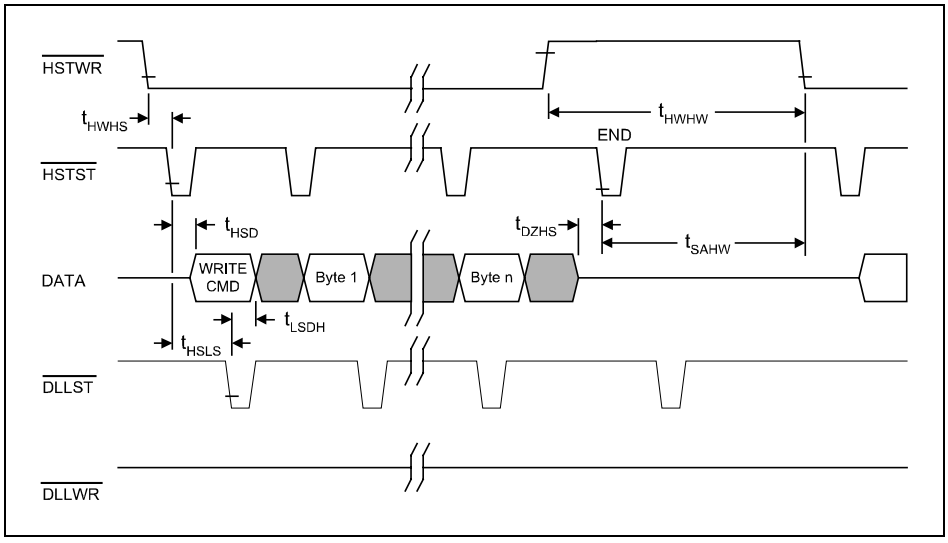


Figure 4. Host Write Command Sequence Diagram

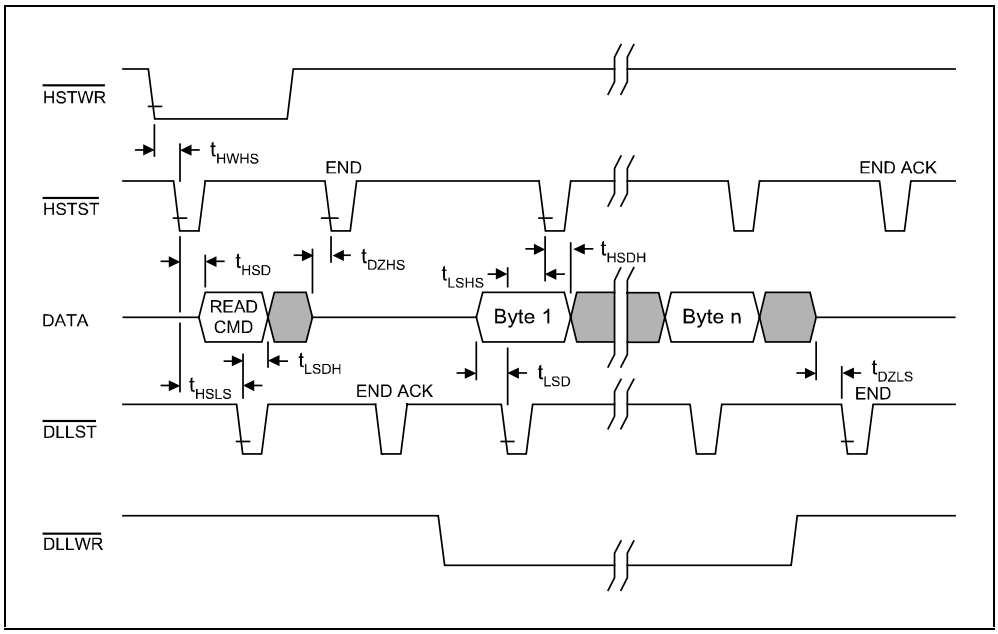


Figure 5. Enhanced Host Read Command Sequence Diagram

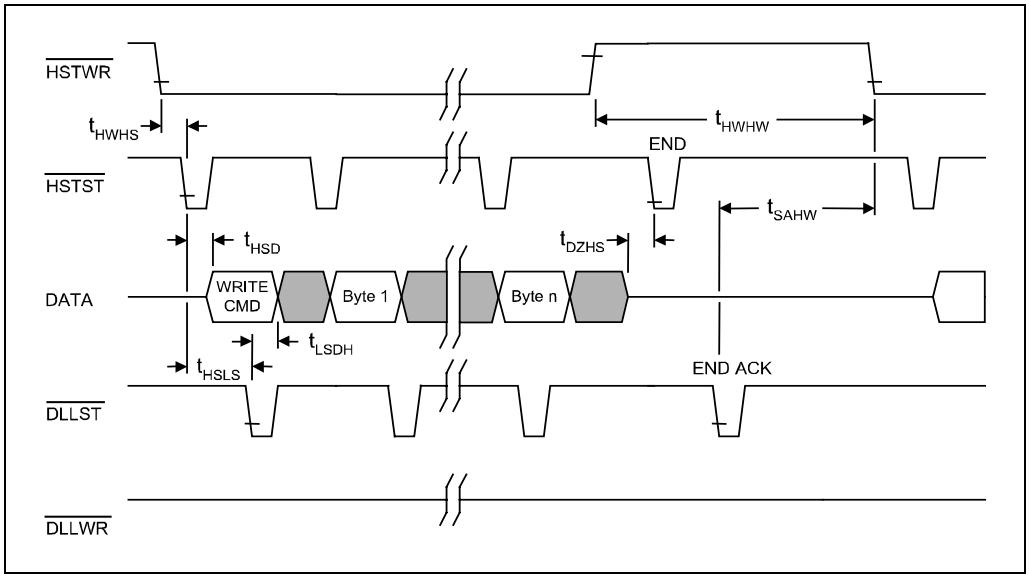


Figure 6. Enhanced Host Write Command Sequence Diagram

Attention Sequence

An Attention sequence is used to “force” the host to execute a command sequence. To prevent a race condition, a non-interruptible Attention sequence is executed by first asserting DLLWR*, and then waiting approximately 15 usec while checking for a HSTST* signal. If a HSTST* is seen during this time, DLLWR* is dropped and the host command sequence is performed. If after approximately 15 μs, no HSTST* has been seen, the DLLST* signal is asserted. The next HSTST* is then interpreted as an acknowledgment of the Attention sequence and the beginning of a host command sequence. The HSTWR* should be asserted by the host prior to asserting the HSTST* and then the DLLWR* signal will be dropped in response to the HSTST* signal. The host command sequence continues, typically with an IR command to access the Interface_Flags byte.

Any command can be executed in response to an attention sequence. However, if the host does not execute an Interface Read command then there is a risk of data loss if the attention sequence is signaling an incoming packet.

NOTE: It is incumbent on the host to read and process any and all asserted flags in the Interface_Flags byte since the flags are cleared immediately after they are read by the host.

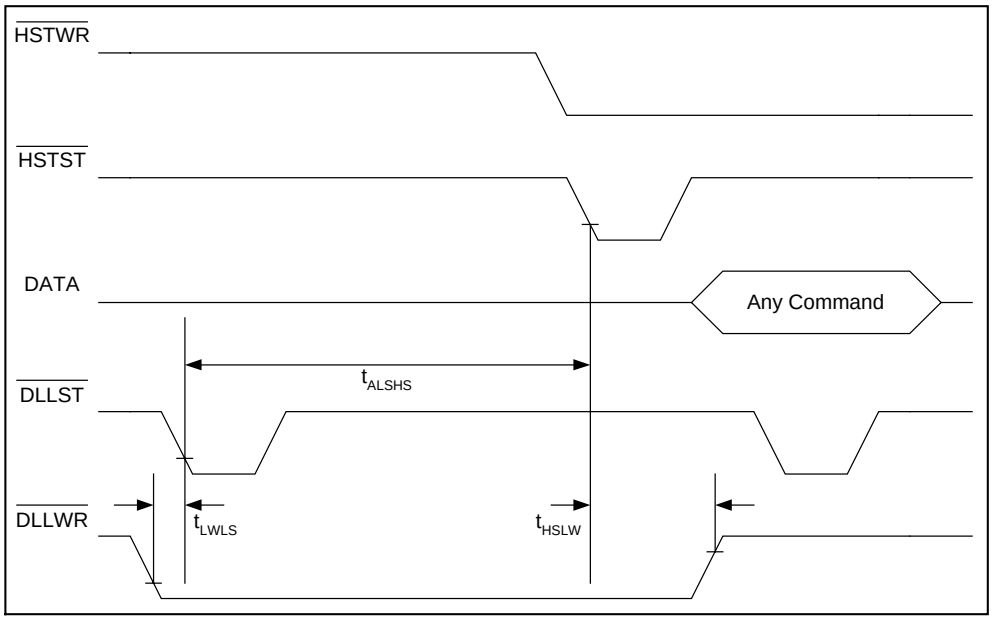


Figure 7. Attention Sequence Timing Diagram

Table 15. Host Command Sequence Timing Values

Symbol	Parameter	Min	Max	Units	Notes
t_{HWHS}	HSTWR* to HSTST* Delay		15	µsec	1,2,3
t_{HSD}	HSTST* to DATA Setup		0	µsec	1,2
t_{HSLS}	HSTST* to DLLST* Delay		1000	µsec	1,2,3
t_{LSDH}	DLLST* to DATA Hold	0		µsec	1,2
t_{DZHS}	DATA High Z to HSTST* Setup	1		µsec	1,2
t_{LSD}	DLLST* to DATA Setup	1		µsec	1,2
t_{LSHS}	DLLST* to HSTST* Delay		1000	µsec	1,2,3
t_{HSDH}	HSTST* to DATA Hold	1		µsec	1,2
t_{DZLS}	DATA High Z to DLLST* Setup	1		µsec	1,2
t_{HWHW}	HSTWR* to HSTWR* Delay w/o Enhanced Protocol	500		µsec	1,2,3
t_{SAHW}	DLLST* (END ACK) to HSTWR* Delay w/ Enhanced Protocol	0		µsec	1,2,3
t_{LWLS}	DLLWR* to DLLST* Delay		15	µsec	1,2,3
t_{ALSHS}	DLLST* (Attention) to HSTST* Delay		2.7	msec	1,2,3
t_{HSLW}	HSTST* to DLLWR* Delay		500	µsec	1,2,3

NOTES:

1. Measured at V_{IH}=2.0V or V_{IL}=0.8V and 10msec maximum rise and fall time.
2. Measured with 50 pF load.
3. Measured at V_{OH}=2.4V or V_{OL}=0.4V.

Mechanical

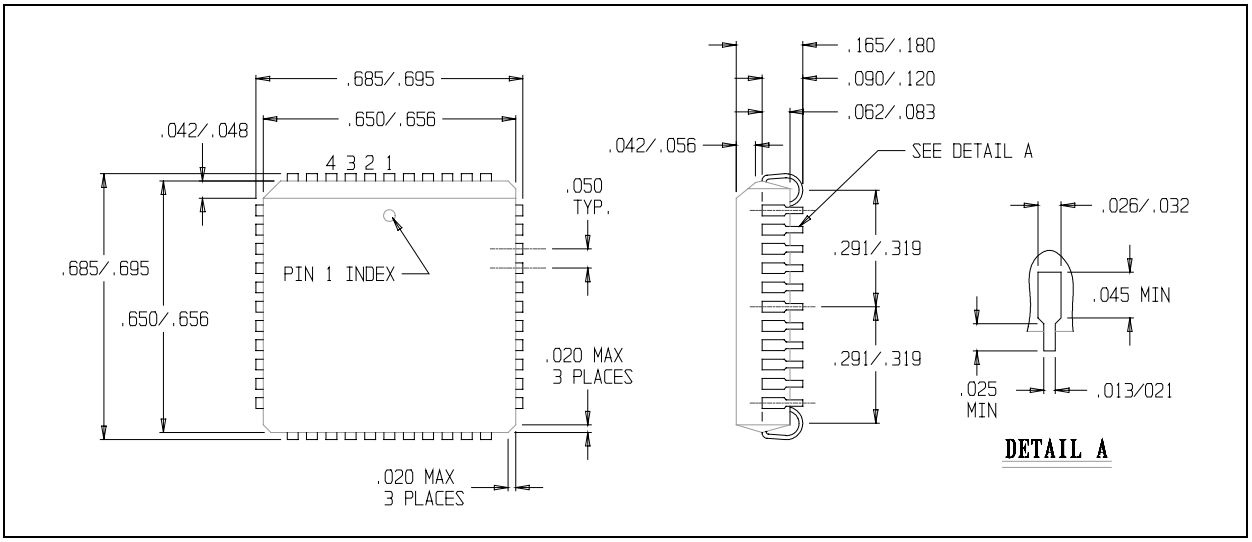


Figure 8. SSC R400 IC Mechanical Drawing

Supplemental Information

RF Design Package

- White paper #0026 “RF SSC Technology”
- Application Note # 0057 “CENode (Host) Interface”
- Application Note #0064 “Your First CEBus Packet”

Ordering Information

SSC R400	RF Network Interface Controller, 44 PLCC

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