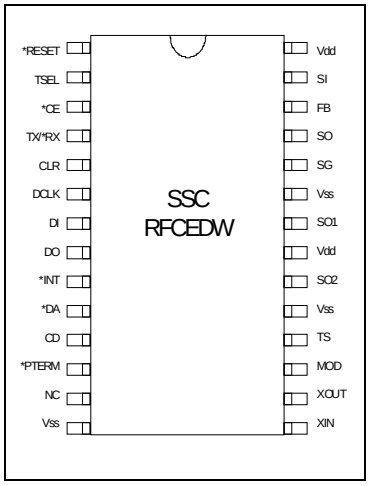
SSC RFCEDW

RF Transceiver IC, CEBus Compliant



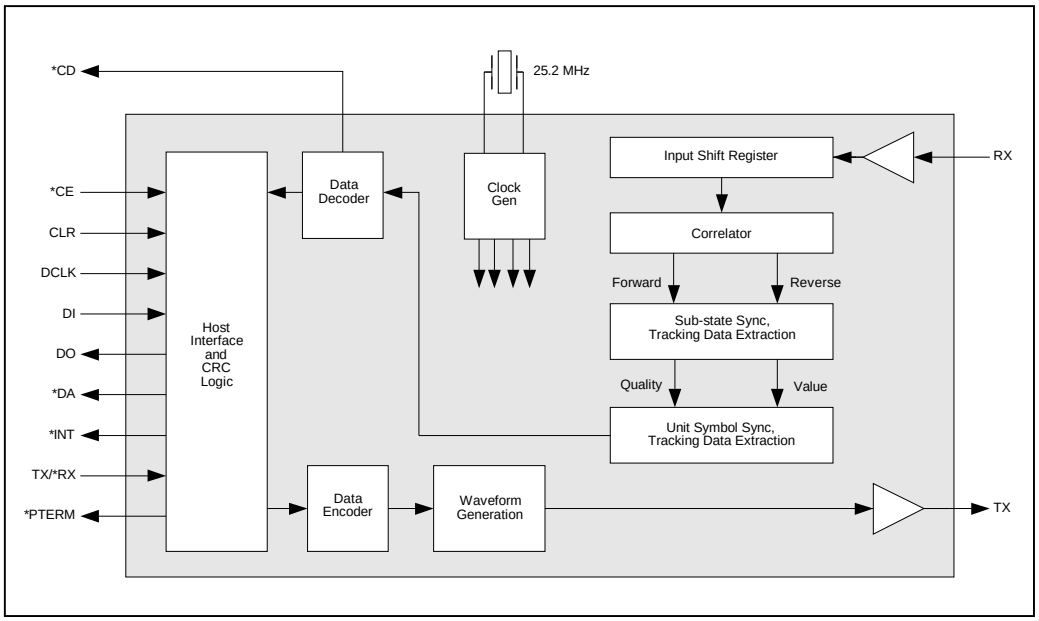
Features

- Implements baseband signaling for EIA-600 (CEBus® Standard) RF Physical Layer
- Spread Spectrum Carrier™ technology
- Data rate of 10,000 "one-bits" per second
- 16-bit CRC for reliable communications
- Uses Intellon's symbol interface
- FCC Part 15 unlicensed 902-928 MHz design
- 28 pin SOIC package

Introduction

The Intellon SSC RFCEDW is the principal component used to implement the EIA-600 radio frequency (RF) Physical Layer, operating at a data rate of 10,000 "one-bits" (USTs) per second. Data is transferred between the host and the SSC RFCEDW in groups of eight (8) Unit Symbol Times (UST) using a synchronous serial interface. The SSC RFCEDW performs all the spread spectrum signal generation and reception. With the addition of appropriate RF circuitry a FCC Part 15.247 unlicensed spread spectrum radio transceiver can be implemented.

SSC RFCEDW Block Diagram



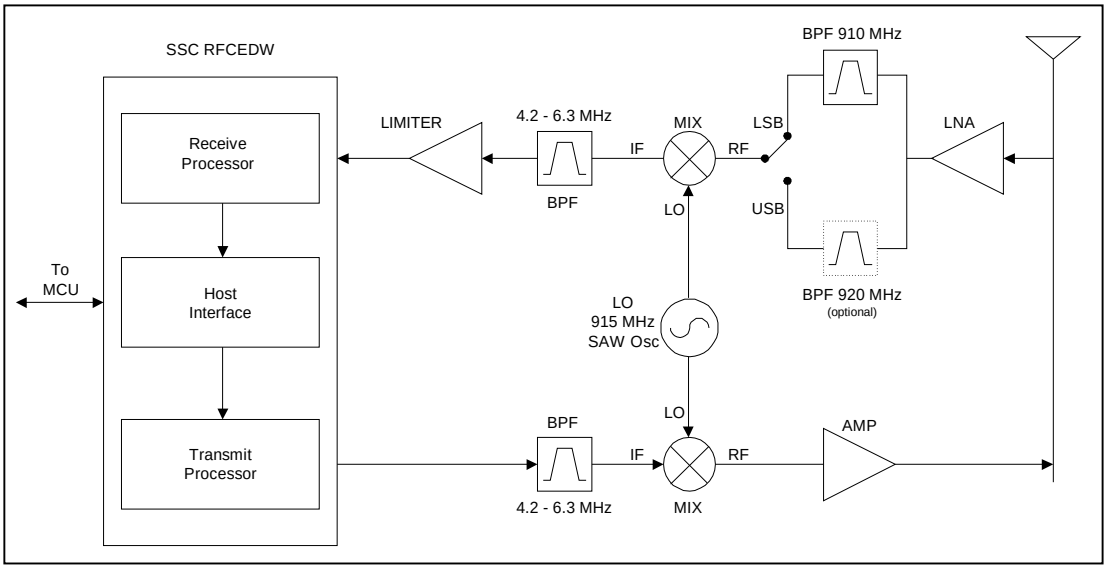
SSC RFCEDW Description

The SSC RFCEDW provides all of the timing requirements specified by the EIA-600 RF Physical Layer specification. The host controller is not responsible for any Physical Layer timing. The SSC RFCEDW handles portions of the Physical Layer Symbol Encoding (PLSE) sub-layer, including complete CRC generation and detection, and some Media Access Control (MAC) sub-layer functions. The SSC RFCEDW also does preamble detection and stripping on reception, and provides for all data synchronization and timing.

Specifications

Parameter	Value/Range
Supply Voltage	+ 5 Vdc (+/- 10%)
Supply Current (Tx)	30 mA
Supply Current (Rx)	30 mA
Oscillator Frequency	25.20 MHz
Output Current	+/- 48 mA (max.)
Output Impedance	50 Ohm typical
Operating Temperature	-40° C to +85° C

Application Circuit



Ordering Information

Part No.	Description	Tube Qty.	Package
SSC RFCEDW	RF Transceiver IC, CEBus Compliant	25	28 pin SOIC