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Audacity-T2U Processor

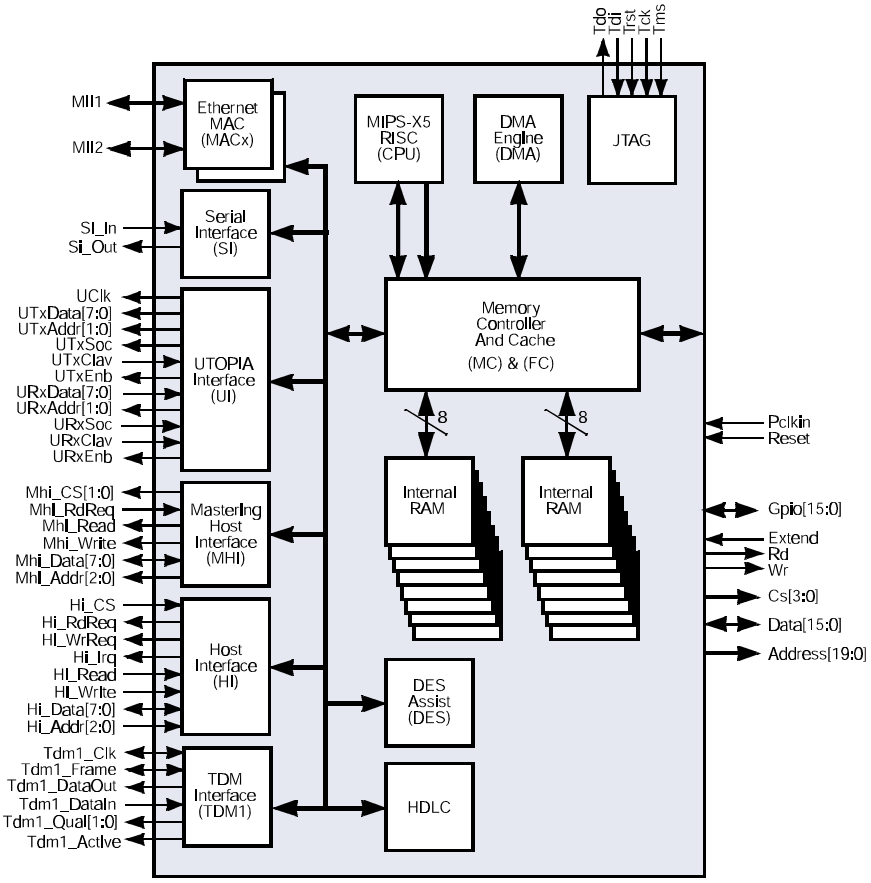
Netergy Microelectronics' Audacity-T2U Voice-over-Packet (VoP) processor is a high performance system-on-a-chip that contains a unified RISC/DSP processor, an Ethernet 10/100 Base-T MAC, and an ATM Utopia interface that is also configurable as a second Ethernet MAC. The Audacity-T2U processor has substantial on-chip SRAM, eliminating the need for external SRAM or DRAM when deployed with Netergy Microelectronics' Veracity VoIP software suite.

The Veracity software suite for the Audacity-T2U processor provides all the features required for VoIP applications. The compact and efficient stacks reside in an external FLASH memory and leave memory space for system application code within the same FLASH. Supported codecs include G.711, G.723.1, G.726, G.728, G.729A/B, and G.729E. Supported call control protocols include H.323, MGCP, SIP, and Megaco. The Veracity software suite also provides T.38 FAX-over-IP (FoIP) capability. For Voice-over-DSL (VoDSL) applications, ATM application adaptation layers AAL2 and AAL5 protocol stacks are supported. There are no third party royalty fees associated with the use of any Netergy Microelectronics' standards-compliant call control protocols.

When used with the Veracity software suite and development environment, the Audacity-T2U processor makes it easy to build cost effective, high quality VoIP/VoDSL gateways, IP-PBXs, and IP phones.

Features

- Netergy Microelectronics' MIPS-X5 unified RISC and DSP core (up to 180 DSP MIPS)
- Pin and code compatible with the Audacity-T2 processor
- 384 KByte on-chip RAM, 16-way interleaved with single cycle access
- 16 KByte, 2-way set associative cache for external FLASH/SRAM memory
- Hardware support for cache profiling and application performance analysis
- External memory-mapped bus supporting 8-bit and 16-bit asynchronous devices
- 4K instructions (16K Bytes) of internal boot ROM
- Four external chip selects for glueless memory-mapped bus interfacing
- External ISA/SRAM-like device support via memory-mapped bus
- Multichannel DMA engine integrated with peripherals
- Hardware acceleration for DES/3DES, CRC, and HDLC operations
- Two 10/100 Base-T Ethernet MACs with MII interface for external PHY
- ATM UTOPIA interface, level 2, single status, 8-bit databus, 2 ports
- H.100/H.110, MVIP, and SCSA compatibility via TDM port
- Multimedia codec compatibility via TDM port
- Glueless multiple SLAC support via TDM port
- GCI/IOM-2 support via TDM port
- Mastering Host port for scaleable multi-chip systems
- Serial and parallel debug interface via Serial and Host Interfaces
- Glueless support of SLIC/SLAC ringing and on/off hook features via GPIO functions
- Glueless support of character LCD via GPIO functions
- Telephone-style keypad and LED support via GPIO functions
- IEEE-1149.1 JTAG boundary scan board-level test interface
- Low power, 1.8V core voltage, 3.3V I/O voltage
- 0.18 micron 6 layer metal CMOS process
- 196-pin BGA package, body size 15x15mm, ball pitch 1mm



Architecture

The Audacity-T2U processor implements a Harvard-architecture RISC microprocessor with substantial DSP extensions:

- The **CPU** implements Netergy Microelectronics' MIPS-X5 ISA (Instruction Set Architecture). The CPU supports single cycle multiply-accumulate with concurrent address pointer update and memory to register file data fetch. The multiplier supports all combinations of 16-bit and 32-bit precision operations. Four dedicated address pointer registers, two 40-bit accumulators, and 32 general-purpose 32-bit registers are included in the CPU.

- The **Memory Controller** provides arbitration and non-blocking switching between internal RAM interleaves, peripherals, CPU, and the DMA engine.

- The **Host Interface** allows external microprocessors to operate with the Audacity-T2U processor. The Host Interface has three logical bi-directional ports supported by six DMA channels.

- Two **Ethernet Media Access Controllers (MACs)** implement the packet based network interface(s).

- An internal **DMA Engine** supports all DMA channels.

- A **TDM Bitstream Interface** implements the raw audio input/output mechanism. The TDM is very flexible and supports four bi-directional streams via eight DMA channels.

- The **Mastering Host Interface** allows the Audacity-T2U to communicate efficiently with two additional Audacity-T2U or Audacity-T2 processors. The interface supports a bi-directional DMA stream in hardware for each slave device.

- A **UTOPIA Interface** supports the direct connection of an ATM PHY, typically a xDSL modem device. The interface provides hardware ATM header expansion/packing using an aligned descriptor and supports programmable hardware acceleration for header matching of received cells. The interface is supported by four DMA channels.

- The **UART Interface** provides a two-wire serial port with hardware DMA support.

- The **DES Accelerator** provides a low-level hardware based implementation of the compute-intensive DES encryption algorithm. With the supporting software, numerous encryption standards, such as IPSec, can be efficiently implemented.

- The **HDLC/CRC Accelerator** provides a hardware implementation of low-level HDLC (High-level Data Link Control) bitstream operations as well as 10-bit, 16-bit, and 32-bit CRC algorithms.

- The 43 pin **General-Purpose I/O Interface** supports character-based liquid crystal displays, keypad scanning, LED operation, and slave to master IRQs in multi-device configurations.

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