FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-28216-2E

ASSP For Video Applications

CMOS

8-bit 100 MSPS A/D Converter

MB40C328

■ DESCRIPTION

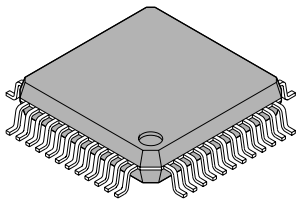
MB40C328 is a high-speed A/D converter using a fast CMOS technology.

■ FEATURES

- Resolution : 8 bit
- Linearity error : ±0.40% (standard)
- Maximum conversion rate : 100 MSPS (minimum)
- Power supply voltage : 3.3 V single (standard)
- Digital input/output voltage range : CMOS level compatible
- Analog input voltage range : 0 to 3.0 V (2 Vp-p)
- Analog input capacitance : 22 pF (standard)
- Power dissipation : 210 mW (standard)
- Additional features : Reference voltage generator circuit: V_{REFT} = 3.0 V, V_{REFB} = 1.0 V
  High impedance output, power down function
  1:2 demultiplex output enable (RESET action enable)
  1/2 deviding clock output
  Cross sampling at 50 MHz (two-phase CLK) enable (CLKA, CLKB)
- Package : LQFP48 (7 mm × 7 mm, lead pitch 0.5 mm)

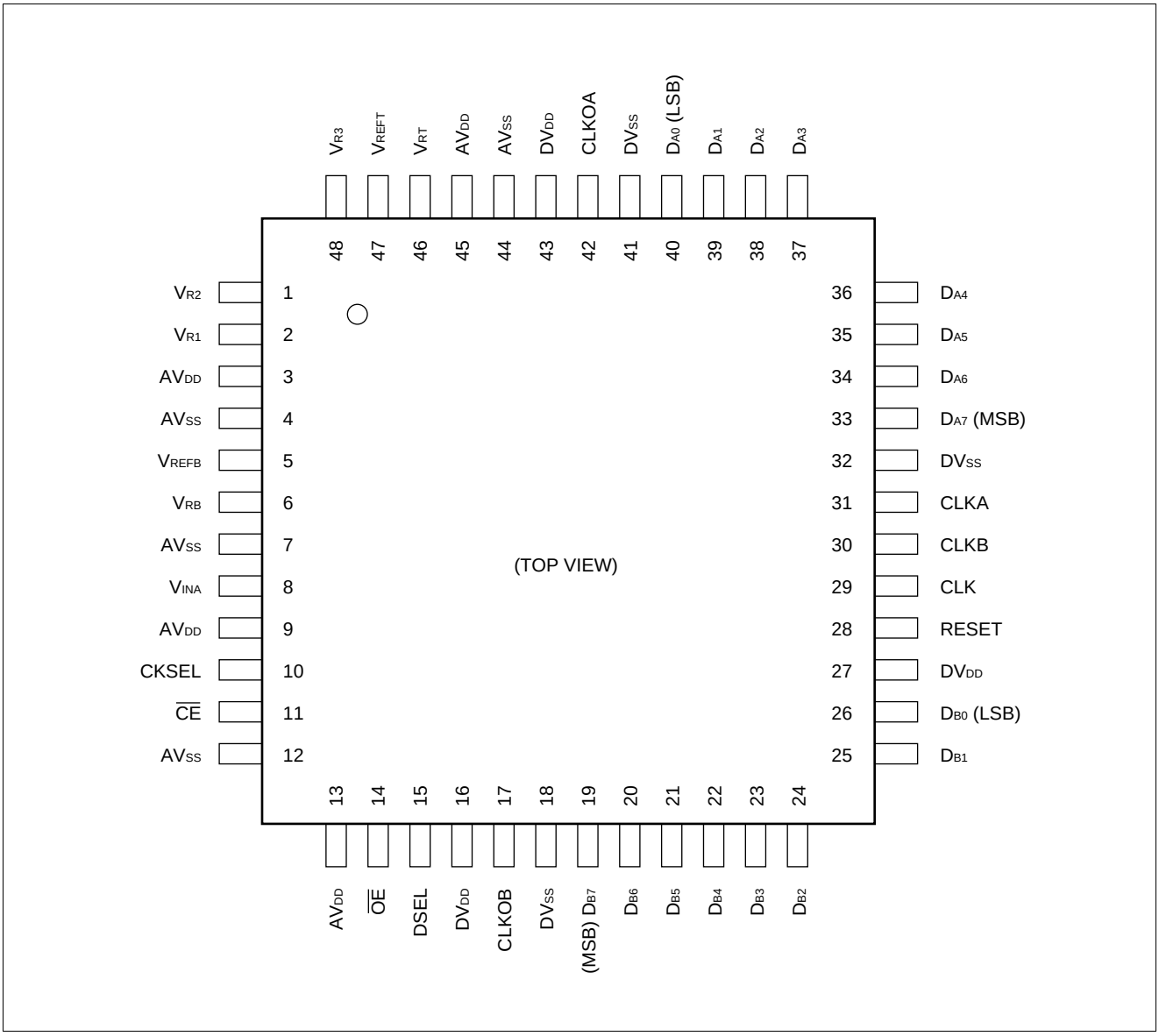
■ PACKAGE

48-pin plastic LQFP



(FPT-48P-M05)

■ PIN ASSIGNMENT



■ PIN DESCRIPTION

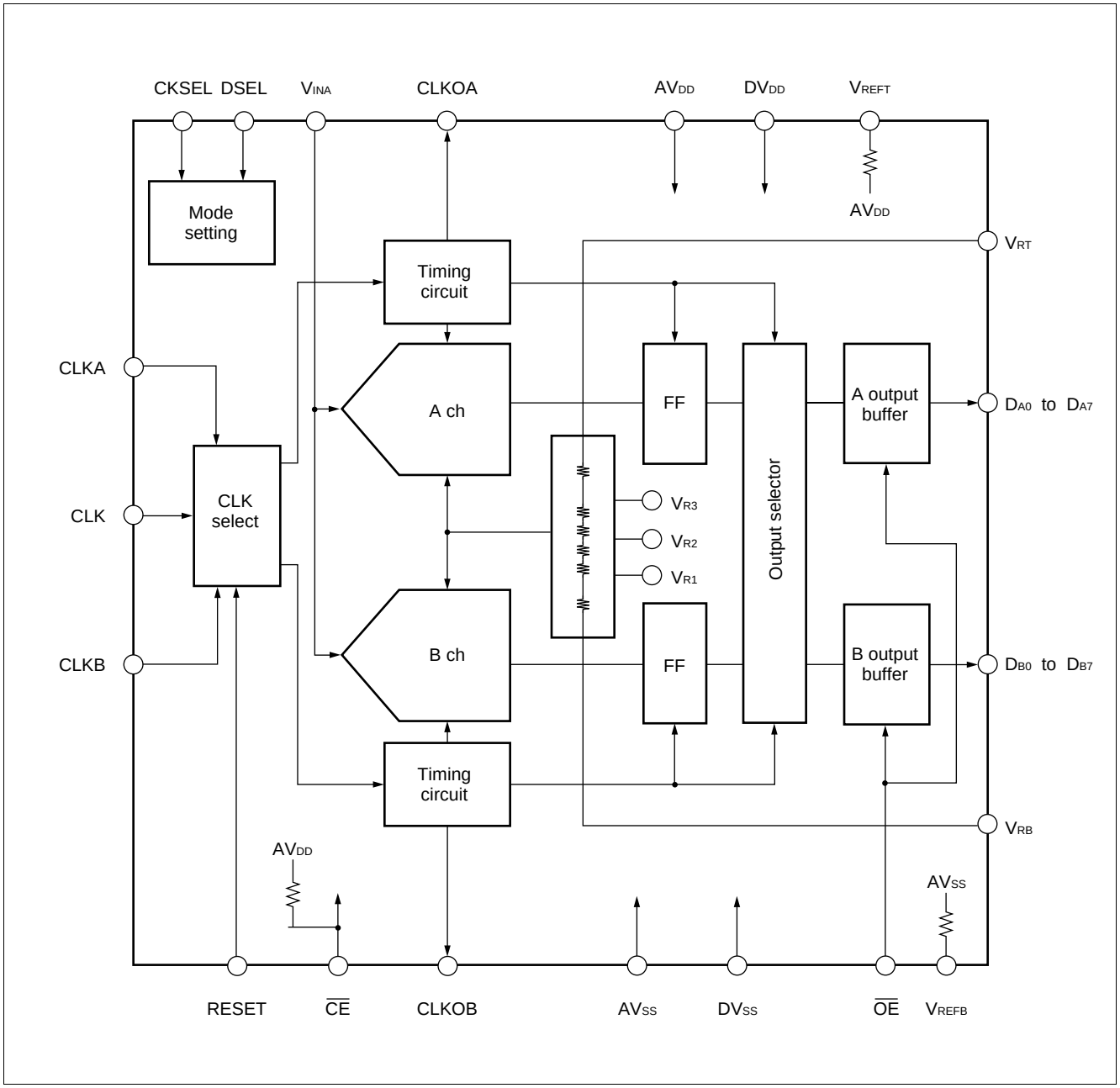
Pin No.	Symbol	Description
3, 9, 13, 45	AV_{DD}	Analog power supply (+3.3 V)
16, 27, 43	DV_{DD}	Digital power supply (+3.3 V)
4, 7, 12, 44	AV_{SS}	Analog power supply ground pin (0 V)
18, 32, 41	DV_{SS}	Digital power supply ground pin (0 V)
33 to 40	D_{A7} to D_{A0}	Digital output pin (Port A) D_{A7}: MSB, D_{A0}: LSB
19 to 26	D_{B7} to D_{B0}	Digital output pin (Port B) D_{B7}: MSB, D_{B0}: LSB
11	$\overline{CE}$	Power down at $\overline{CE}$ input “H” (internal pull-up resistor)
14	$\overline{OE}$	Digital output (Both Port A, B) and clock output (CLKOA, CLKOB) are high impedance at $\overline{OE}$ input “H”.
10	CKSEL	Mode of operation setting input pin (Refer to ■ MODE SETTING)
15	DSEL	
28	RESET	Dividing circuit reset input pin (See ■ TIMING CHART 2, 3)
29	CLK	Clock input pin (max 100 MHz)
31	CLKA	A ch clock input pin (max 50 MHz)
30	CLKB	B ch clock input pin (max 50 MHz)
42	CLKOA	Clock output pin (See ■ TIMING CHART 1 to 4)
17	CLKOB	Clock output pin (See ■ TIMING CHART 1 to 4)
8	V_{INA}	Analog input pin Input range is V_{RT} to V_{RB} (0 V to 3.0 V: 2 Vp-p)
2 1 48	V_{R1} V_{R2} V_{R3}	Reference 1/4 voltage output pin (Add 0.1 µF for AV_{SS}) Reference 1/2 voltage output pin (Add 0.1 µF for AV_{SS}) Reference 3/4 voltage output pin (Add 0.1 µF for AV_{SS})
46	V_{RT}	Reference voltage input pin on top side
47	V_{REFT}	Reference voltage output pin By connecting to V_{RT}, 0.9 × AV_{DD} (≒ 3 V) is generated.
6	V_{RB}	Reference voltage input pin on bottom side
5	V_{REFB}	Reference voltage output pin By connecting to V_{RB}, 0.3 × AV_{DD} (≒ 1 V) is generated.

The values in parentheses are standard.

■ PRECAUTIONS ON USE

- Be sure to ground the pins of AV_{DD}, DV_{DD}, V_{RT}, V_{RB}, V_{R1}, V_{R2}, and V_{R3} via high-frequency capacitor. Place the high-frequency capacitor as close as possible to the pin.
- To avoid generation of undesired current owing to indetermination of internal logic, set $\overline{CE}$ to “H” at powering on and input more than five clock pulses just after operation ($\overline{CE}$: “H” → “L”).

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Power supply voltage	AV_{DD}, DV_{DD}	–0.3	+4.0	V
Input/output voltage	V_{INA}, V_{RT}, V_{RB}, V_{REFT}, V_{REFB}, V_{R1}, V_{R2}, V_{R3}, $\overline{CE}$, CKSEL	–0.3	AV_{DD}+0.3*	V
	D_{A0} to D_{A7}, D_{B0} to D_{B7}, CLKOA, CLKOB, CLKA, CLKB, CLK, DSEL, $\overline{OE}$, RESET	–0.3	DV_{DD}+0.3*	V
Storage temperature	T_{STG}	–55	+125	°C

* : Do not exceed +4.0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
Power supply voltage		AV_{DD}, DV_{DD}	3.00	3.30	3.60	V
Analog input voltage		V_{INA}	V_{RB}	—	V_{RT}	V
Analog reference voltage: T		V_{RT}	—	—	3.00	V
Analog reference voltage: B		V_{RB}	0.00	—	—	V
Analog reference voltage range		$V_{RT} – V_{RB}$	1.90	2.00	2.10	V
Digital “H” level input voltage	$\overline{OE}$, DSEL, RESET, CLK, CLKA, CLKB	V_{IHD}	$DV_{DD} – 0.5$	—	—	V
	CKSEL, $\overline{CE}$		$AV_{DD} – 0.5$	—	—	V
Digital “L” level input voltage	$\overline{OE}$, DSEL, RESET, CLK, CLKA, CLKB	V_{ILD}	—	—	0.5	V
	CKSEL, $\overline{CE}$		—	—	0.5	V
Digital input current		I_{ID}	–20	—	5	μA
Single-phase clock frequency		f_{CLK}	0.1	—	100	MHz
Two-phase clock frequency		f_{CLKA}, f_{CLKB}	0.1	—	50	MHz
Minimum clock pulse width (single-phase)		t_{WS}^+, t_{WS}^-	4.0	5.0	—	ns
Minimum clock pulse width (two-phase)		t_{WD}^+, t_{WD}^-	8.0	10.0	—	ns
Clock pulse rising/falling time		t_r, t_f	—	2.0	—	ns
RESET signal setup time		t_s	3.0	—	—	ns
RESET signal hold time		t_h	3.0	—	—	ns
Operating temperature range		Ta	–20	—	70	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

• DC Characteristics in Analog Section

(AV_{DD} = DV_{DD} = 3.00 V to 3.60 V, Ta = –20°C to +70°C)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Resolution	—	—	8	—	bit
Linearity error	LE	—	±0.40	±0.6	%
Differential linearity error	DLE	—	±0.20	±0.36	%
Analog input capacity	C_{INA}	—	22	—	pF
Reference voltage: T	V_{REFT}	$0.88 \times AV_{DD}$	$0.91 \times AV_{DD}$	$0.94 \times AV_{DD}$	V
Reference voltage: B	V_{REFB}	$0.27 \times AV_{DD}$	$0.3 \times AV_{DD}$	$0.33 \times AV_{DD}$	V
Reference current	I_{RB}	–15	–10	—	mA
Analog supply current	AI_{DD}	—	42.0	85.0	mA
Digital supply current	DI_{DD}	—	20.0	40.0	mA
Standby current	I_{SB}	—	100	—	mA

• DC Characteristics in Digital Section

(AV_{DD} = DV_{DD} = 3.00 V to 3.60 V, Ta = –20°C to +70°C)

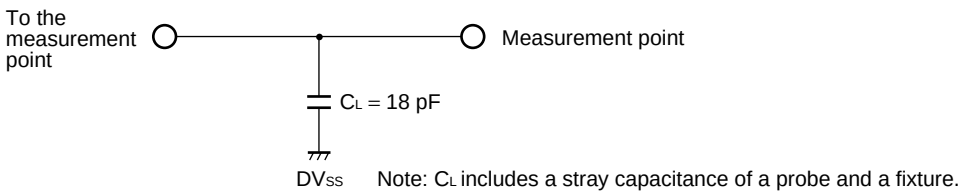
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Digital “H” level output voltage	V_{OHD}	DV_{DD} – 0.4	—	DV_{DD}	V
Digital “L” level output voltage	V_{OLD}	—	—	0.4	V
Digital “H” level output current	I_{OHD}	–400	—	—	µA
Digital “L” level output current	I_{OLD}	—	—	1.6	mA

• **Switching Characteristics**

(AV_{DD} = DV_{DD} = 3.00 V to 3.60 V, Ta = –20°C to +70°C)

Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
Maximum conversion rate		f_S	100	—	—	MSPS
Aperture time		t_{AD}	—	1.7	—	ns
Digital output delay time	Timing chart 1	t_{pdS}	2.5	6.0	9.0	ns
		t_{pdSO}	t_{WS^+} + 2.5	t_{WS^+} + 6.0	t_{WS^+} + 10	ns
	Timing chart 2	t_{pdM1}	2.5	5.5	10	ns
		t_{pdM1O}	T + 2.5	T + 5.5	T + 10	ns
	Timing chart 3	t_{pdM2}	2.5	5.5	10	ns
		t_{pdM2O}	T + 2.5	T + 5.5	T + 10	ns
	Timing chart 4	t_{pdD}	2.5	6.5	11	ns
		t_{pdDO}	t_{WD^+} + 2.5	t_{WD^+} + 6.5	t_{WD^+} + 11	ns

■ DIGITAL OUTPUT BUFFER LOAD CIRCUIT



Note: C_L includes a stray capacitance of a probe and a fixture.

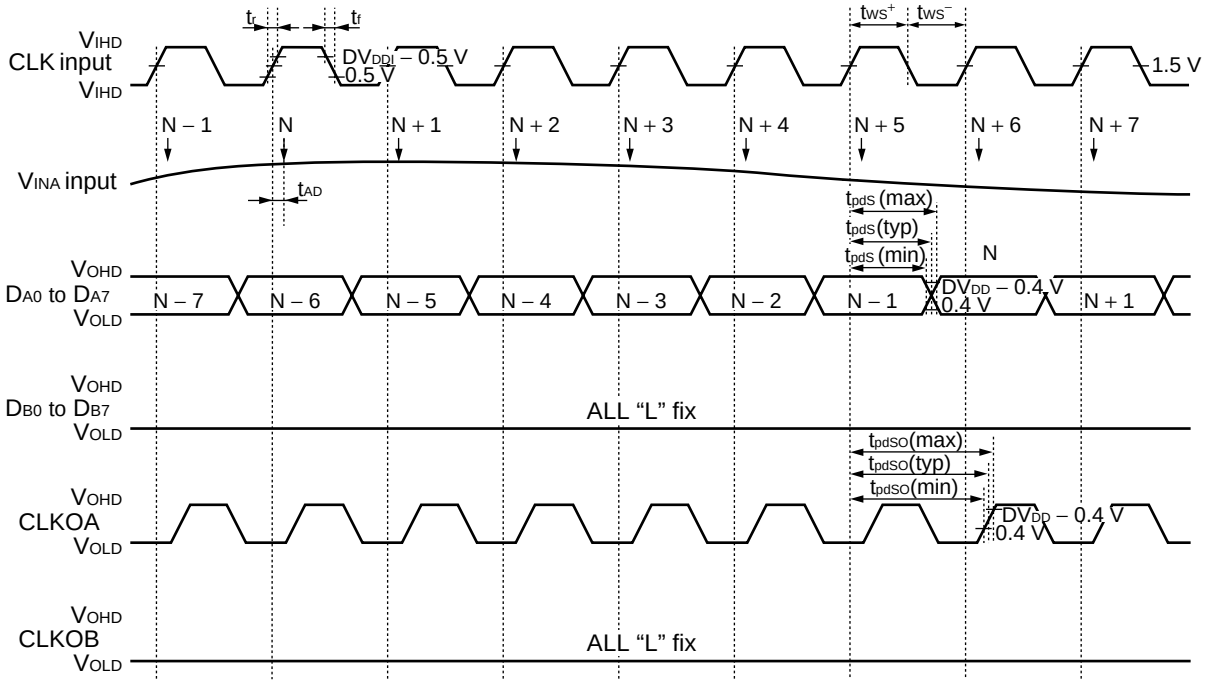
■ MODE SETTING

CKCEL	DCEL	Mode	Timing Chart
H	H	CLK input-straight output mode	Timing chart 1
H	L	CLK input-demultiplex output (in-phase) mode	Timing chart 2
L	H	CLK input-demultiplex output (two-phase) mode	Timing chart 3
L	L	Two-phase CLK input mode (CLKA, CLKB)	Timing chart 4

■ TIMING CHART 1

CLK input-straight output mode

- CLK = 100 MHz (max)
- CLKA = CLKB = “L” (DV_{SS})
- CKSEL = “H” (AV_{DD})
- DSEL = “H” (DV_{DD})
- RESET = “H” (DV_{DD})
- $\overline{CE}$ = “L” (AV_{SS})
- $\overline{OE}$ = “L” (DV_{SS})

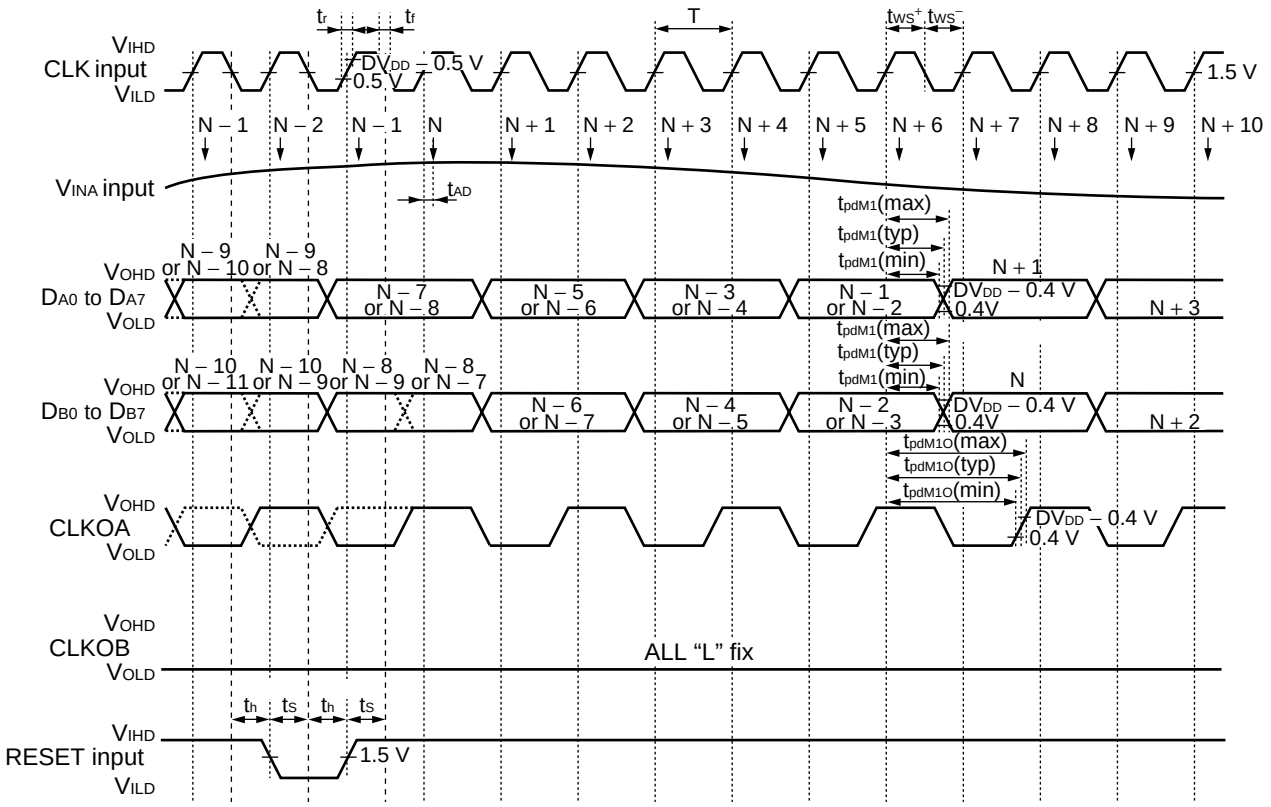


- V_{INA} input — Sampling at CLK rising
- D_{A0} to D_{A7} — Output (after 5 CLK + t_{pdS} from Sampling) at CLK rising

■ TIMING CHART 2

CLK input-demultiplex output (in-phase) mode

- CLK = 100 MHz (max)
- CLKA = CLKB = “L” (DV_{SS})
- CKSEL = “H” (AV_{DD})
- DSEL = “L” (DV_{SS})
- $\overline{CE}$ = “L” (AV_{SS})
- $\overline{OE}$ = “L” (DV_{SS})

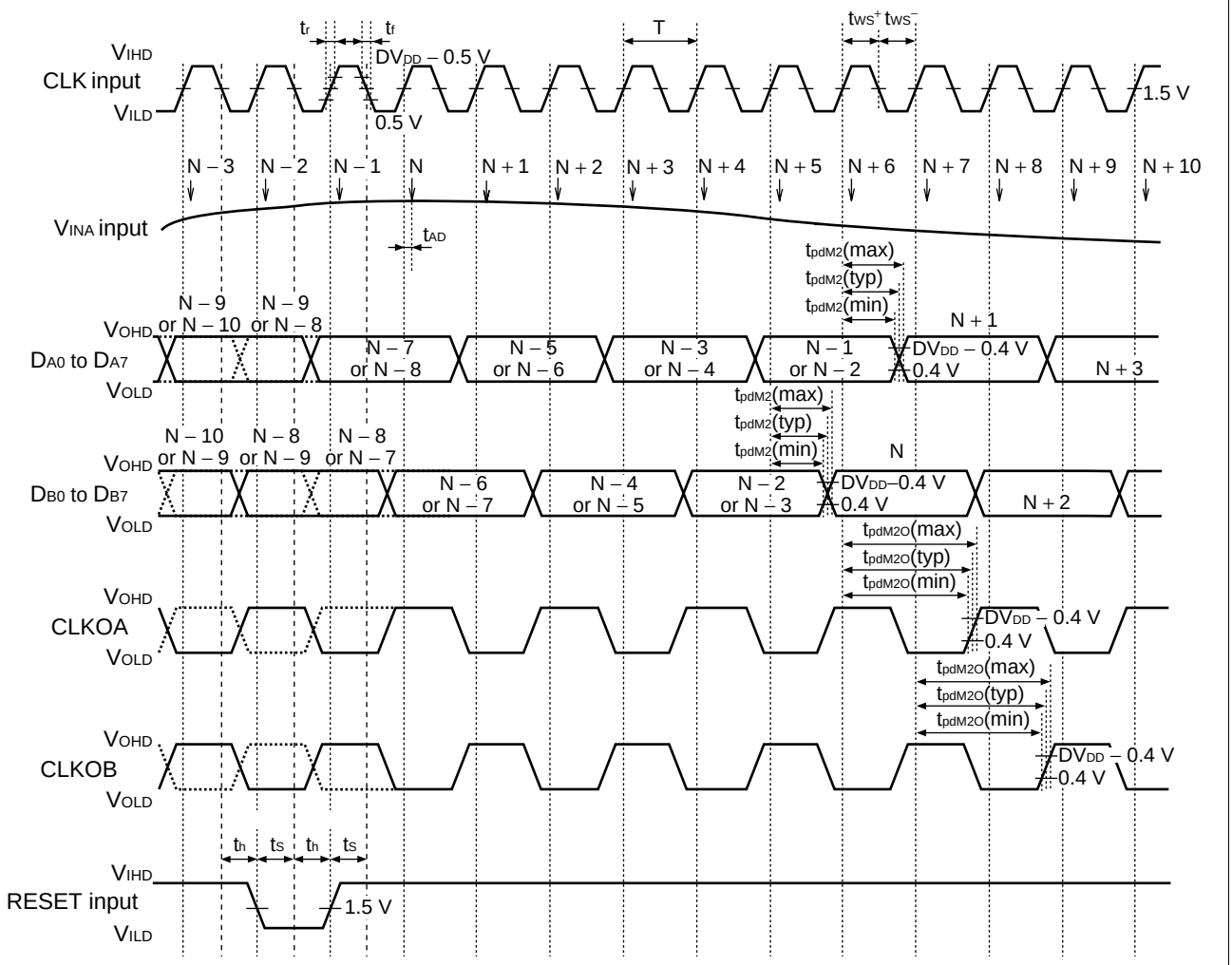


- V_{INA} input — Sampling at CLK rising
- D_{A0} to D_{A7} — Output (after 5 CLK + t_{pdM1} from Sampling) at CLK rising
- D_{B0} to D_{B7} — Output (after 6 CLK + t_{pdM1} from Sampling) at CLK rising

■ TIMING CHART 3

CLK input-demultiplex output (two-phase) mode

- CLK = 100 MHz (max)
- CLKA = CLKB = “L” (DV_{SS})
- CKSEL = “L” (AV_{SS})
- DSEL = “H” (DV_{DD})
- $\overline{CE}$ = “L” (AV_{SS})
- $\overline{OE}$ = “L” (DV_{SS})

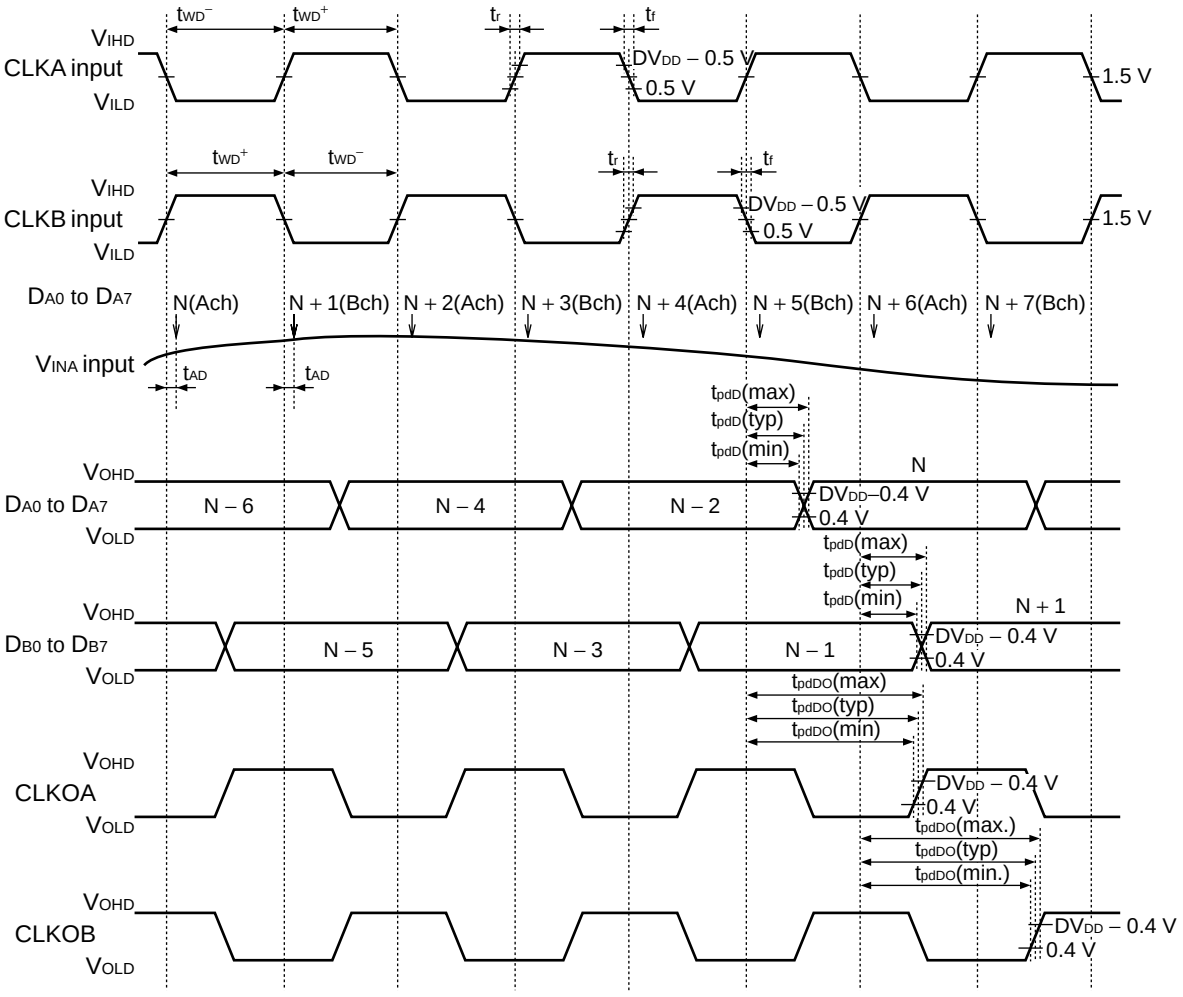


- V_{INA} input — Sampling at CLK rising
- D_{A0} to D_{A7} — Output (after 5 CLK + t_{pdM2} from Sampling) at CLK rising
- D_{B0} to D_{B7} — Output (after 5 CLK + t_{pdM2} from Sampling) at CLK rising

■ TIMING CHART 4

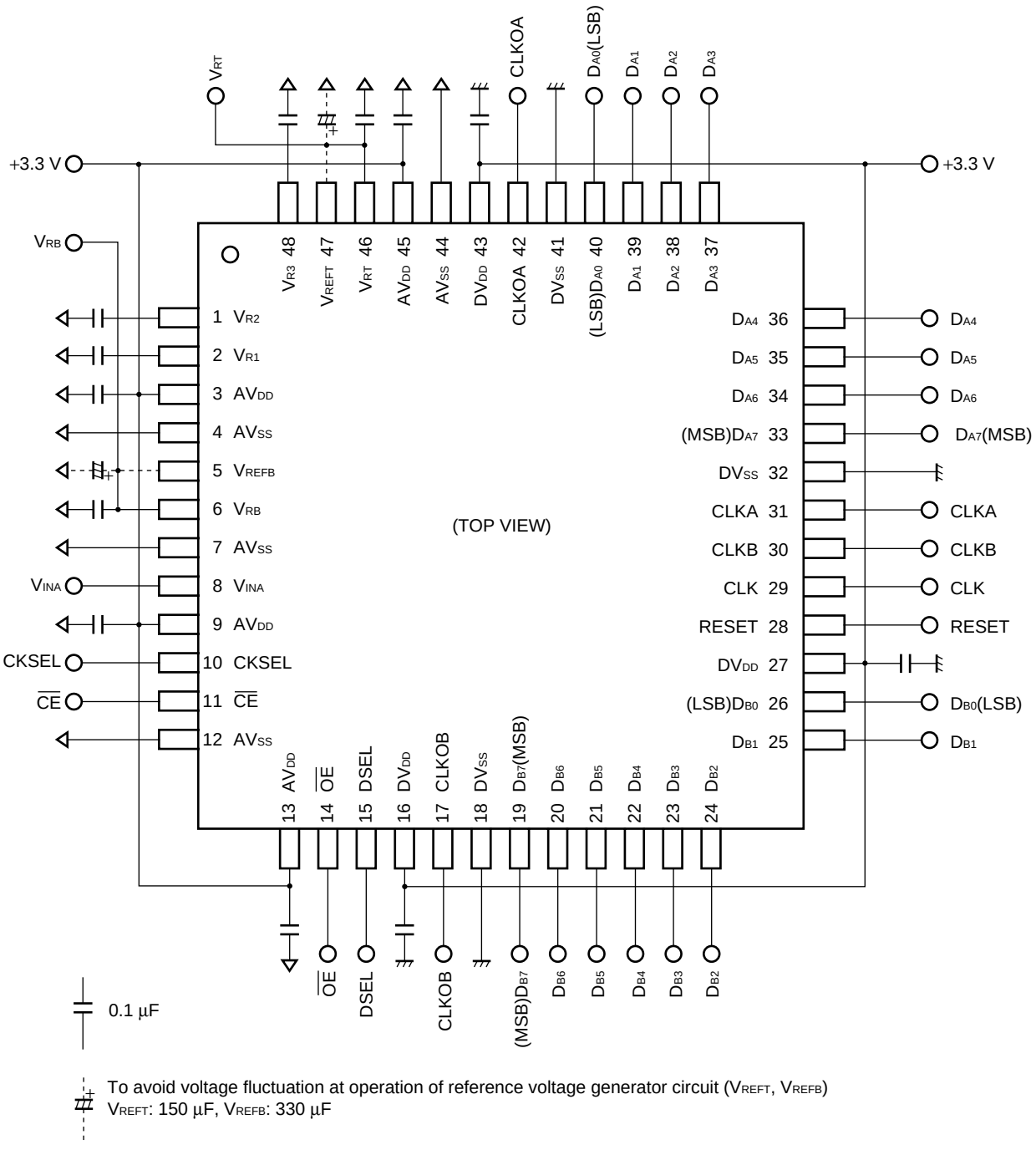
Two-phase CLK input mode (CLKA, CLKB)

- CLK = “L” (DV_{SS}) or “H” (DV_{DD})
- CLKA = CLKB = 50 MHz (max)
- CKSEL = “L” (AV_{SS})
- DSEL = “L” (DV_{SS})
- RESET = “H” (DV_{DD}) or “L” (DV_{SS})
- $\overline{CE}$ = “L” (AV_{SS})
- $\overline{OE}$ = “L” (DV_{SS})



- V_{INA} input — Sampling (A ch) at CLKA falling
  Sampling (B ch) at CLKB falling
- D_{A0} to D_{A7} — Output (after 2.5 CLK + t_{pdD} from Sampling) at CLKA rising
- D_{B0} to D_{B7} — Output (after 2.5 CLK + t_{pdD} from Sampling) at CLKB rising

■ TYPICAL CONNECTION EXAMPLE



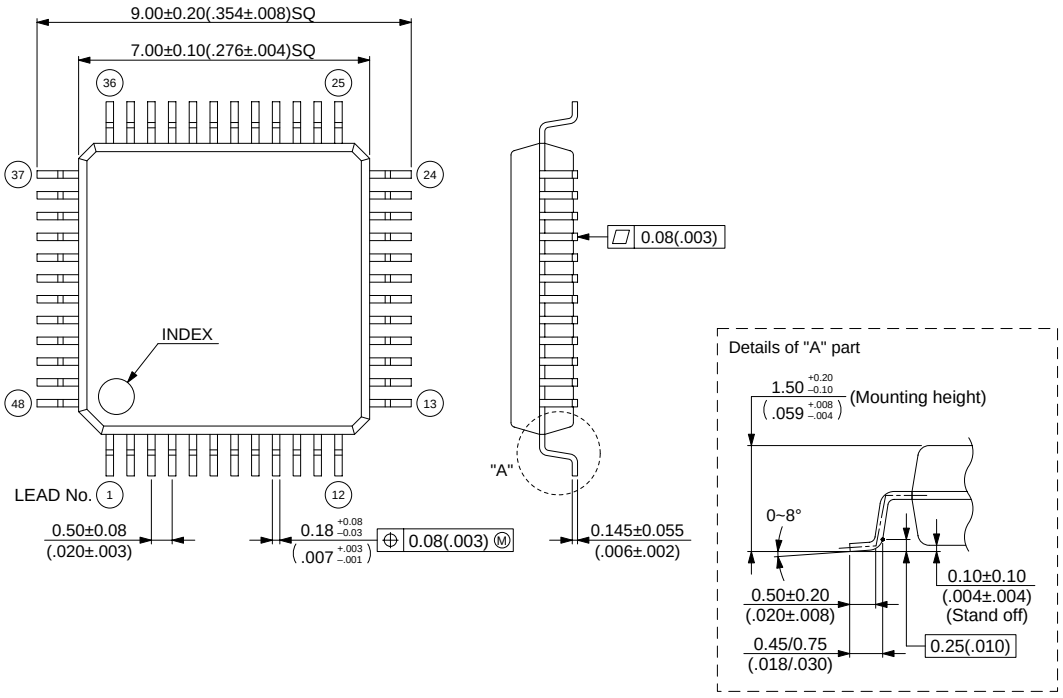
■ ORDERING INFORMATION

Part number	Package	Remark
MB40C328PFV	48-pin Plastic LQFP (FPT-48P-M05)	

■ PACKAGE DIMENSION

48-pin Plastic LQFP
(FPT-48P-M05)

Note) Pins width and pins thickness include plating thickness.



Dimensions in mm (inches).

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