

# ASSP For Video Applications

CMOS

## 3 ch 8-bit 162 MSPS A/D Converter

# MB40C338

### ■ DESCRIPTION

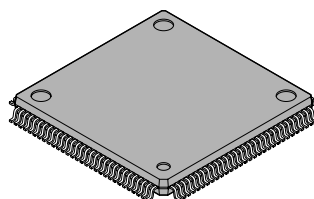
MB40C338 is a high-speed 3ch A/D converter using a fast CMOS technology.

### ■ FEATURES

- Resolution : 8 bit
- No. of AD channels : 3 ch
- Linearity error :  $\pm 0.40\%$  (typical)
- Maximum conversion rate : 162 MSPS (minimum)
- Power supply voltage : 3.3 V (typical : internal circuit)
- Digital input voltage range : TTL level
- Digital output voltage range : 3.3 V CMOS level
- Amp. input voltage range :  $0.7 V_{P-P}$  (typical)
- Amp. gain : 1.9 double fixed
- Power dissipation : 1100 mW (typical)
- Additional features : PLL circuit  
Video amp. circuit (1.9 double fixed gain)  
CLAMP circuit  
 $V_{RT}$  AMP circuit (RGB 3 ch common)  
 $V_{RB}$  AMP circuit (RGB 3 ch common)  
Overflow output  
High impedance output, power down function
- Package : LQFP120 (16 mm  $\times$  16mm, lead pitch : 0.5 mm)

### ■ PACKAGE

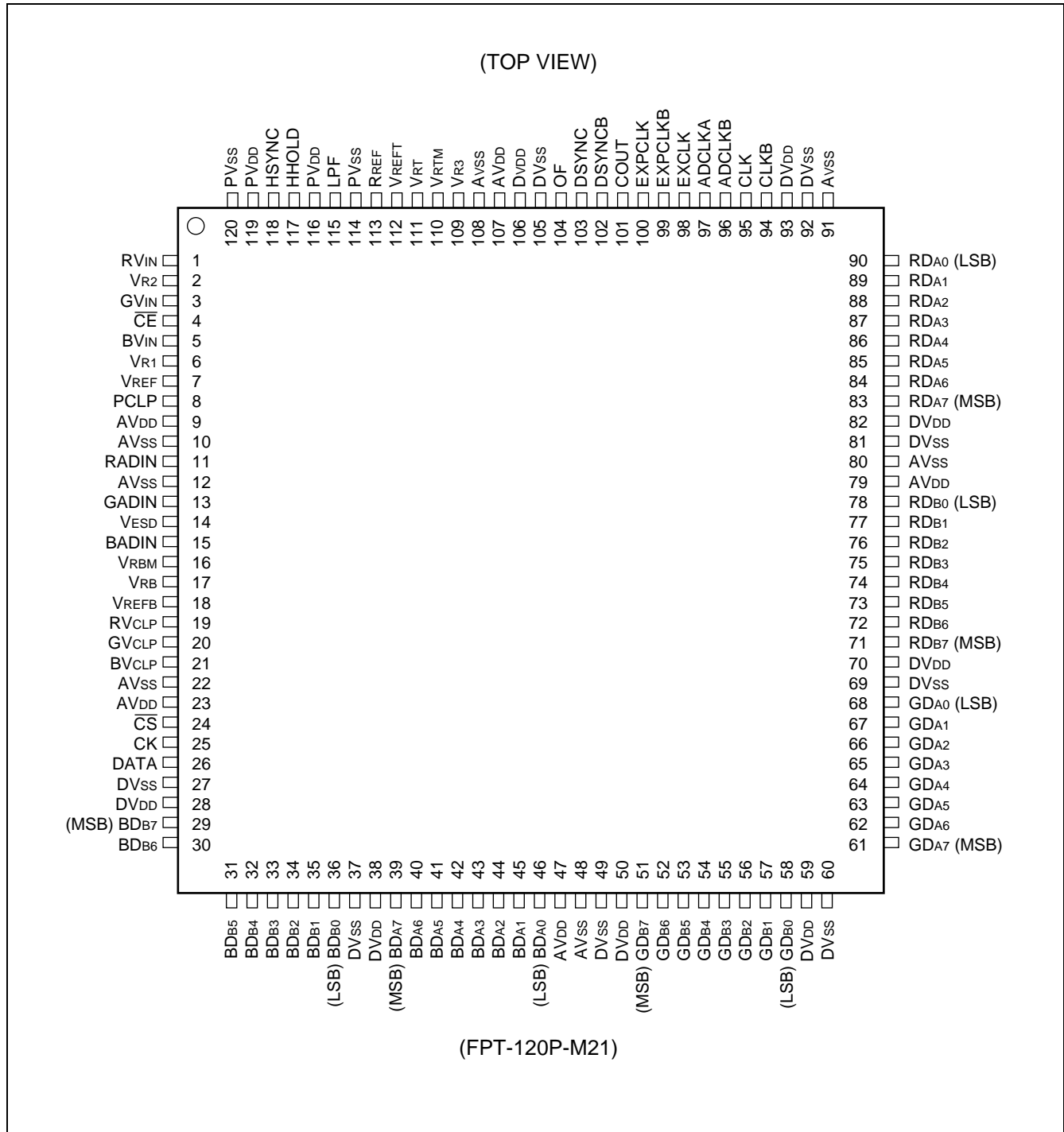
120-pin plastic LQFP



(FPT-120P-M21)

# MB40C338

## PIN ASSIGNMENT



## ■ PIN DESCRIPTION

Pin No.	Symbol	Description
9, 23, 47, 79, 107	AV <sub>DD</sub>	Analog power supply (+3.3 V)
28, 38, 50, 59, 70, 82, 93, 106	DV <sub>DD</sub>	Digital power supply (+3.3 V)
116, 119	PV <sub>DD</sub>	PLL Power supply pin (+3.3 V)
14	V <sub>ESD</sub>	Digital input power supply for protect device (+3.3 V or +5 V)
10, 12, 22, 48, 80, 91, 108	AV <sub>SS</sub>	Analog power supply ground pin (0 V)
27, 37, 49, 60, 69, 81, 92, 105	DV <sub>SS</sub>	Digital power supply ground pin (0 V)
114, 120	PV <sub>SS</sub>	PLL Power supply ground pin (0 V)
1 3 5	RV <sub>IN</sub> GV <sub>IN</sub> BV <sub>IN</sub>	1.9 double amp. input pin
11 13 15	RADIN GADIN BADIN	A/D converter input pin Please set these pins to open usually.
19 20 21	RV <sub>CLP</sub> GV <sub>CLP</sub> BV <sub>CLP</sub>	Clamp voltage setting input pin
110	V <sub>RTM</sub>	Reference voltage output pin on top side
111	V <sub>RT</sub>	Reference voltage input pin on top side
112	V <sub>REFT</sub>	Reference voltage generator output pin on top side
16	V <sub>RBM</sub>	Reference voltage output pin on bottom side
17	V <sub>RB</sub>	Reference voltage input pin on bottom side
18	V <sub>REFB</sub>	Reference voltage generator output pin on bottom side
6 2 109	V <sub>R1</sub> V <sub>R2</sub> V <sub>R3</sub>	Reference 1/4 voltage output pin (Add 0.1 μF for AV <sub>SS</sub> ) Reference 1/2 voltage output pin (Add 0.1 μF for AV <sub>SS</sub> ) Reference 3/4 voltage output pin (Add 0.1 μF for AV <sub>SS</sub> )
25	CK	Serial data transfer clock input pin
26	DATA	Serial data input pin
24	$\overline{CS}$	Chip select signal input pin It is possible to input to the shift register at $\overline{CS}$ falling The content of the shift register is executed at $\overline{CS}$ rising.
98	EXCLK	Clock input pin for A/D converter (CMOS level) Fix to "L" level when unused.

Note: The values in parentheses are standard.

(Continued)

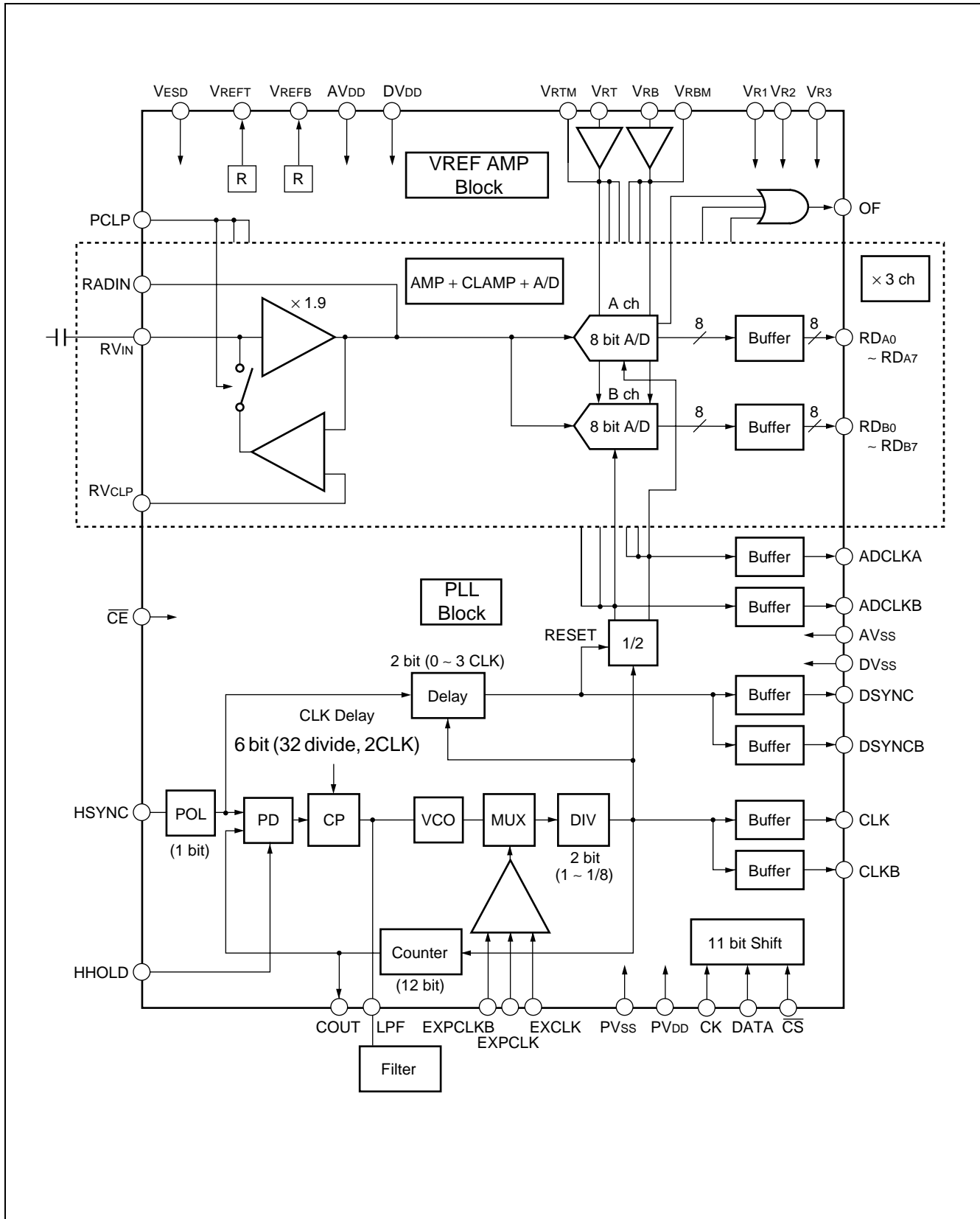
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Parameter	Symbol	Description
99	EXPCLKB	Differential clock (negative-phase) input pin for A/D converter Fix to "H" level when unused.
100	EXPCLK	Differential clock (positive-phase) input pin for A/D converter Fix to "L" level when unused.
		PECL level
8	PCLP	Clamp pulse input pin
4	$\overline{CE}$	Power down at $\overline{CE}$ input "H" (internal pull-up resistor)
113	R <sub>REF</sub>	Internal current setting pin (Add 12 k $\Omega$ for AV <sub>ss</sub> )
103	DSYNC	Delay sync signal output pin
102	DSYNCB	Inverted delay sync signal output pin
95	CLK	Clock output pin (See "■ TIMING DIAGRAM".)
94	CLKB	
97	ADCLKA	
96	ADCLKB	
83 to 90 61 to 68 39 to 46	RD <sub>A7</sub> to RD <sub>A0</sub> GD <sub>A7</sub> to GD <sub>A0</sub> BD <sub>A7</sub> to BD <sub>A0</sub>	Digital output pin (Port A) RD <sub>A7</sub> , GD <sub>A7</sub> , BD <sub>A7</sub> : MSB RD <sub>A0</sub> , GD <sub>A0</sub> , BD <sub>A0</sub> : LSB
71 to 78 51 to 58 29 to 36	RD <sub>B7</sub> to RD <sub>B0</sub> GD <sub>B7</sub> to GD <sub>B0</sub> BD <sub>B7</sub> to BD <sub>B0</sub>	Digital output pin (Port B) RD <sub>B7</sub> , GD <sub>B7</sub> , BD <sub>B7</sub> : MSB RD <sub>B0</sub> , GD <sub>B0</sub> , BD <sub>B0</sub> : LSB
101	COUT	PLL counter output pin
115	LPF	External capacitor/resistor connection pin
117	HHOLD	Phase detector operation is hold by input "H" level
118	HSYNC	Horizontal sync signal input pin
7	V <sub>REF</sub>	Internal voltage output pin (Add 3.3 $\mu$ F for AV <sub>ss</sub> )
104	OF	Overflow output pin ("H" level output at overflow)

Note: The values in parentheses are standard.

## ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Power supply voltage	AV <sub>DD</sub> , DV <sub>DD</sub> , PV <sub>DD</sub>	-0.3	+4.0	V
	V <sub>ESD</sub>	-0.3	+7.0	V
Input/output voltage	RV <sub>IN</sub> , GV <sub>IN</sub> , BV <sub>IN</sub> , RADIN, GADIN, BADIN, RV <sub>CLP</sub> , GV <sub>CLP</sub> , BV <sub>CLP</sub> , V <sub>RT</sub> , V <sub>RTM</sub> , V <sub>REFT</sub> , V <sub>RB</sub> , V <sub>RBM</sub> , V <sub>REFB</sub> , V <sub>R1</sub> , V <sub>R2</sub> , V <sub>R3</sub> V <sub>REF</sub> , R <sub>REF</sub>	-0.3	AV <sub>DD</sub> +0.3*1	V
	RD <sub>A0</sub> to RD <sub>A7</sub> , RD <sub>B0</sub> to RD <sub>B7</sub> , GD <sub>A0</sub> to GD <sub>A7</sub> , GD <sub>B0</sub> to GD <sub>B7</sub> , BD <sub>A0</sub> to BD <sub>A7</sub> , BD <sub>B0</sub> to BD <sub>B7</sub> , DSYNC, DSYNCB, OF, COUT, CLK, CLKB, ADCLKA, ADCLKB	-0.3	DV <sub>DD</sub> +0.3*1	V
	LPF	-0.3	PV <sub>DD</sub> +0.3*1	V
	CK, DATA, $\overline{CS}$ , EXPCLKB, EXPCLK, PCLP, $\overline{CE}$ , EXCLK, HHOLD, HSYNC	-0.3	V <sub>ESD</sub> +0.3*2	V
Storage temperature	T <sub>STG</sub>	-55	+125	°C

\*1 : Do not exceed +4.0 V.

\*2 : Do not exceed +7.0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Rating			Unit
		Min.	Typ.	Max.	
Power supply voltage	$AV_{DD}, DV_{DD}$	3.00	3.30	3.60	V
	$PV_{DD}$	3.00	3.30	3.60	V
	$V_{ESD}$	3.00	—	5.25	V
A/D converter input voltage	$V_{ADIN}$	$V_{RB}$	—	$V_{RT}$	V
Analog reference voltage: T	$V_{RT}$	—	2.2	$AV_{DD} - 0.6$	V
Analog reference voltage: B	$V_{RB}$	0.6	0.7	—	V
Analog reference voltage range	$V_{RT} - V_{RB}$	1.0	1.5	1.8	V
Video AMP input voltage	$V_{IN (P-P)}$	0.5	—	0.9	$V_{P-P}$
Clamp input voltage	$V_{CLP}$	0.6	$V_{RB}$	1.7	V
Digital “H” level input voltage	$V_{IHD}$	2.5	—	$V_{ESD}$	V
Digital “L” level input voltage	$V_{ILD}$	0	—	0.5	V
Digital “H” level output current	$I_{OHD}$	–400	—	—	$\mu A$
Digital “L” level output current	$I_{OLD}$	—	—	1.6	mA
PLL counter	$P_C$	100	—	4095	—
HSYNC input frequency range	$f_{HSYNC}$	10	—	100	kHz
HHOLD set up time	$t_{SHHOLD}$	20	—	—	ns
HHOLD hold time	$t_{HHHOLD}$	20	—	—	ns
Clamp pulse width	$t_{WCLP}$	0.5	—	—	$\mu s$
CK clock pulse width	$t_{WCKL}, t_{WCKH}$	100	—	—	ns
DATA set up time	$t_{SDATA}$	30	—	—	ns
DATA hold time	$t_{HDATA}$	30	—	—	ns
$\overline{CS}$ set up time	$t_{SCS}$	50	—	—	ns
$\overline{CS}$ hold time	$t_{HCS}$	50	—	—	ns
$\overline{CS}$ “H” level hold time	$t_{WCSH}$	100	—	—	ns
Operating temperature range	$T_a$	–20	—	70	$^{\circ}C$

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

# MB40C338

## ■ ELECTRICAL CHARACTERISTICS

### 1. DC Characteristics in Analog Section

- Power supply current ( $AV_{DD} = DV_{DD} = PV_{DD} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{ESD} = 3.0\text{ V to }5.25\text{ V}$ ,  $T_a = -20\text{ }^\circ\text{C to }+70\text{ }^\circ\text{C}$ )

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Analog power supply current	$I_{DD}$	—	220	310	mA
Digital power supply current	$I_{DD}$	—	100	110	mA
Power supply current PLL section (@ $f_{VCOH} = 162\text{ MHz}$ , $I_{CP} = 0.5\text{ mA}$ , $DIV = 1/1$ )	$I_{DD}$	—	16	20	mA
Standby current	$I_{SB}$	—	10	—	mA

- A/D Block ( $AV_{DD} = DV_{DD} = PV_{DD} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{ESD} = 3.0\text{ V to }5.25\text{ V}$ ,  $T_a = -20\text{ }^\circ\text{C to }+70\text{ }^\circ\text{C}$ )

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Resolution	—	—	8	—	bit
Linearity error (DC Accuracy)	LE	-0.8	$\pm 0.4$	+0.8	%
Differential linearity error (DC Accuracy)	DLE	-0.36	$\pm 0.2$	+0.65	%
Reference voltage : T	$V_{REFT}$	$0.63 \times AV_{DD}$	$0.67 \times AV_{DD}$	$0.70 \times AV_{DD}$	V
Reference voltage : B	$V_{REFB}$	$0.18 \times AV_{DD}$	$0.21 \times AV_{DD}$	$0.24 \times AV_{DD}$	V
Analog reference voltage input current	$I_{RT}, I_{RB}$	—	5	20	$\mu\text{A}$

- Video AMP Block ( $AV_{DD} = DV_{DD} = PV_{DD} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{ESD} = 3.0\text{ V to }5.25\text{ V}$ ,  $T_a = -20\text{ }^\circ\text{C to }+70\text{ }^\circ\text{C}$ )

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Video AMP gain	$G_{AMP}$	1.8	1.9	2.0	—
Video AMP output voltage range	$V_{AMP\text{OUT}}$	0.5	—	$AV_{DD} - 0.6$	V
Video AMP frequency width	BW	—	250	—	MHz
Video AMP input capacity	$C_{VIN}$	—	5	—	pF

- CLAMP Block ( $AV_{DD} = DV_{DD} = PV_{DD} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{ESD} = 3.0\text{ V to }5.25\text{ V}$ ,  $T_a = -20\text{ }^\circ\text{C to }+70\text{ }^\circ\text{C}$ )

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
$V_{CLP}$ input current	$I_{CLP}$	—	5	20	$\mu\text{A}$
Clamp voltage	$V_{CLAMP}$	$V_{CLP} - 0.1$	$V_{CLP}$	$V_{CLP} + 0.1$	V

- PLL Block ( $AV_{DD} = DV_{DD} = PV_{DD} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{ESD} = 3.0\text{ V to }5.25\text{ V}$ ,  $T_a = -20\text{ }^\circ\text{C to }+70\text{ }^\circ\text{C}$ )

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
CLK jitter (@ $f_{HSYNC} = 79.98\text{ kHz}$ , $f_{CLK} = 135.0\text{ MHz}$ )	$P_{ij}$	—	1.0	1.5	ns



## 2. DC Characteristic in Digital Section

( $A_{VDD} = DV_{DD} = PV_{DD} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{ESD} = 3.0\text{ V to }5.25\text{ V}$ ,  $T_a = -20\text{ }^\circ\text{C to }+70\text{ }^\circ\text{C}$ )

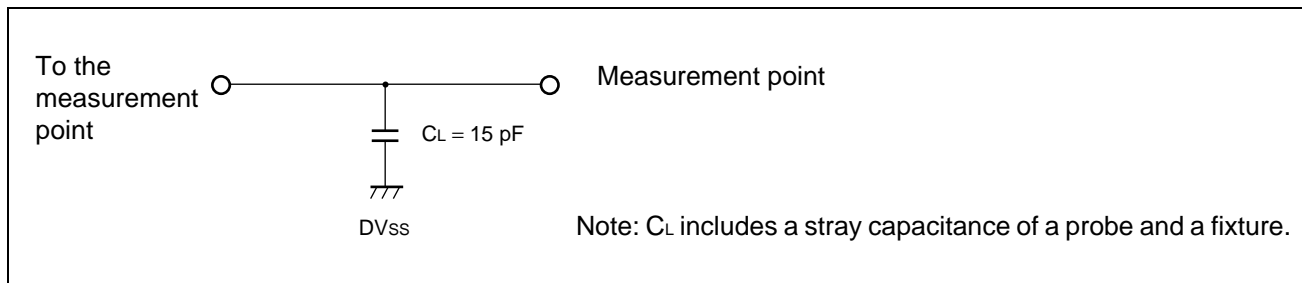
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Digital input current	$I_{ID}$	-20	—	5	$\mu\text{A}$
Digital "H" level output voltage	$V_{OHD}$	$DV_{DD} - 0.4$	—	—	V
Digital "L" level output voltage	$V_{OLD}$	—	—	0.4	V

## 3. Switching Characteristics

( $A_{VDD} = DV_{DD} = PV_{DD} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{ESD} = 3.0\text{ V to }5.25\text{ V}$ ,  $T_a = -20\text{ }^\circ\text{C to }+70\text{ }^\circ\text{C}$ )

Parameter	Symbol	Value			Unit	
		Min.	Typ.	Max.		
A/D Maximum conversion rate	$f_s$	162	—	—	MSPS	
Aperture time	$t_{AD}$	—	1.5	—	ns	
VCO oscillation frequency	VCOL	$f_{VCOL}$	75	—	140	MHz
	VCOH	$f_{VCOH}$	85	—	162	MHz
CLK output delay time	$t_{pd}(\text{HSYNC-CLK})$	1.0	2.0	4.0	ns	
Digital output delay time	$t_{pd}(\text{CLK-ADCLK2})$	0.0	1.0	2.0	ns	
	$t_{pd}(\text{CLK-DATA2})$	2.5	4.0	6.0	ns	
DSYNC output delay time	$t_{pd}(\text{CLK-DSYNC})$	0.5	1.5	2.0	ns	

### ■ DIGITAL OUTPUT BUFFER LOAD CIRCUIT



### ■ MODE SETTING

Symbol	Setting	Mode
$\overline{CE}$	H	All function power OFF
	L	Operation mode

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## ■ SERIAL DATA SETTING (MSB FAST)

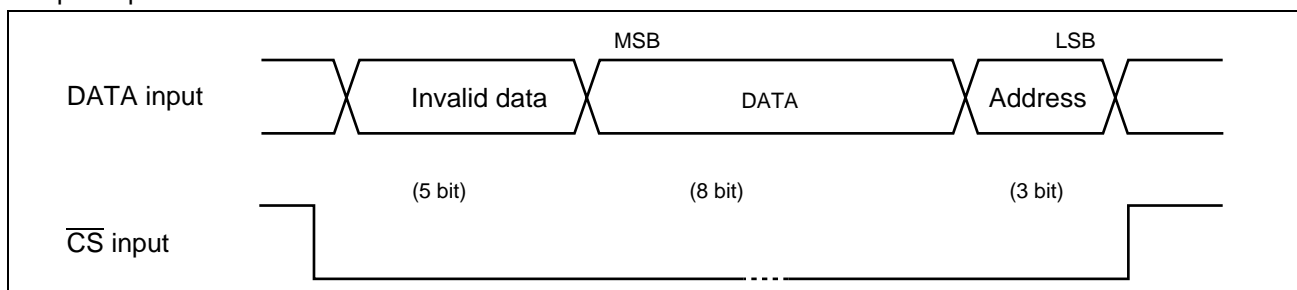
RES	(Address)			(Data)								Function			
	LSB		MSB	D0	D1	D2	D3	D4	D5	D6	D7		D8	D9	D10
1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	Counter low ranking 8 bit
2	0	1	0	0	0	0	0	0	0	X	X	X	X		Counter high ranking 4 bit
3	1	1	0	0	0	0	0	0	0	0	0	0	1	0	CLK DELAY adjust*1 : $t_d = N / (32 \times f_{CLK})$
	1	1	0	0	0	0	0	0	0	0	0	0	1	0	HSYNC polarity : 0 = through, 1 = inversion
	1	1	0	0	0	0	0	0	0	0	0	0	1	0	A/D converter output : 0 = operation, 1 = high impedance
4	0	0	1	0	0	0	0	0	0	0	0	0	1	0	CLK output : 0 = on, 1 = "L"
	0	0	1	0	0	0	0	0	0	0	0	0	1	0	CLKB output : 0 = on, 1 = "L"
	0	0	1	0	0	0	0	0	0	0	0	0	1	0	DSYNC output : 0 = on, 1 = "L"
	0	0	1	0	0	0	0	0	0	0	0	0	1	0	DSYNCB output : 0 = on, 1 = "L"
	0	0	1	0	0	0	0	0	0	0	0	0	1	0	ADCLKA output : 0 = on, 1 = "L"
	0	0	1	0	0	0	0	0	0	0	0	0	1	0	ADCLKB output : 0 = on, 1 = "L"
	0	0	1	0	0	0	0	0	0	0	0	0	1	0	DSYNC delay*2 : 0, 1, 2, 3
5	1	0	1	0	0	0	0	0	0	0	0	0	1	0	CLK change : 0 = VCO, 1 = External clock
	1	0	1	0	0	0	0	0	0	0	0	0	1	0	External clock input : 0 = CMOS, 1 = PECL
	1	0	1	0	0	0	0	0	0	0	0	0	1	0	Counter operation : 0 = on, 1 = off
	1	0	1	0	0	0	0	0	0	0	0	0	1	0	Charge pump current*3 : 0.1 mA, 0.5 mA, 1 mA
	1	0	1	0	0	0	0	0	0	0	0	0	1	0	VCO select : 0 = VCOL, 1 = VCOH
	1	0	1	0	0	0	0	0	0	0	0	0	1	0	Divider setting*4 : 1, 1/2, 1/4, 1/8 × 1

\*1 : Setting at 6bit, Resolution :  $1/32 \times CLK$ , Setting range : 0 to  $63/32 \times CLK$

\*2, \*3, \*4 : See under table

Setting	0 (0, 0)	1 (1, 0)	2 (0, 1)	3 (1, 1)
DSYNC delay*2	0 CLK	1 CLK	2 CLK	3 CLK
Charge pump current*3	0.1 mA	0.5 mA	1.0 mA	—
Divider setting*4	1/1	1/2	1/4	1/8

Example: input at 16 bit



## ■ RECOMMENDED VALUE OF SERIAL DATA SETTING

	f <sub>CLK</sub> (MHz)	f <sub>HSYNC</sub> (kHz)	Counter	I <sub>CP</sub> (mA)	VCO select	Divider	f <sub>VCO</sub> (MHz)
UXGA	162.000	75.000	2160	0.5	VCOH	1/1	162.000
SXGA	157.500	91.146	1728	0.5	VCOH	1/1	157.500
	135.000	81.130	1664	0.5	VCOH or VCOL	1/1	135.000
	108.000	64.904	1664	0.5	VCOH or VCOL	1/1	108.000
XGA	94.500	68.677	1376	0.5	VCOH or VCOL	1/1	94.500
	78.750	60.023	1312	0.5	VCOL	1/1	78.750
	75.000	56.476	1328	0.5	VCOH	1/2	150.000
	65.000	48.363	1344	0.5	VCOH or VCOL	1/2	130.000
SVGA	56.250	53.674	1048	0.5	VCOH or VCOL	1/2	112.500
	50.000	48.077	1040	0.5	VCOH or VCOL	1/2	100.000
	49.500	46.875	1056	0.5	VCOH or VCOL	1/2	99.000
	40.000	37.879	1056	0.5	VCOL	1/2	80.000
VGA	36.000	43.269	832	0.5	VCOH	1/4	144.000
	31.500	37.861	832	0.5	VCOH or VCOL	1/4	126.000
	25.175	31.469	800	0.5	VCOH or VCOL	1/4	100.700
	25.149	31.436	800	0.5	VCOH or VCOL	1/4	100.596
PAL	29.375	15.625	1880	0.5	VCOH or VCOL	1/4	117.500
	22.031	15.625	1410	0.5	VCOH or VCOL	1/4	88.125
	14.688	15.625	940	0.5	VCOH or VCOL	1/8	117.500
NTSC	24.545	15.734	1560	0.5	VCOH or VCOL	1/4	98.180
	18.409	15.734	1170	0.5	VCOH	1/8	147.270
	12.273	15.734	780	0.5	VCOH or VCOL	1/8	98.180

VCO select : VCOH (f<sub>VCO</sub> = 85 MHz to 162 MHz)

VCOL (f<sub>VCO</sub> = 75 MHz to 140 MHz)

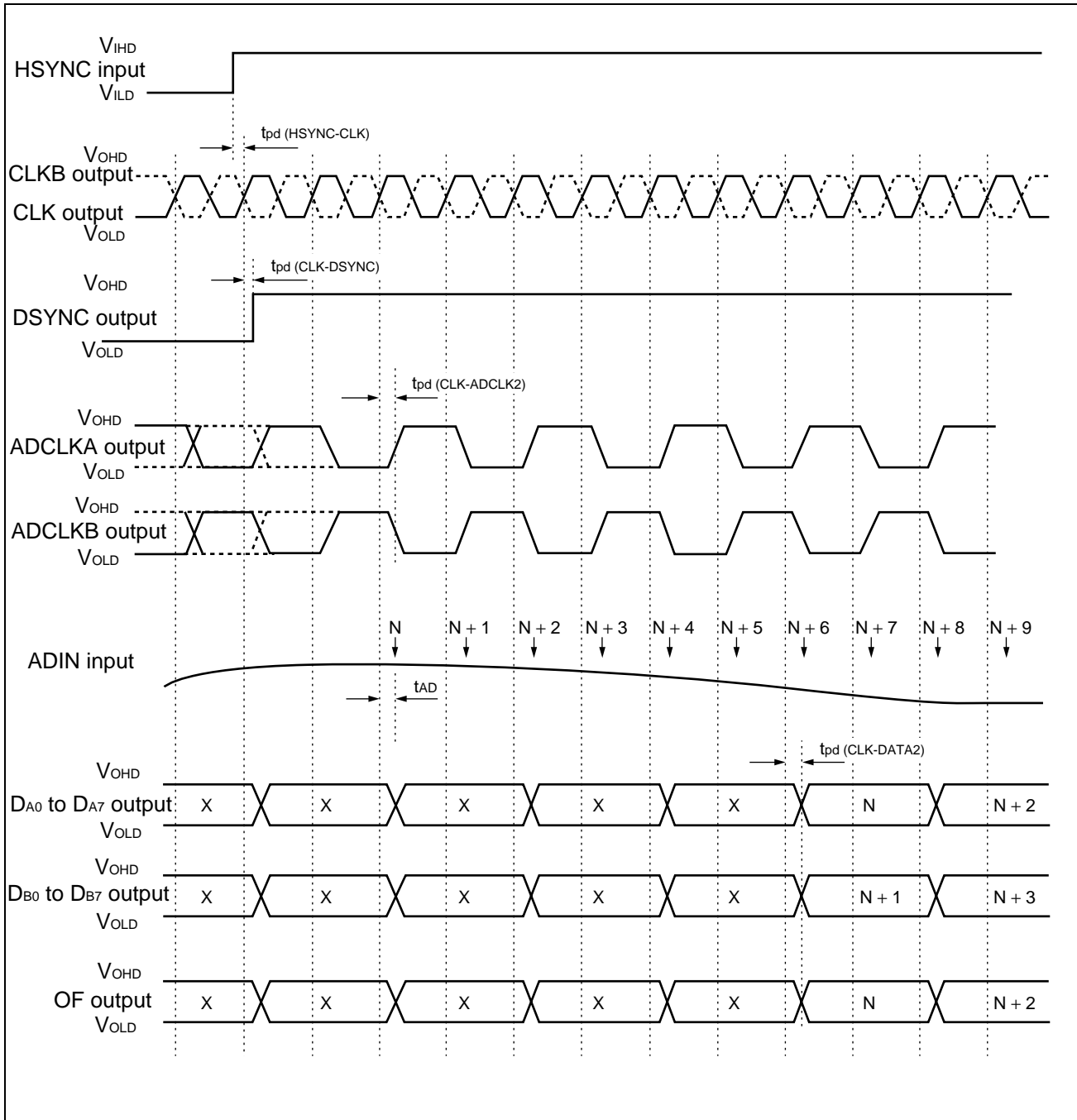
$$f_{CLK} = f_{HSYNC} \times \text{Counter}$$

$$f_{VCO} = f_{HSYNC} \times \text{Counter/Divider}$$

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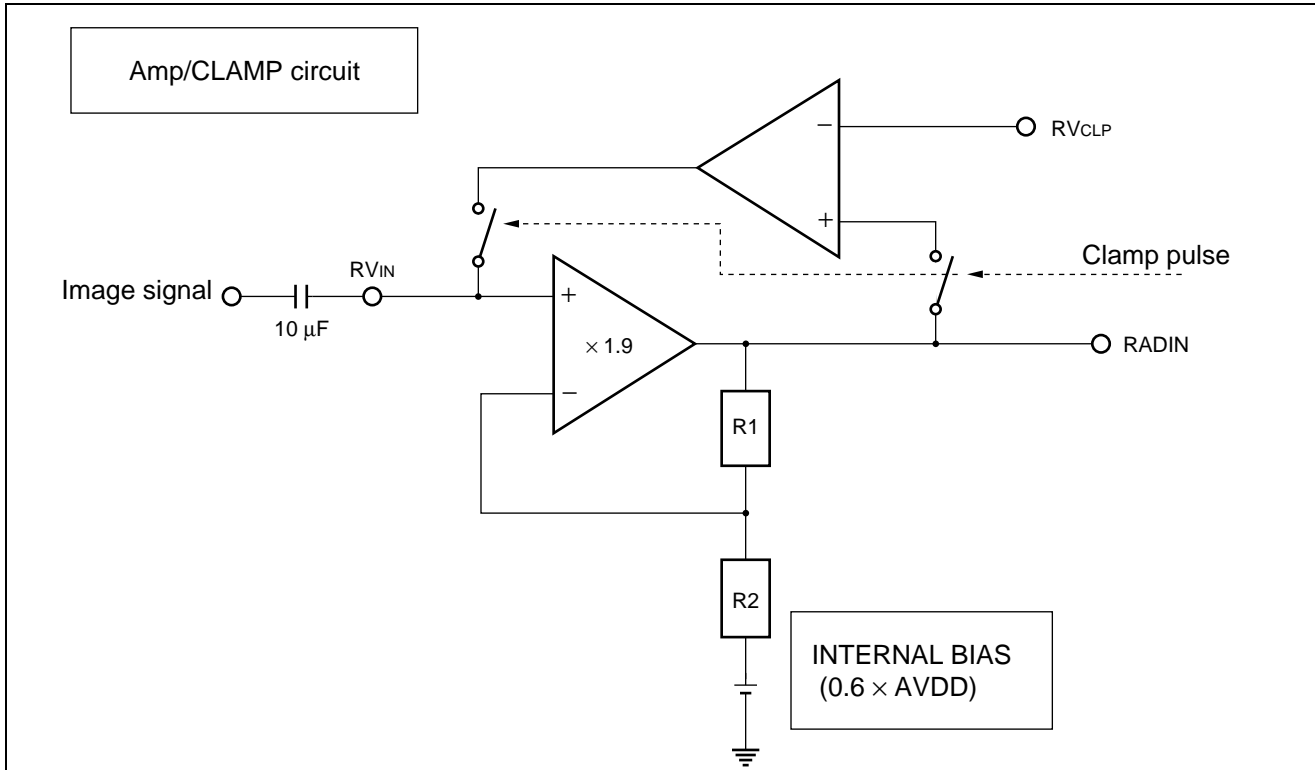
## TIMING DIAGRAM

- Demultiplex Output (in-phase) Mode

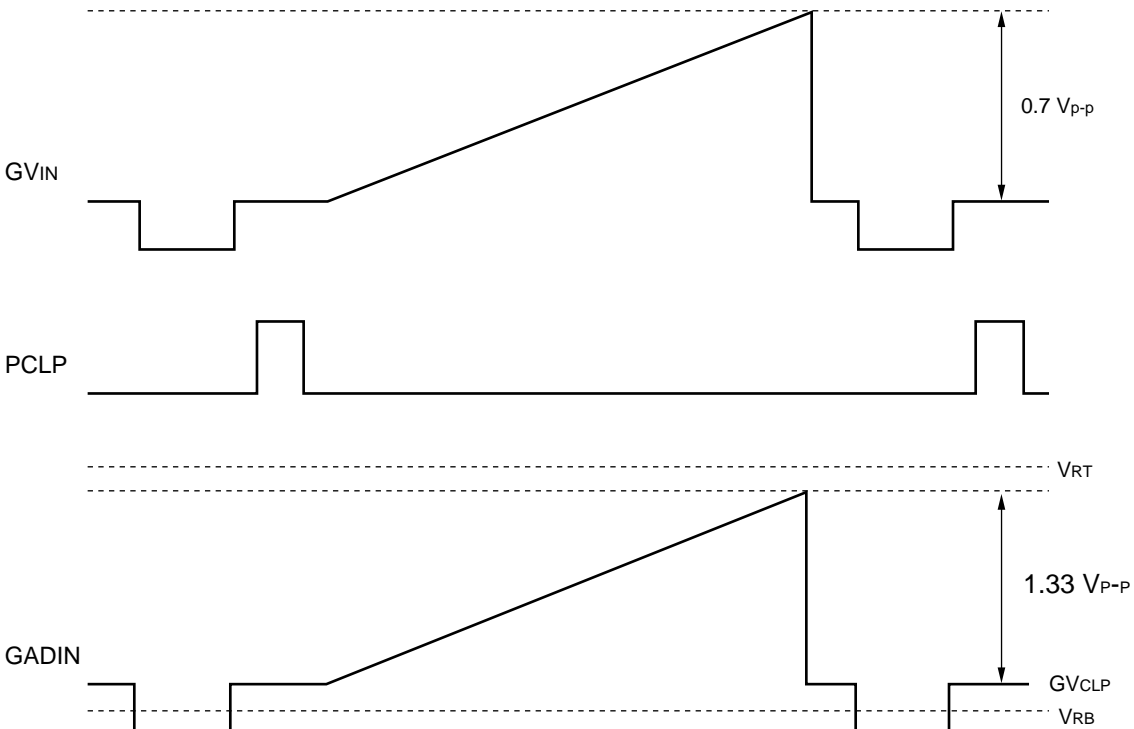


- ADIN input: Sampling at CLK rising (at CLKB falling)
- DA0 to DA7: Output (after  $6 \text{ CLK} + t_{pd}(\text{CLK-DATA2})$  from sampling) at CLK rising (at CLKB falling)
- DB0 to DB7: Output (after  $5 \text{ CLK} + t_{pd}(\text{CLK-DATA2})$  from sampling) at CLK rising (at CLKB falling)

## CLAMP and AMP OPERATION

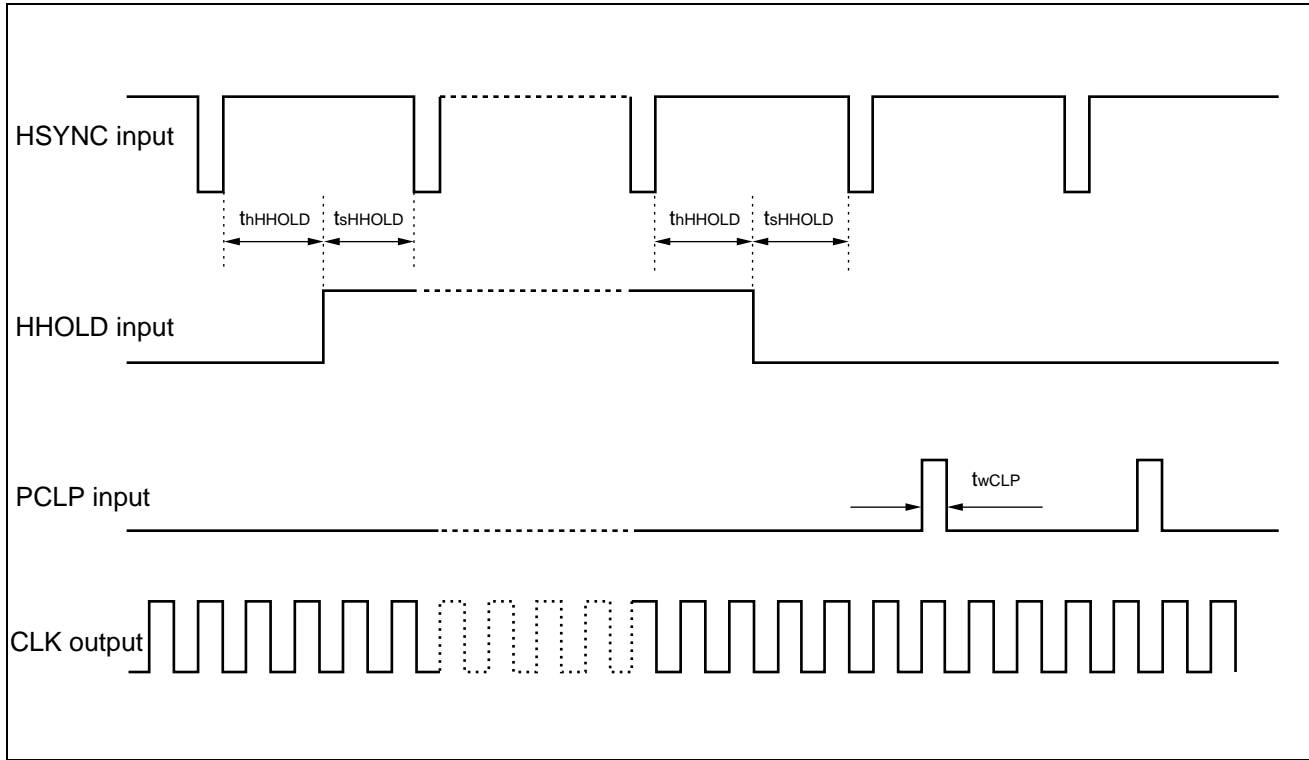


< For example, Sync on G signal input >

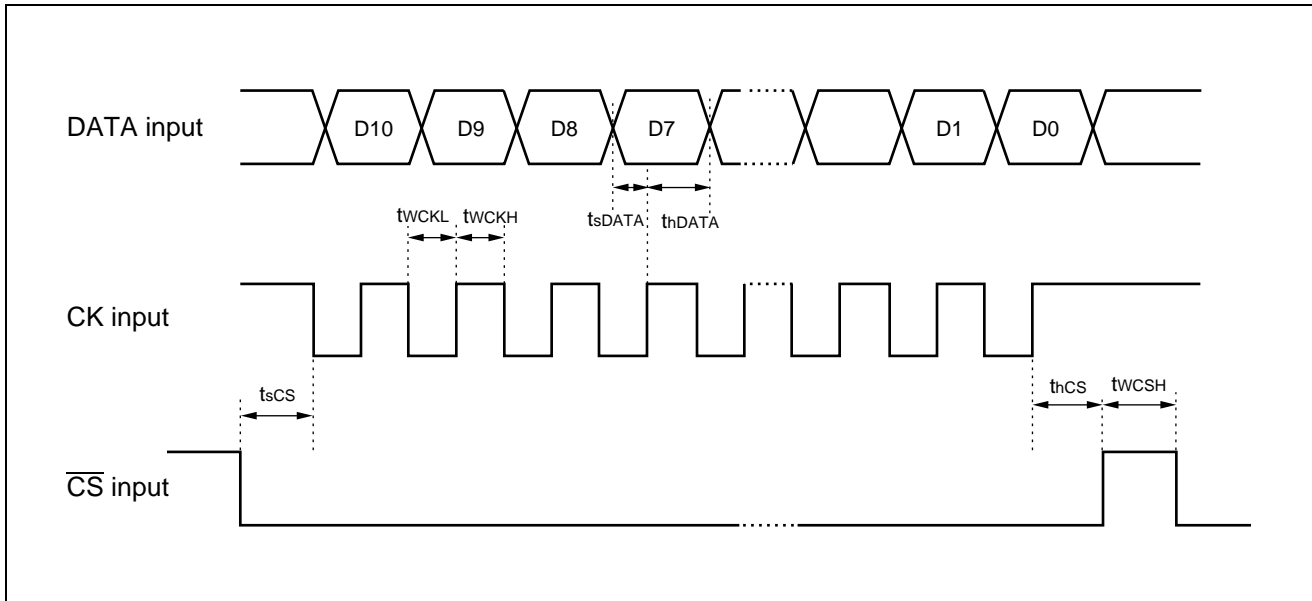


Contrast adjust : controlling the voltage difference between  $V_{RT}$  and  $V_{RB}$  (typ :  $V_{RT} - V_{RB} = 1.33 \text{ V}$ )  
 Brightness adjust : controlling the voltage difference between  $V_{CLP}$  and  $V_{RB}$  (typ :  $V_{CLP} = V_{RB}$ )

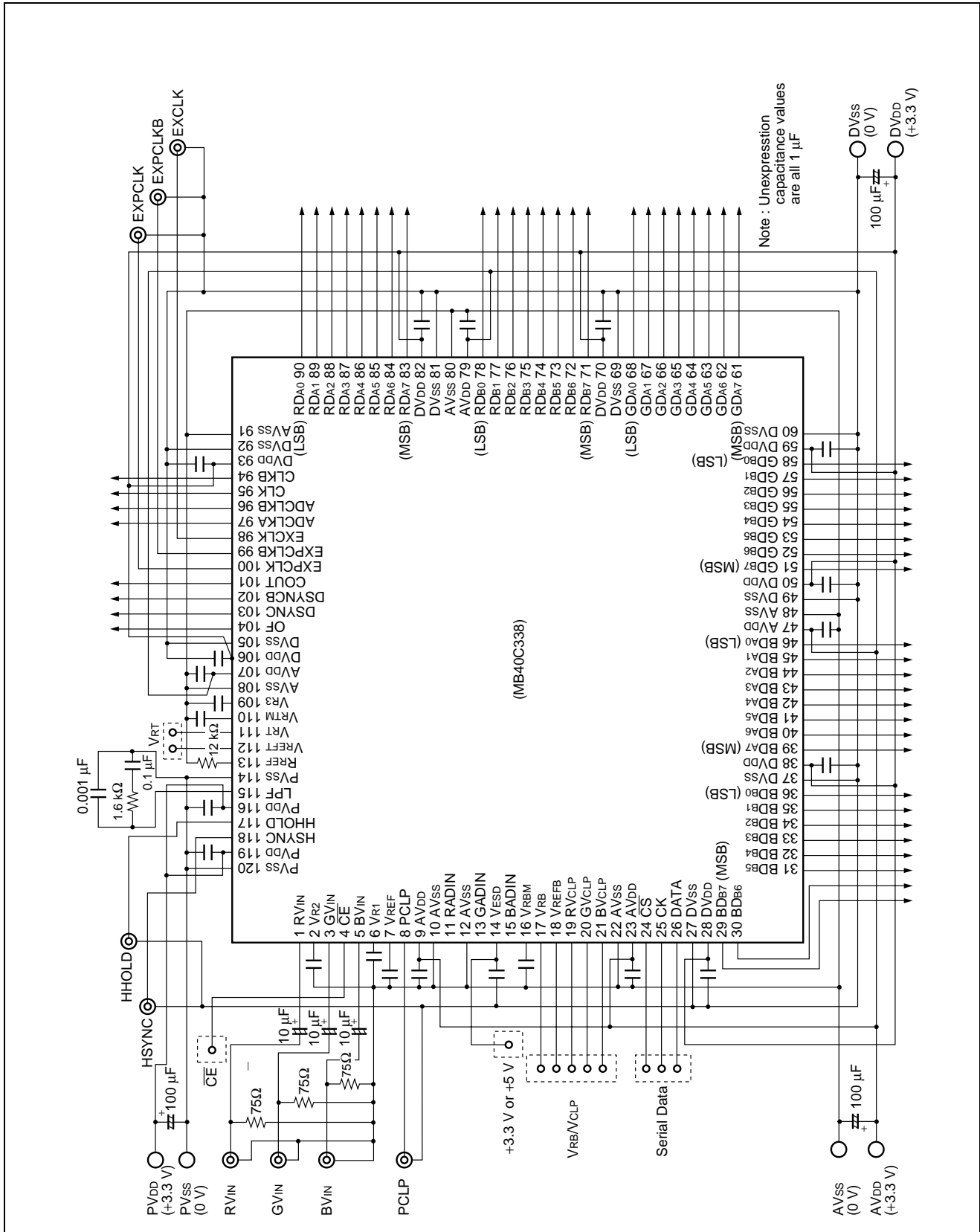
## CLAMP SIGNAL and HOLD SIGNAL



## SERIAL DATA TRANSFER TIMING



## TYPICAL APPLICATION



# MB40C338

## ■ USAGE PRECAUTIONS

Be sure to ground the pins of AV<sub>DD</sub>, DV<sub>DD</sub>, PV<sub>DD</sub>, V<sub>ESD</sub>, V<sub>RTM</sub>, V<sub>RBM</sub>, V<sub>R1</sub>, V<sub>R2</sub>, V<sub>R3</sub> and V<sub>REF</sub> via high-frequency capacitor.

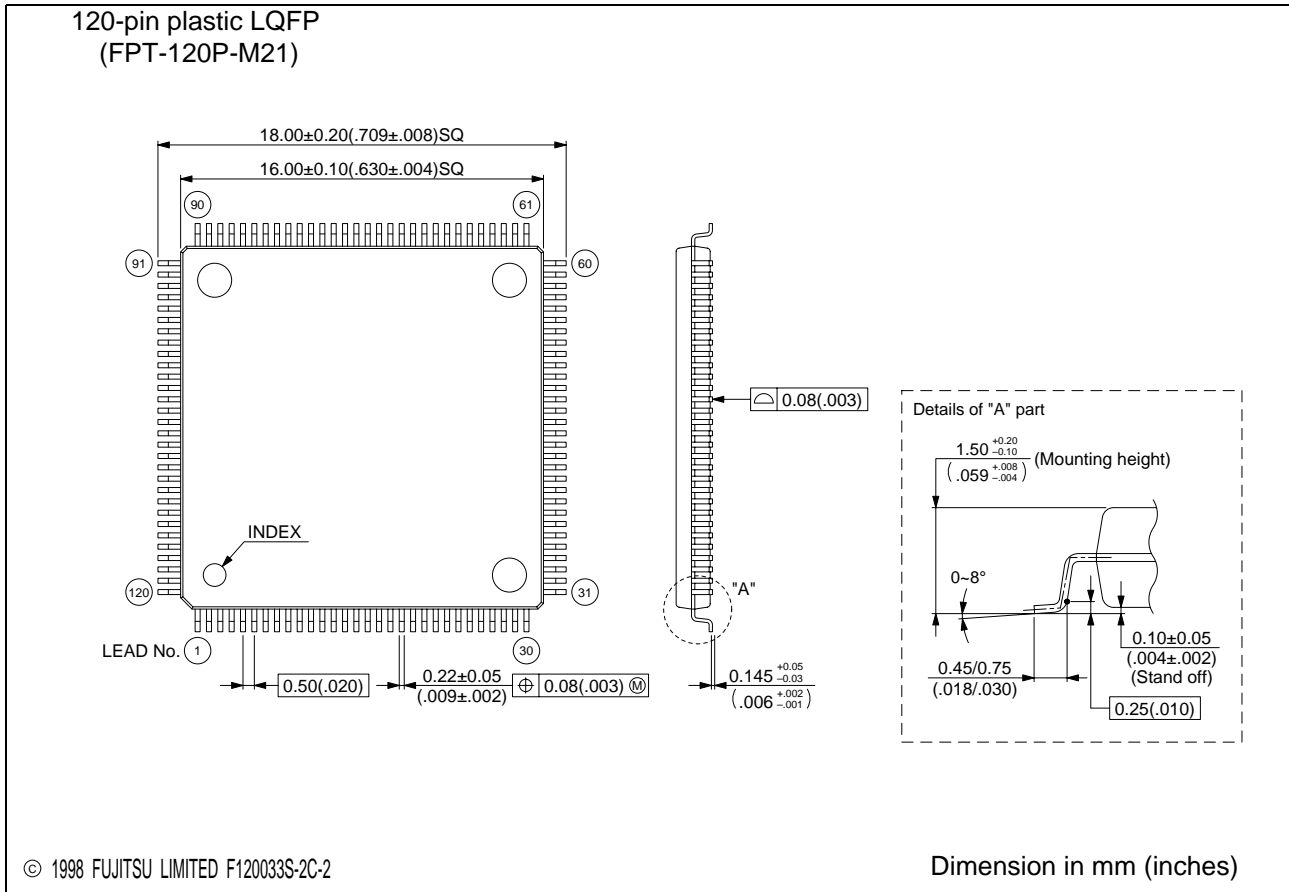
Place the high-frequency capacitor as close as possible to the pin.

## ■ ORDERING INFORMATION

Part number	Package	Remark
MB40C338PFV	120-pin plastic LQFP (FPT-120P-M21)	



## ■ PACKAGE DIMENSION



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