

General Purpose Linear IC's General Purpose Converters

CMOS

D/A Converter for Digital Tuning

(With Built-in OP Amp and I/O Expander)

MB88141

■ DESCRIPTION

The FUJITSU MB88141 is a D/A converter with 12 built-in channels.

The 12 analog output channels have built-in OP Amps, providing large current drive capability.

Data input is compatible with I²C specifications, and is controlled by two control lines.

The built-in I/O expander function allows the MB88141 to be controlled by devices incompatible with I²C bus specifications (provides conversion between I²C serial and 8- or 4-bit parallel I/O).

Can be adapted for tuning by electronically variable or pre-fixed resistance, etc.

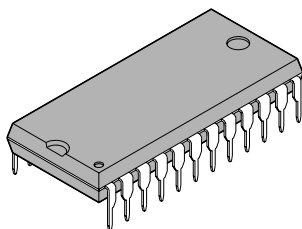
■ FEATURES

- Ultra-low power consumption (0.9 mW/channel Typ.)
- Ultra-compact package
- Built-in 12-channel R-2R type 8-bit D/A converter
- Built-in analog output amplifier (maximum sink current 1.0 mA, maximum source current 1.0 mA)
- Analog output range 0 V to V_{cc}

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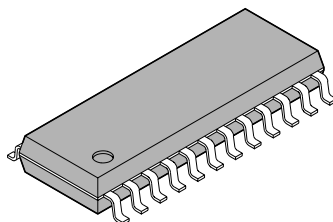
■ PACKAGES

24-pin plastic DIP



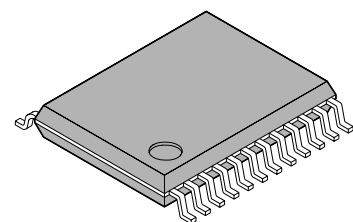
(DIP-24P-M02)

24-pin plastic SOP



(FPT-24P-M01)

24-pin plastic SSOP



(FPT-24P-M03)

"Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips."

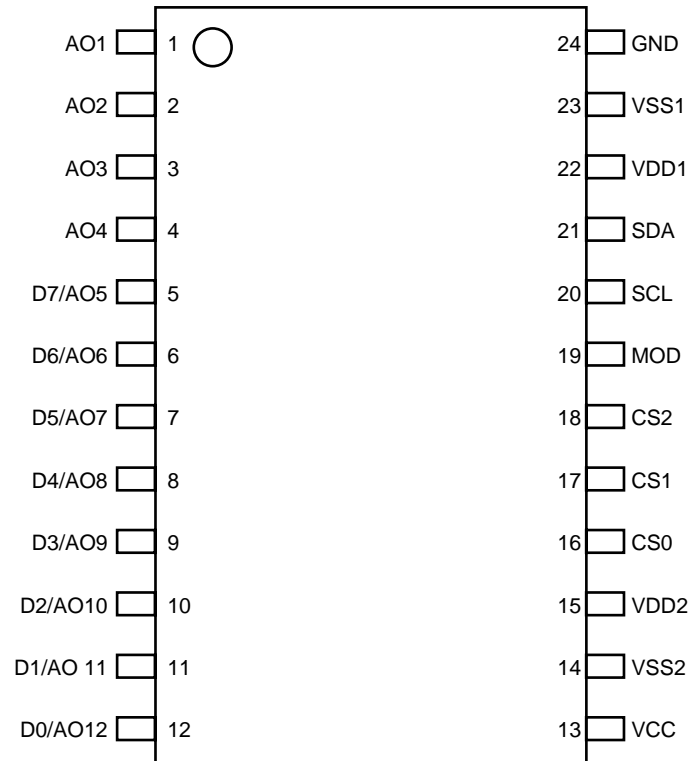
MB88141

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- 5 V single power supply
- Power supply/GND for MCU interface and OP Amp is separate from power supply/GND for D/A converter
- Power supply for D/A converter is divided into two systems for V_{DD1}/V_{SS1} (AO₁ to AO₄) and V_{DD2}/V_{SS2} (AO₅ to AO₁₂), allowing separate level settings for each system
- Compatible with serial data input, I²C specifications
- Built-in I/O expander function (converts between I²C serial and 8- or 4-bit parallel)
- CMOS process
- Packages: DIP 24-pin, SOP 24-pin, SSOP 24-pin

■ PIN ASSIGNMENT

(TOP VIEW)



(DIP-24P-M02)
(FPT-24P-M01)
(FPT-24P-M03)

■ PIN DESCRIPTIONS

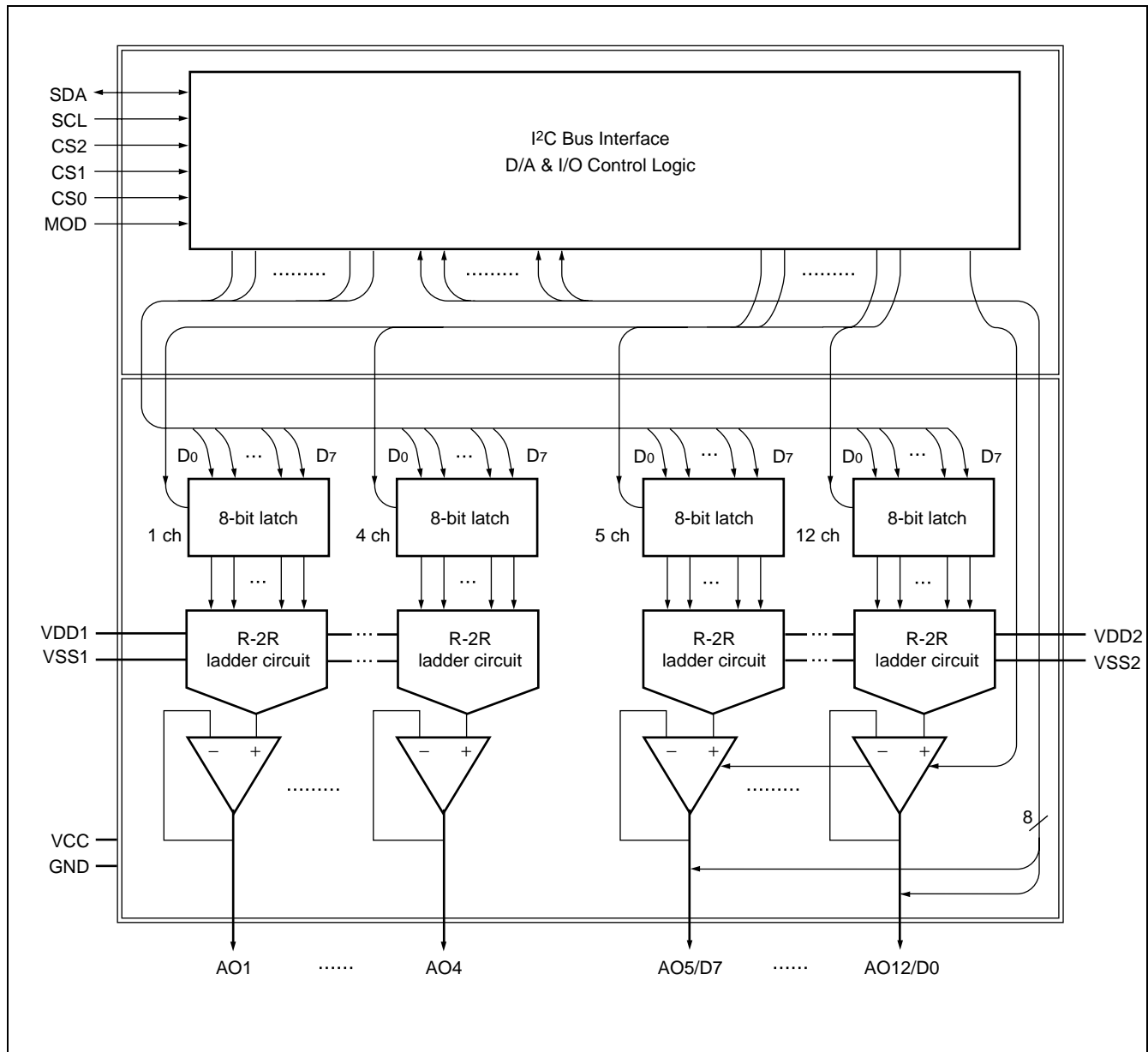
Pin no.	Symbol	I/O	Description
21	SDA	BUS	I ² C bus data input/output pin (hysteresis input). *2 Outputs the acknowledge signal.
20	SCL	I	I ² C bus shift clock input pin (hysteresis input). *2
19	MOD	I	D/A converter and I/O expander mode switching pin. *1, *3 Input "L" to operate as a D/A converter, "H" to operate as I/O expander and D/A converter.
16 17 18	CS0 CS1 CS2	I	Lower 3 bits of the slave address setting pins. *1 This allows up to eight MB88141 chips to be used on the same bus line.
1 2 3 4	AO1 AO2 AO3 AO4	O	8-bit D/A output with OP Amp. *3
5 6 7 8 9 10 11 12	D7/AO5 D6/AO6 D5/AO7 D4/AO8 D3/AO9 D2/AO10 D1/AO11 D0/AO12	I/O	8-bit D/A output with OP Amp. *3 In I/O expander operation, these pins function as parallel data input/output pins.
13	VCC	—	Power supply pin for digital circuits and OP Amp.
24	GND	—	GND pin for digital circuits and OP Amp.
22	VDD1	—	Reference power supply pin for D/A converter (H). AO1 to AO4.
23	VSS1	—	Reference power supply pin for D/A converter (L). AO1 to AO4.
15	VDD2	—	Reference power supply pin for D/A converter (H). AO5 to AO12.
14	VSS2	—	Reference power supply pin for D/A converter (L). AO5 to AO12.

*1: The MOD and CS0-CS2 pins should be used with fixed level input.

*2: Use particular caution in handling the SDA and SCL pins. These pins have no transistor protection against V_{CC} voltage and therefore have weaker anti-static characteristics than other pins.

*3: When using the I/O expander function together with the D/A converter function, take care that D/A converter output precision is within a range that will not affect overall system operation.

■ BLOCK DIAGRAM



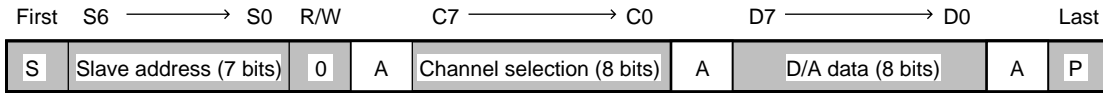
MB88141

■ DATA CONFIGURATION

The MB88141 data configuration differs in each of the two operating modes (D/A converter (12-channel) and I/O expander plus D/A converter), selected by the MOD pin signal.

1. For D/A Converter (12-channel) Operation (MOD = "L")

(1) I²C Bus Format



 : Sent from master device : Sent from MB88141 (slave device)

S: "Start" condition P: "Stop" condition A: "Acknowledge" output

(2) Slave Address Comparison (7 bits)

Slave address input (7 bits)						
S6	S5	S4	S3	S2	S1	S0
1	0	0	1	0	0	0
1	0	0	1	0	0	1
1	0	0	1	0	1	0
1	0	0	1	0	1	1
1	0	0	1	1	0	0
1	0	0	1	1	0	1
1	0	0	1	1	1	0
1	0	0	1	1	1	1

=
=
=
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=

Internally fixed				Externally set		
CS6	CS5	CS4	CS3	CS2	CS1	CS0
1	0	0	1	0	0	0
1	0	0	1	0	0	1
1	0	0	1	0	1	0
1	0	0	1	0	1	1
1	0	0	1	1	0	0
1	0	0	1	1	0	1
1	0	0	1	1	1	0
1	0	0	1	1	1	1

Address comparison: Operates only for devices whose own slave address (internally fixed CS6 to CS3 and externally set CS2 to CS0) matches the slave address input value.

(3) R/W Selection (1 bit)

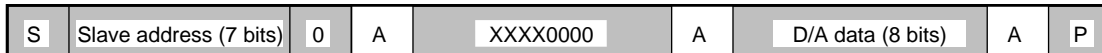
Fixed at "0" (the D/A converter performs write operations only).

(4) Channel Selection (8 bit)

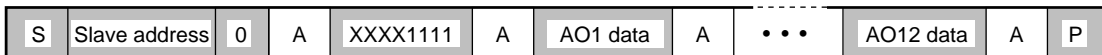
C7	C6	C5	C4	C3	C2	C1	C0	Channel select
x	x	x	x	0	0	0	0	All channels selected *1
x	x	x	x	0	0	0	1	AO1 selected
\	\	\	\	\	\	\	\	\
x	x	x	x	1	1	0	0	AO12 selected
x	x	x	x	1	1	0	1	Don't care
x	x	x	x	1	1	1	0	Don't care
x	x	x	x	1	1	1	1	All channels selected *2

x: Don't care

*1: The 1 byte of data following the channel selection is set on all channels (all channels set to the same data value).



*2: The 12 bytes of data following the channel selection are set on all channels (all channels set to separate data values).



 : Sent from master device : Sent from MB88141 (slave device)

S: "Start" condition P: "Stop" condition A: "Acknowledge" output

Note: Setting will repeat, continuing in order from ch1, until the start and stop conditions are acknowledged.

(5) D/A Data (8 bits)

D7	D6	D5	D4	D3	D2	D1	D0	Channel select
0	0	0	0	0	0	0	0	$\cong V_{SS}$
0	0	0	0	0	0	0	1	$\cong (V_{REF} / 256) \times 1 + V_{SS}$
0	0	0	0	0	0	1	0	$\cong (V_{REF} / 256) \times 2 + V_{SS}$
\	\	\	\	\	\	\	\	\
1	1	1	1	1	1	1	0	$\cong (V_{REF} / 256) \times 254 + V_{SS}$
1	1	1	1	1	1	1	1	$\cong (V_{REF} / 256) \times 255 + V_{SS}$

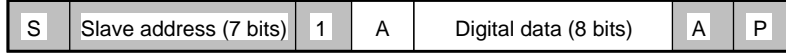
Note: $V_{REF} = V_{DD} - V_{SS}$

MB88141

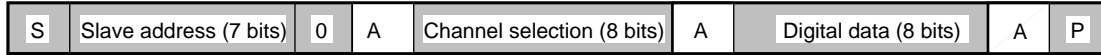
2. For D/A Converter + I/O Expander Operation (MOD = "H")

(1) I²C Bus Format

First S6 → S0 R/W D7 → D0 Last



First S6 → S0 R/W C7 → C0 D7 → D0 Last



 : Sent from master device : Sent from MB88141 (slave device)

S: "Start" condition P: "Stop" condition A: "Acknowledge" output

(2) Slave Address Comparison (7 bits)

Slave address comparison is the same as for D/A converter (12-channel) operation (see "1. (2) "Slave Address Comparison"), with the exception that the CS2 setting determines the number of D/A converter channels and the number of I/O expander bits.

CS2	D/A converter	I/O expander
0	4 channels (AO1 to AO4)	8 bits (D7 to D0)
1	8 channels (AO1 to AO8)	4 bits (D3 to D0)

When CS2 = "1" is selected, the upper 4 bits (D₇ to D₄) of write operations (I²C bus to parallel interface) are ignored, and the upper 4 bits or read operations (parallel interface to I²C bus) are output at "0" (low).

(3) R/W Selection (1 bit)

R/W	I/O expander operation	D/A converter operation
0	I ² C bus input → parallel data output	I ² C bus input → analog output
1	Parallel data input → I ² C bus output	—

(4) Channel Selection (8 bits)

C7	C6	C5	C4	C3	C2	C1	C0	Channel select
×	×	×	×	0	0	0	0	I/O expander operation
×	×	×	×	0	0	0	1	AO1 selected
∖	∖	∖	∖	∖	∖	∖	∖	∖
×	×	×	×	0	1	0	0	AO4 selected
×	×	×	×	0	1	0	1	Don't care (AO5 selected)
∖	∖	∖	∖	∖	∖	∖	∖	∖
×	×	×	×	1	0	0	0	Don't care (AO8 selected)
×	×	×	×	1	0	0	1	Don't care
∖	∖	∖	∖	∖	∖	∖	∖	∖
×	×	×	×	1	1	1	0	Don't care
×	×	×	×	1	1	1	1	I/O expander continuous operation

(): When using D/A converter 8 channel, I/O expander 4 bit operation.

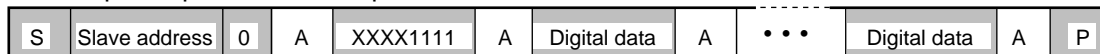
x: Don't care

(5) D/A Data (8 bits)

Same as "1. (5) D/A Data (8 bits)."

(6) I/O Expander Continuous Operation

I²C bus input → parallel data output



Note: In continuous operation, operation continues until start and stop conditions are acknowledged.

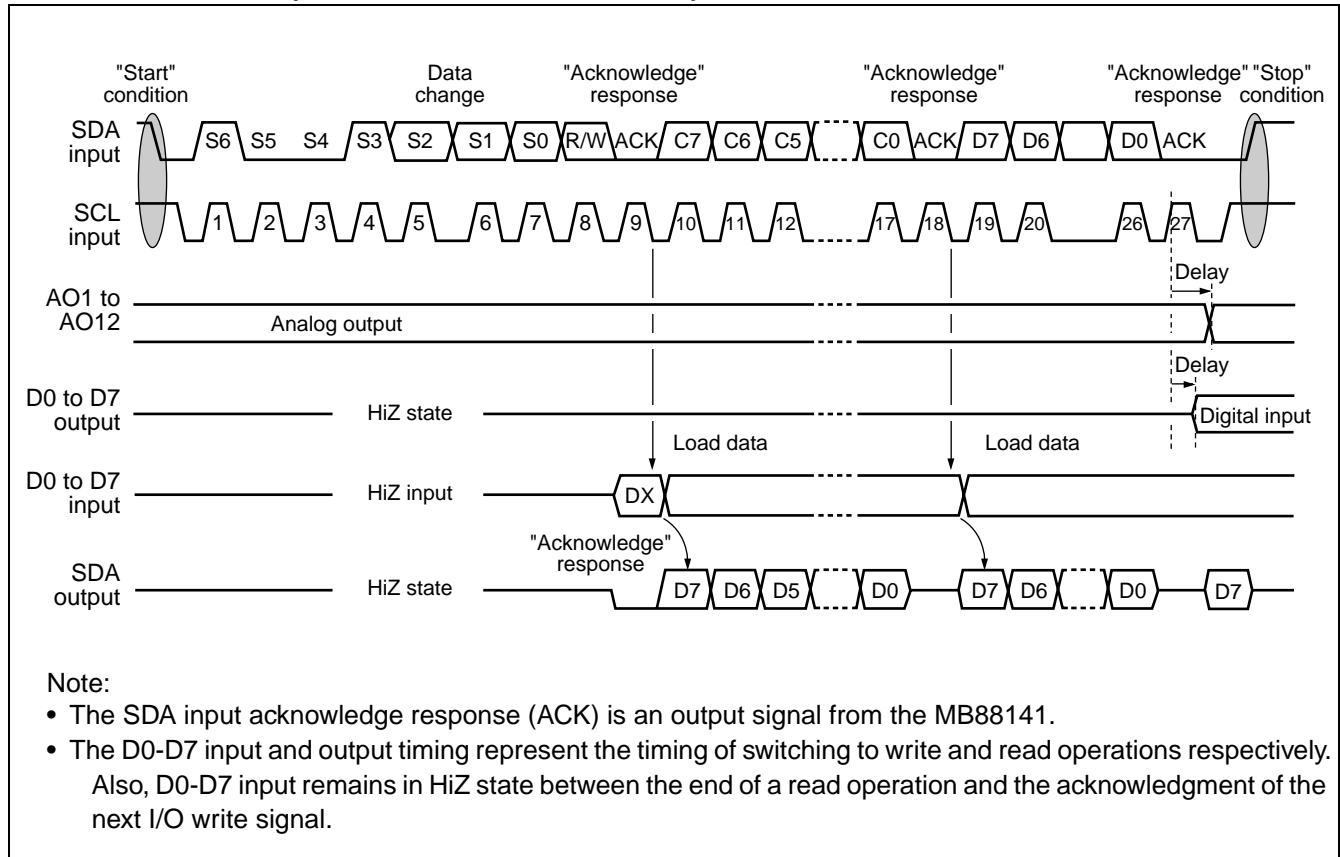
Parallel data input → I²C bus output



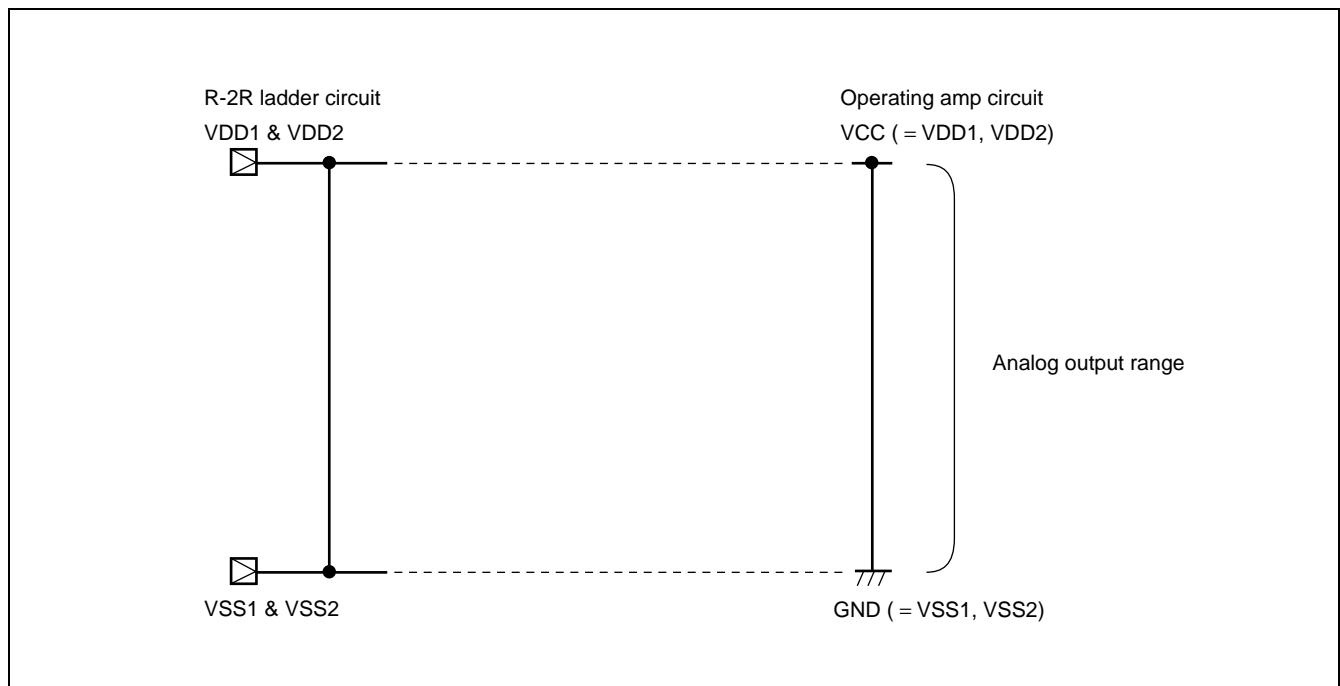
◻ : Sent from master device ◻ : Sent from MB88141 (slave device)

S: "Start" condition P: "Stop" condition A: "Acknowledge" output

■ TIMING CHART (I²C BUS SPECIFICATIONS)



■ ANALOG OUTPUT VOLTAGE RANGE



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating		Unit
			Min.	Max.	
Supply voltage	V _{CC}	With reference to GND, at Ta = +25 °C	-0.3	+7.0*	V
	V _{DD}		-0.3	+7.0*	V
	V _{SS}		-0.3	+7.0*	V
Input voltage	V _{IN}		-0.3	V _{CC} + 0.3	V
Output voltage	V _{OUT}		-0.3	V _{CC} + 0.3	V
Power consumption	P _D	—	—	250	mW
Operating temperature	Ta	—	-20	+85	°C
Storage temperature	Tstg	—	-55	+120	°C

*: V_{CC} ≥ V_{DD1} ≥ V_{SS1}, V_{CC} ≥ V_{DD2} ≥ V_{SS2}

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Supply voltage 1	V _{CC}	—	4.5	5.0	5.5	V
	GND	—	—	0	—	V
Supply voltage 2	V _{DD1}	V _{CC} ≥ V _{DD1} > V _{SS1}	2.0	—	V _{CC}	V
	V _{SS1}	V _{DD1} - V _{SS1} ≥ 2.0 V	0	—	3.5	V
Supply voltage 3	V _{DD2}	V _{CC} ≥ V _{DD2} > V _{SS2}	2.0	—	V _{CC}	V
	V _{SS2}	V _{DD2} - V _{SS2} ≥ 2.0 V	0	—	3.5	V
Analog output current	I _{AL}	Source current	0	—	1.0	mA
	I _{AH}	Sink current	0	—	1.0	mA
Oscillator limit output capacitance	C _{OL}	—	—	—	1.0	μF
Digital data setting range	—	—	#00	—	#FF	—
Operating temperature	Ta	—	-20	—	+85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(1) Digital Circuits

(VCC = 5 V ± 10%, GND = 0 V, Ta = -20 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min.	Typ.	Max.	
Supply voltage	V _{CC}	VCC	—	4.5	5.0	5.5	V
Supply current	I _{CC}		SCL = 400 kHz, no load	—	1.0	3.7	mA
Input leak current	I _{ILK}	SDA, SCL, CS0, CS1, CS2, MOD, D0 to D7	V _{IN} = 0 to V _{CC}	-10	—	+10	μA
“L” level input voltage	V _{IL}		—	0	—	0.3 V _{CC}	V
“H” level input voltage	V _{IH}		—	0.7 V _{CC}	—	V _{CC}	V
Input hysteresis width	V _{HYS}	SDA, SCL	—	0.05 V _{CC}	—	—	V
“H” level output voltage	V _{OH}	D0 to D7	I _{OH} = -400 μA	V _{CC} - 0.4	—	—	V
“L” level output voltage	V _{OL1}		I _{OL} = 2.5 mA	—	—	0.4	V
	V _{OL2}	SDA	I _{OL} = 3.0 mA	—	—	0.4	V
	V _{OL3}		I _{OL} = 6.0 mA	—	—	0.6	V

(2) Analog Circuits 1

(VCC = 5 V ± 10%, GND = 0 V, Ta = -20 °C to +85 °C)

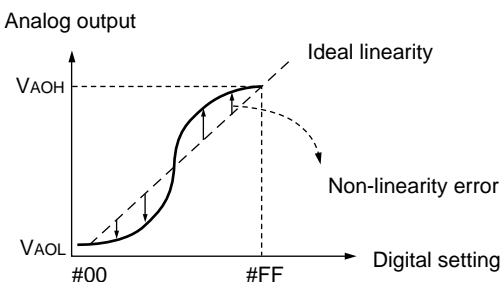
Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min.	Typ.	Max.	
Current consumption	I _{DD}	VDD1, VDD2	No load I _{DD} = I _{DD1} + I _{DD2}	—	1.2	2.5	mA
Analog voltage	V _{DD}		V _{DD1} - V _{SS1} ≥ 2.0 V	2.0	—	V _{CC}	V
	V _{SS}	V _{DD2} - V _{SS2} ≥ 2.0 V	GND	—	3.5	V	
Resolution	Res	AO1 to AO12	No load V _{DD1} , V _{DD2} ≤ V _{CC} - 0.1 V V _{SS1} , V _{SS2} ≥ 0.1 V	—	8	—	bit
Monotonic increase	Rem			—	8	—	bit
Non-linearity error	LE			-1.5	—	+1.5	LSB
Differential linearity error	DLE			-1.0	—	+1.0	LSB

Non-linearity error:

Error in the input/output curve with respect to a straight line connecting output voltage at “00” and output voltage at “FF” levels.

Differential linearity error:

Deviation from ideal voltage with respect to a 1-bit increase in digital value.



Note: V_{AOH} and V_{DD} , as well as V_{AOL} and V_{SS} are not necessarily the same values.

(3) Analog Circuits 2

($V_{CC} = V_{DD1} = V_{DD2} = 5.0\text{ V}$, $GND = V_{SS1} = V_{SS2} = 0.0\text{ V}$, $T_a = -20\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

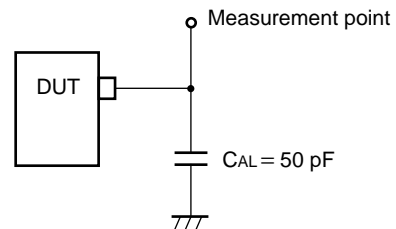
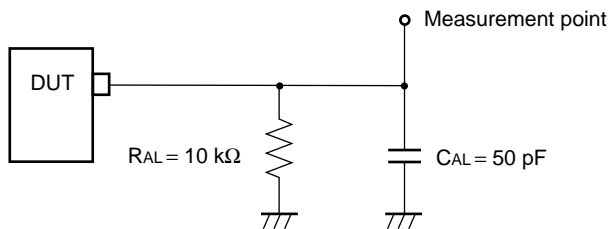
Parameter	Symbol	Pin name	Conditions	Value			Unit	
				Min.	Typ.	Max.		
Output minimum voltage 1	V_{AOL1}	AO1 to AO12	$I_{AL} = 0\ \mu\text{A}$	Digital data "00"	V_{SS}	—	$V_{SS} + 0.1$	V
Output minimum voltage 2	V_{AOL2}		$I_{AL} = 500\ \mu\text{A}$		$V_{SS} - 0.2$	V_{SS}	$V_{SS} + 0.2$	V
Output minimum voltage 3	V_{AOL3}		$I_{AH} = 500\ \mu\text{A}$		V_{SS}	—	$V_{SS} + 0.2$	V
Output minimum voltage 4	V_{AOL4}		$I_{AL} = 1.0\ \text{mA}$		$V_{SS} - 0.3$	V_{SS}	$V_{SS} + 0.3$	V
Output minimum voltage 5	V_{AOL5}		$I_{AH} = 1.0\ \text{mA}$		V_{SS}	—	$V_{SS} + 0.3$	V
Output maximum voltage 1	V_{AOH1}		$I_{AL} = 0\ \mu\text{A}$	Digital data "FF"	$V_{DD} - 0.1$	—	V_{DD}	V
Output maximum voltage 2	V_{AOH2}		$I_{AL} = 500\ \mu\text{A}$		$V_{DD} - 0.2$	—	V_{DD}	V
Output maximum voltage 3	V_{AOH3}		$I_{AH} = 500\ \mu\text{A}$		$V_{DD} - 0.2$	V_{DD}	$V_{DD} + 0.2$	V
Output maximum voltage 4	V_{AOH4}		$I_{AL} = 1.0\ \text{mA}$		$V_{DD} - 0.3$	—	V_{DD}	V
Output maximum voltage 5	V_{AOH5}		$I_{AH} = 1.0\ \text{mA}$		$V_{DD} - 0.3$	V_{DD}	$V_{DD} + 0.3$	V

2. AC Characteristics

Parameter	Symbol	Condition	Value				Unit	
			Standard mode		High speed mode			
			Min.	Max.	Min.	Max.		
SCL clock frequency	f _{SCL}	—	0	100	0	400	kHz	
Bus free time between “stop” condition and “start” condition	t _{BUF}	—	4.7	—	1.3	—	μs	
Hold time (resend) “start” condition. The first clock pulse is generated after this interval.	t _{HD ; STA}	—	4.0	—	0.6	—	μs	
SCL clock low hold time	t _{LOW}	—	4.7	—	1.3	—	μs	
SCL clock high hold time	t _{HIGH}	—	4.0	—	0.6	—	μs	
Resend “start” condition setup time	t _{SU ; STA}	—	4.7	—	0.6	—	μs	
Data hold time	t _{HD ; DAT}	—	0	—	0	0.9	μs	
Data setup time	t _{SU ; DAT}	—	250	—	100	—	ns	
SDA and SCL signal fall time	t _R	—	—	1000	20 + 0.1 C _b	300	ns	
SDA and SCL signal rise time	t _F	—	—	300	20 + 0.1 C _b	300	ns	
“Stop” condition setup time	t _{SU ; STO}	—	4.0	—	0.6	—	μs	
Pulse width of spike suppressed by input filter	t _{SP}	—	—	—	0	50	ns	
Output fall time when bus capacitance is between 10 pF and 400 pF	Sink current 3 mA	t _{OF}	—	—	250	20 + 0.1 C _b	250	ns
	Sink current 6 mA		—	—	—	20 + 0.1 C _b	250	ns
I ² C bus line capacitance load	C _b	—	—	400	—	400	pF	
D/A	Analog output settling time	t _{DL ; AO}	*1	—	100	—	100	μs
I/O expander	Digital output delay time	t _{DL ; DO}	*2	—	300	—	300	ns
	Input open time	t _{DZ ; DI}	*3	200	—	200	—	ns
	Digital input setup time	t _{SU ; DI}	—	250	—	100	—	ns
	Digital input hold time	t _{HD ; DI}	—	0.9	—	0.9	—	μs

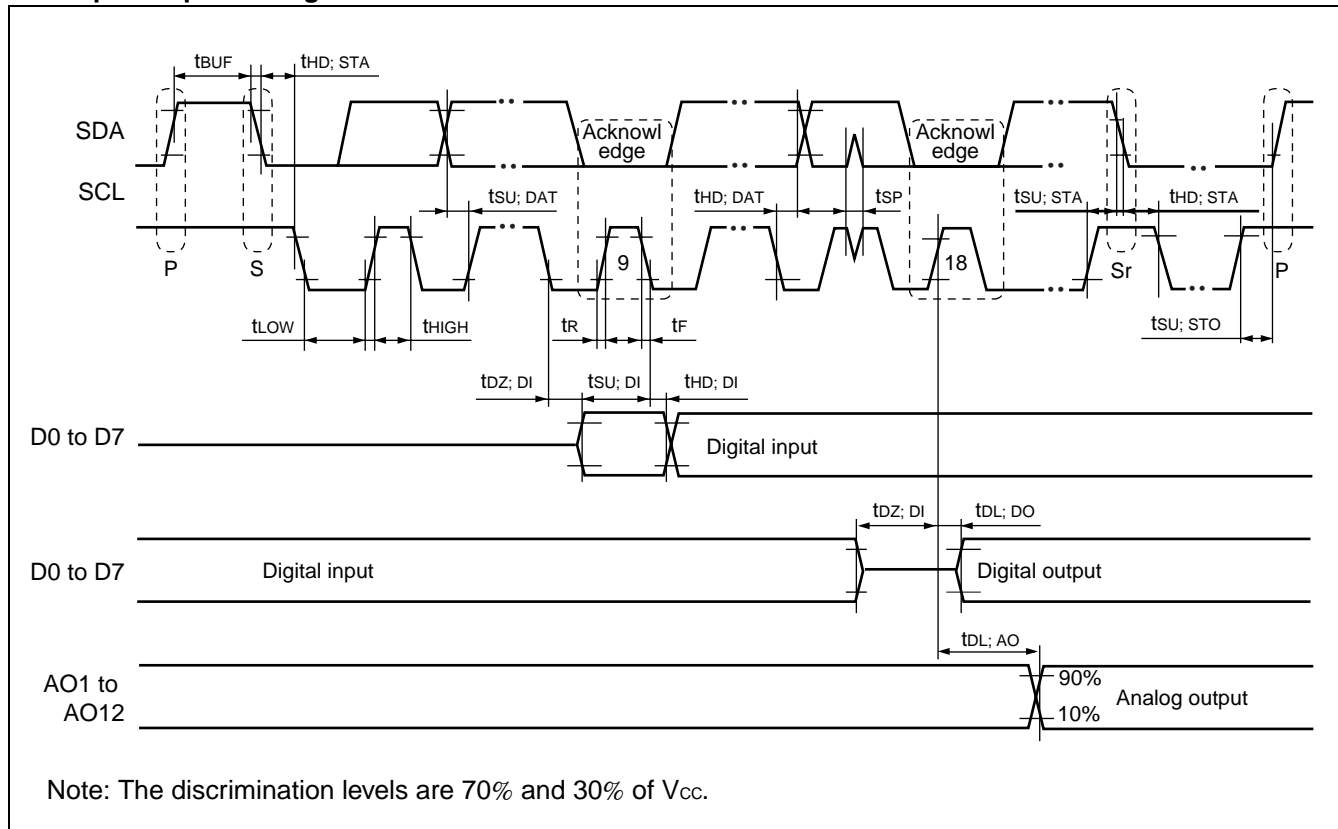
*1: Load condition 1

*2: Load condition 2



*3: The I/O expander input open time value applies to read operation following an I/O write operation, or to an I/O write operation following a read operation.

• Input/output Timing

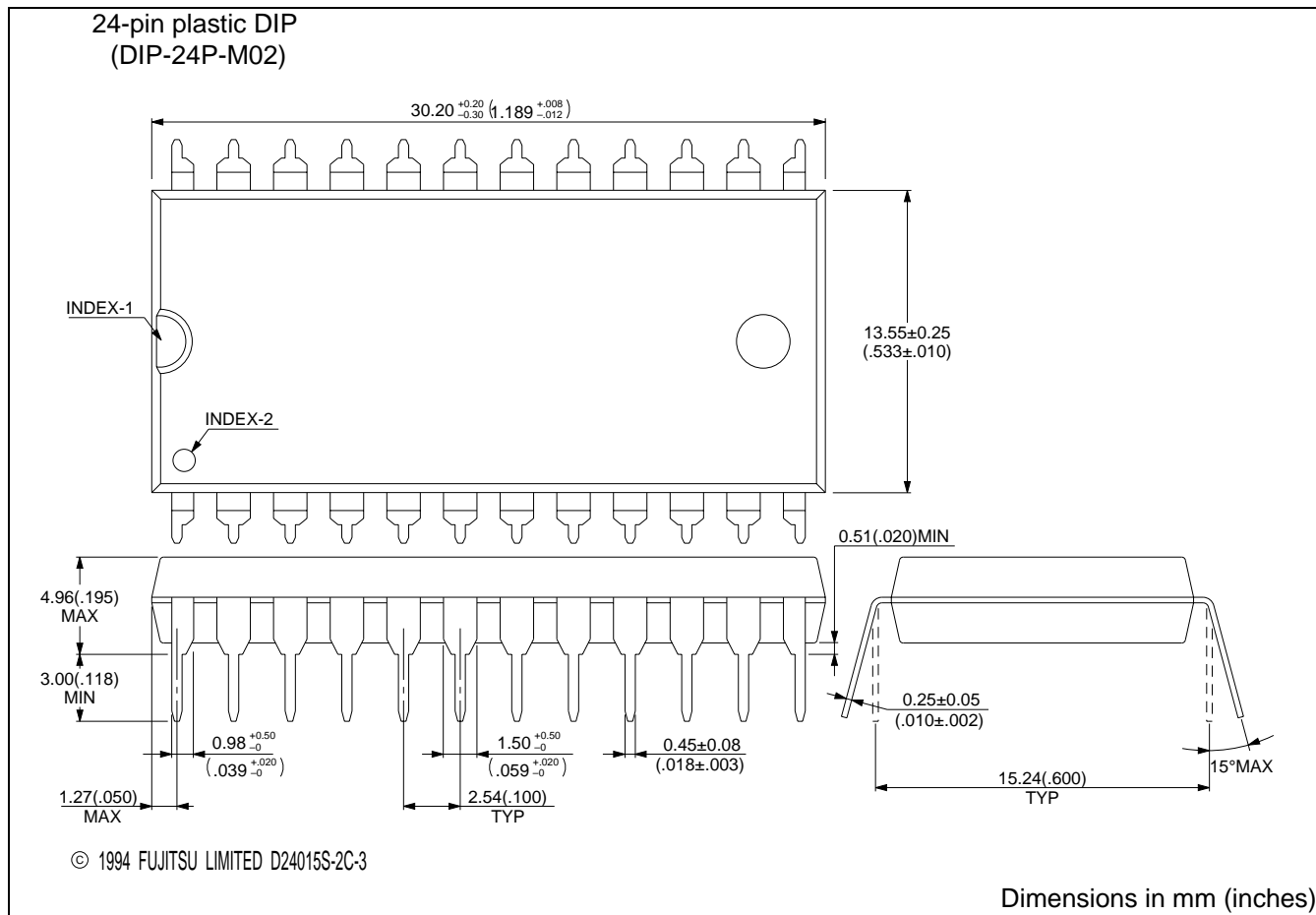


MB88141

■ ORDERING INFORMATION

Part number	Package	Remarks
MB88141P	24-pin plastic DIP (DIP-24P-M02)	
MB88141PF	24-pin plastic SOP (FPT-24P-M01)	
MB88141PFV	24-pin plastic SSOP (FPT-24P-M03)	

■ PACKAGE DIMENSIONS

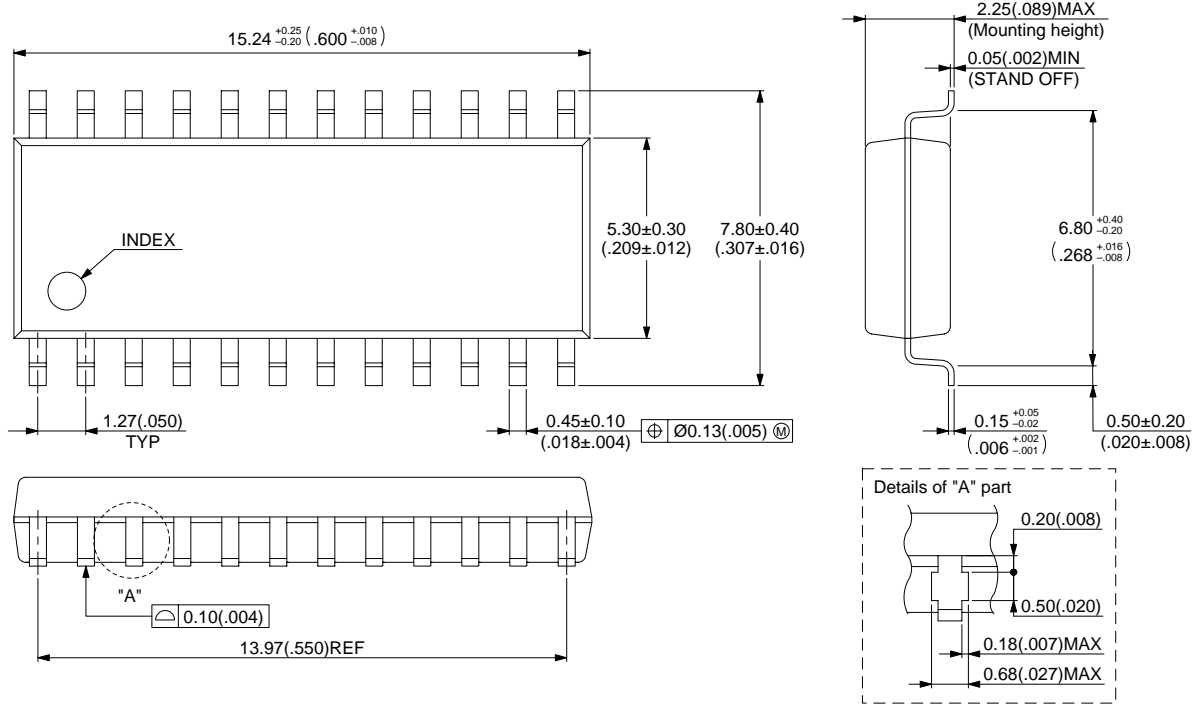


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MB88141

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24-pin plastic SOP
(FPT-24P-M01)



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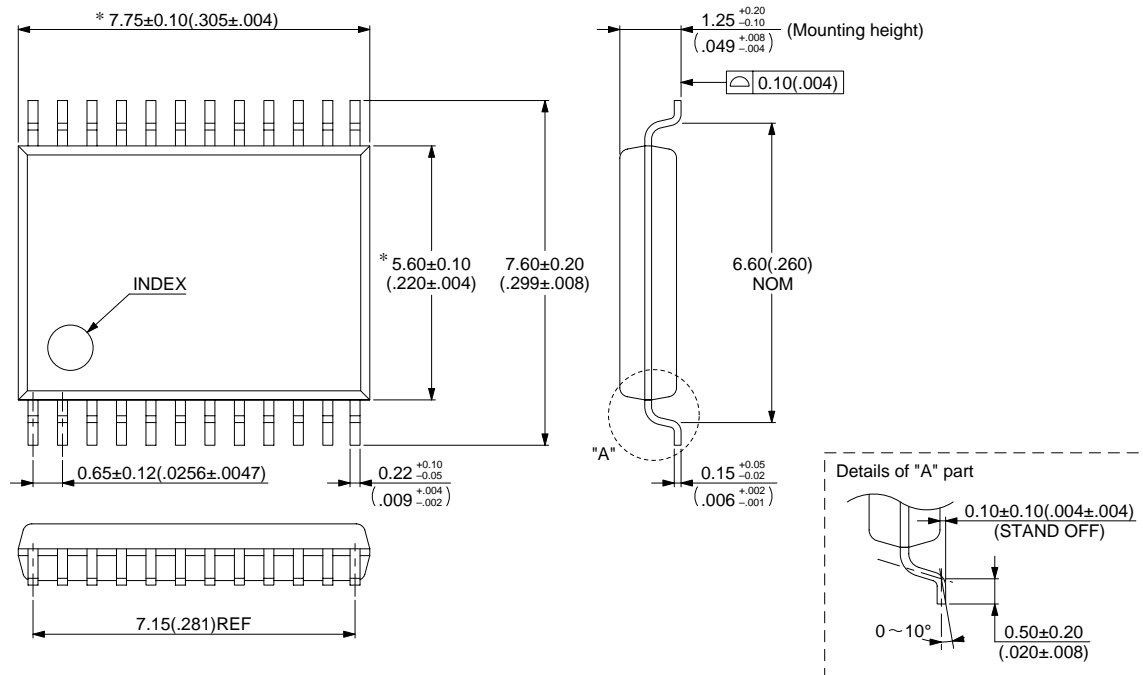
Dimensions in mm (inches)

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24-pin plastic SSOP
(FPT-24P-M03)

Note) * marked dimensions do not include resin residues.



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Dimensions in mm (inches)

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