Smart Two Channel Low-Side Switch

Features

- Power limitation
- Overtemperature protection
- Overload protection
- Short circuit protection
- Diagnostic feedback
- Overvoltage protection
- µC compatible input
- **E**lectro**s**tatic **d**ischarge (ESD) protection

Product Summary

Supply voltage	V_S	6.5 - 40	V
Drain source voltage	$V_{DS(AZ)max}$	60	V
On resistance	$R_{ON\ (typ)}$	0.21	Ω
Output current	I_D	2 x 4	A
Nom. output current	$I_{D(ISO)}$	2 x 1.3	A

Application

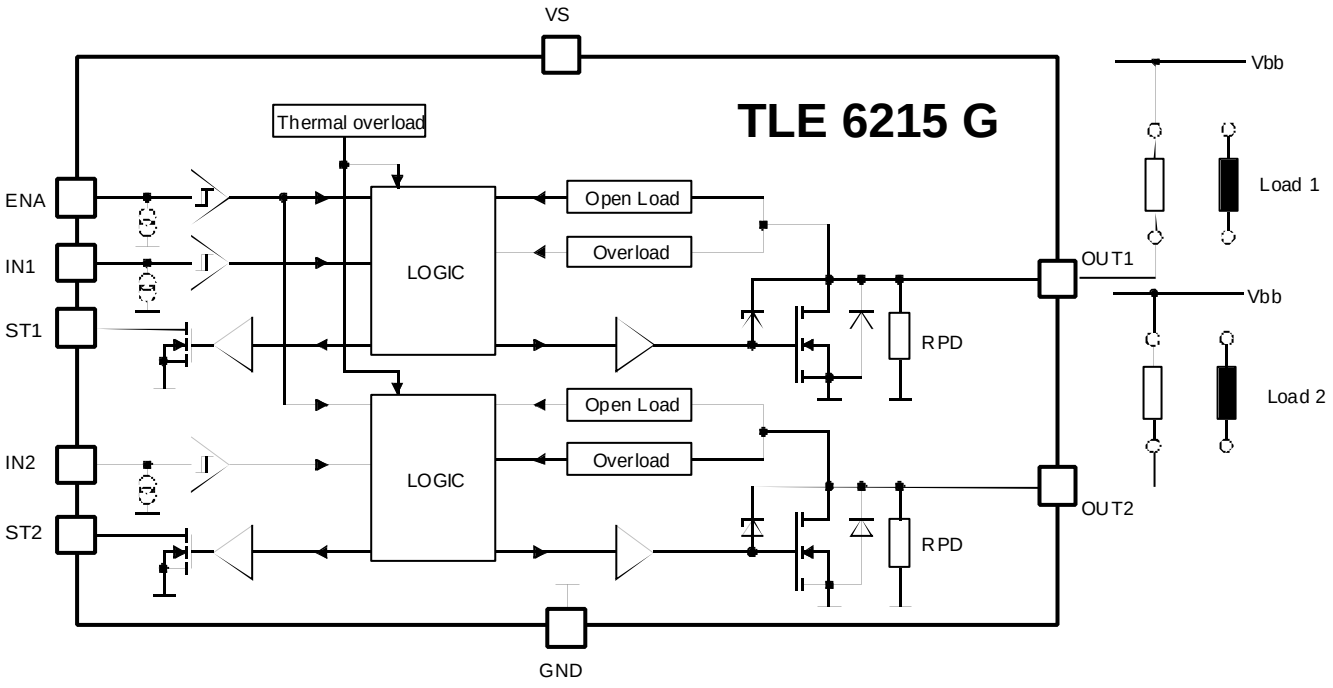
- All kinds of resistive and inductive loads (relays,electromagnetic valves)
- µC compatible power switch
- Solenoid control switch in automotive and industrial control systems

P-DSO-24-3

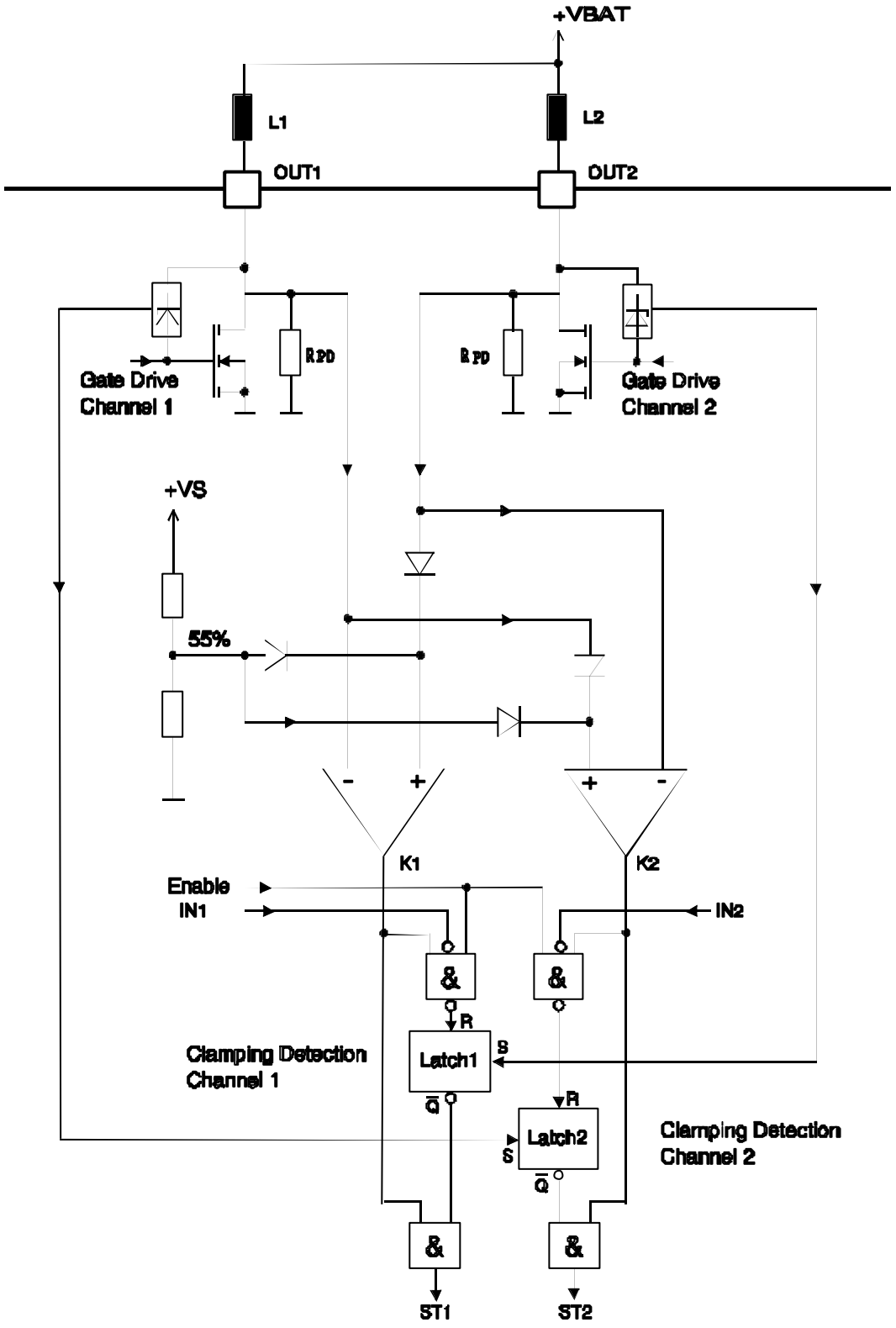
General description

Double channel Low-Side-Switch in Smart Power Technology (SPT) with two seperate inputs and two open drain DMOS output stages. The TLE 6215 G is fully protected by embedded protection functions and designed for automotive and industrial applications.

Block Diagram



Block Diagram of Open Load Detection



Maximum Ratings for T_j = – 40°C to 150°C

Parameter	Symbol	Values	Unit
Supply voltage	V_S	- 0.3 ... + 40	V
Supply voltage operational range	V_S	+ 4.8 ... + 40	V
Continuous drain source voltage (OUT1, OUT2)	V_{DS}	45	V
Input voltage IN1, IN2, ENA	V_{IN}	- 0.3 ... + 6	V
Status output voltage	V_{ST}	- 0.3 ... + 32	V
Operating temperature range Storage temperature range	T_j T_{stg}	- 40 ... + 150 - 55 ... + 150	°C
Output current per channel	$I_{D(lim)}$	Overload shutdown	A
Output current at reversal supply	$I_{D\ 1,2}$	- 4	A
Status output current	I_{ST}	- 5 ... + 5	mA
Inductive load single switch off dissipation energy T_j = 25°C C	E_{AS}	50	mJ
Electro**s**tatic **D**ischarge Voltage (HBM) according to MIL STD 883D, method 3015.7 and EOS/ESD assn. Standard S5.1 – 1993 Output 1,2 Pins All other Pins	 V_{ESD} V_{ESD}	 4000 2000	V V V
Thermal resistance junction - case[1] junction - ambient	R_{thJC} R_{thJA}	12 75	K/W
Maximum operating lifetime (according to "Ambient thermal conditions")	t_b	10000	h

Ambient thermal conditions

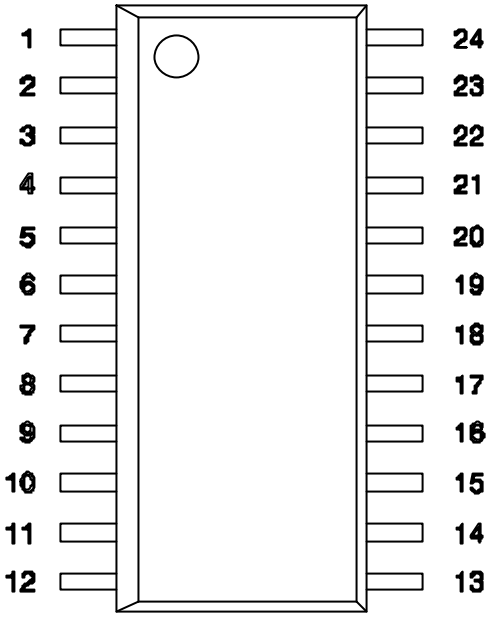
Pos	$T_{Ambient}$ temperature range	operating periods
11	-40 °C	2 %
12	-20 °C	10 %
13	25 °C	24 %
14	60 °C	34 %
15	80 °C	24 %
16	100 °C	5 %
17	> 120 °C	1 %

[1] Case = Pin 5 to 8 and 17 to 20.
Additionally the pins not connected (N.C.) have to be connected to the ground plane used as thermal heatsink to achieve the best thermal resistance.

Pin Definitions and Functions

Pin	Symbol	Function
1	IN1	Control input channel 1
2	ST2	Status output channel 2
3	OUT2	Power output channel 2
4	N.C.	Not connected, cooling
5,6,7,8	GND	Ground, cooling
9,10	N.C.	Not connected, cooling
11	ENA	Enable input for both channels
12	V_S	Supply voltage
13,14,15,16	N.C.	Not connected, cooling
17,18,19,20	GND	Ground, cooling
21	N.C.	Not connected, cooling
22	OUT1	Power output channel 1
23	ST1	Status output channel 1
24	IN2	Control input channel 2

Pin Configuration(top view)



Electrical Characteristics

Parameter and Conditions V_S = 6.5 to 40 V ; T_j = - 40 °C to + 150 °C (unless otherwise specified)		Symbol	Values			Unit
			min	typ	max	
1. Power Supply (V_S)						
Supply current (Outputs ON)	V_S = 40 V	I_S			5	mA
	$V_S \leq$ 18 V			2,5	4	
Supply current (Output OFF)	$V_S \leq$ 18 V	I_S		1,5	3	mA
Operating voltage		V_S	4.8		40	V
2. Power Outputs						
ON state resistance;	T_j = 25 ° C	$R_{DS(ON)}$		0.21		Ω
I_D = 4A; $V_S \geq$ 9.5 V	T_j = 150°C				0.42	
Z-Diode clamping voltage (OUT1, OUT2)		$V_{DS(AZ)}$	45		60	V
Pull down resistor	T_j = 25 ° C	R_{PD}	14	20	26	kΩ
	$T_j \leq$ 125 ° C		10		40	
Output on delay time [2]	I_D = 0.2 A	t_{on}	10	25	40	µs
Output off delay time [2]	I_D = 2 A	t_{off}		40		
Output on fall time [2]	I_D = 0.2 A	t_{fall}		20		
Output off rise time [2]	I_D = 2 A	t_{rise}		25		
Output off status delay time [2]	I_D = 2 A	t_4	20	40	60	
Output on status delay time [2 3 4]		t_5			50	
Overload switch-off delay time [3]		t_{DSO}	50		150	
3. Digital Inputs (IN1, IN2, ENA)						
Input low voltage		V_{INL}	- 0.3		1.0	V
Input high voltage		V_{INH}	2.0		6.0	V
Input voltage hysteresis		V_{INHys}	0.2		0.6	V
Input pull down current	V_{IN} =5 V; $V_S \geq$ 9 V	I_{IN}	50	100	140	µA
Enable pull down current	V_{ENA} =5 V; $V_S \geq$ 9 V	I_{ENA}	15	30	45	µA
4. Digital Status Outputs (ST1, ST2), open Drain						
Output voltage low	I_{ST} = 2 mA	V_{STL}			0.5	V
Leakage current high		I_{STH}			10	µA

[2] See timing diagram, resitive load condition; $V_S \geq$ 9 V
[3] This parameter will not be tested but assured by design
[4] Time till status valid after switching on or error detection

Electrical Characteristics

Parameter and Conditions V_S = 6.5 to 40 V ; T_j = - 40 °C to + 150 °C (unless otherwise specified)		Symbol	Values			Unit
			min	typ	max	
5. Diagnostic Functions						
Open load detection voltage	$V_S \leq 18$ V	$V_{DS(OL)}$	0.515*V_S		0.585*V_S	V
(Output OFF)	V_S = 12 V		6.2		7.0	
Open load compare voltage [5]	18V > V_{DSC} > 0.65*V_S	$V_{DS(OL)C}$	V_{DSC}-1.6		V_{DSC}-0.9	V
Open load detection current (Output ON)		$I_{D(OL)}$	100		500	mA
Overload threshold current	$V_S \geq 9.5$ V	$I_{D(lim)}$	5			A
Overtemperature shutoff threshold [6]		T_{th}	170		200	°C
Hysteresis		T_{hys}		10		K

Application Description

This IC is specially designed to drive inductive loads (relays, electromagnetic valves). Integrated clamp-diodes limit the output voltage peak when switching off an inductive load.

For the detection of errors there are two status outputs, which monitor the following errors by logic levels:

- thermal overload,
- open and short load to ground in active an inactive mode,
- overloading of output (also shorted load to supply) in active mode.

Circuit Description

Input Circuits

The control and enable inputs, all active high, consist of Schmitt triggers with hysteresis. All inputs are connected with pull-down current sources. Not connected inputs are interpreted as "low".

Switching Stages

The power outputs consist of a DMOS power transistor with open drain. The output stages are short-load-protected throughout the operating range. Integrated clamp-diodes limit voltage spikes produced when inductive loads are discharged.

Protective Circuit

The outputs are protected against current overload. There is no protection against reverse polarity of the supply voltage.

[5] V_{DSC} is the output voltage of the other channel used for open load compare detection
[6] This parameter will not be tested but assured by design

Error Detection

The status output signal of the switching stages at normal operation is LOW = OFF; HIGH = ON. In case of any error the status outputs are set according to the table below. If current overload or thermal overload occurs, the error condition is stored in an internal register and the output is shutdown. To reset this register the control input of the affected channel has to be switched off and then on again. The state of the error detection circuit is directly dependent on the input status.
Open load is detected for both on- and off-modus.

In the on-modus the load current is monitored. If it drops below the specified threshold open load is detected. In the off mode, the ouput voltage is monitored.

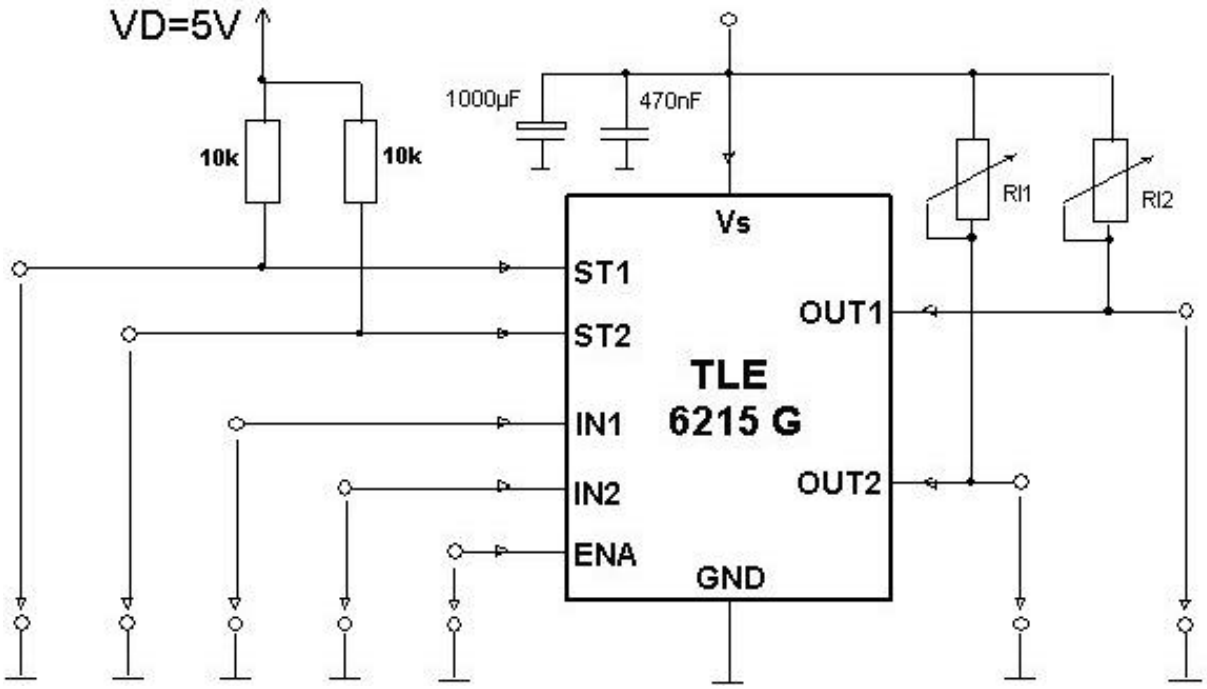
An open load condition is detected when the output voltage of a given channel is below 55 % of the supply voltage Vs. Also the output voltages of two outputs are compaired against each other in off condition with a fixed offset of typ. 1.25 V to recognize GND bypasses. To suppress fault diagnosis during the flyback phase of the compared output, the diagnostic circuit includes a latch function. Reset of this latch is done at end of the flyback phase, additionally it can be reseted by a low signal on the enable input and by a high signal of the input signal. See also the block diagramm of open load detection.

Diagnostic Table

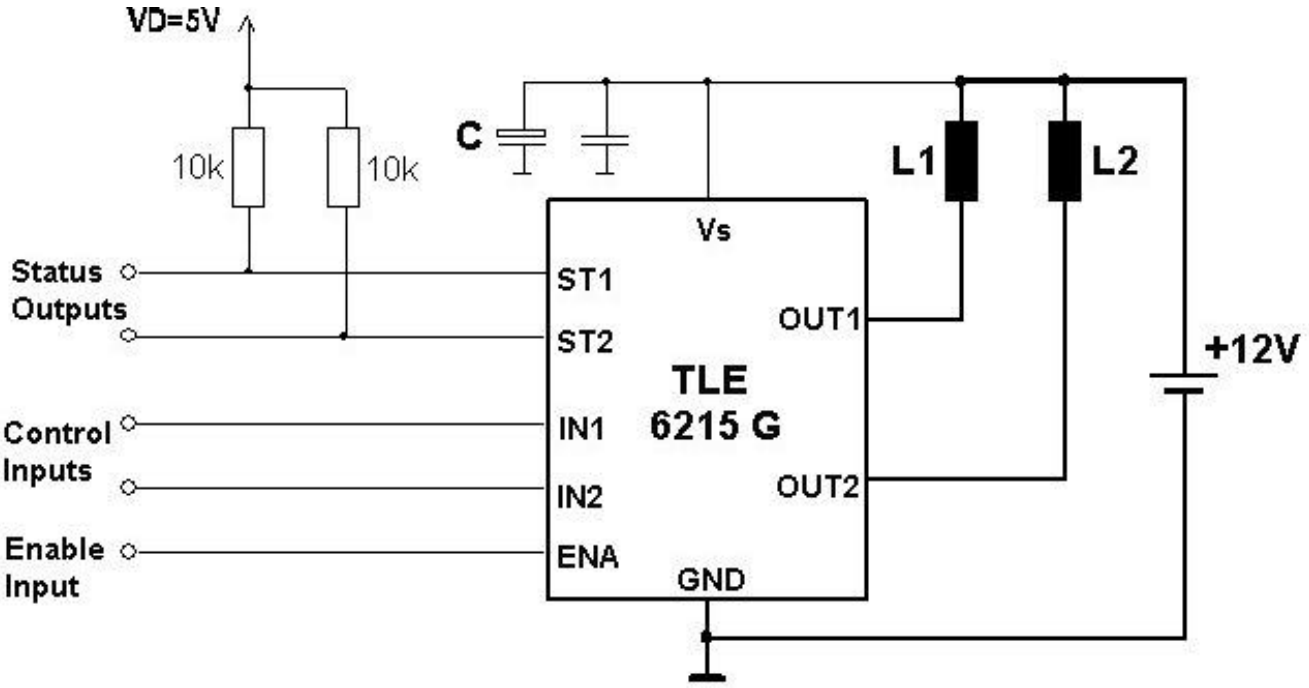
Operating Condition	Inputs			Power Outputs		Status Outputs	
	ENA	**IN1**	**IN2**	**OUT1**	**OUT2**	**ST1**	**ST2**
Normal Function	L	X	X	OFF	OFF	L	L
	H	L	L	OFF	OFF	L	L
	H	H	L	ON	OFF	H	L
	H	L	H	OFF	ON	L	H
	H	H	H	ON	ON	H	H
Thermal Overload	X	L	L	OFF	OFF	L	L
	L	X	X	OFF	OFF	L	L
	H	H	H	OFF	OFF	L	L
Open Load Channel 1	X	L		OFF		H	
	L	H	1)	OFF	1)	H	1)
	H	H		ON		L	
Open Load Channel 2	X		L		OFF		H
	L	1)	H	1)	OFF	1)	H
	H		H		ON		L
Overload Channel 1	L	X		OFF		L	
	H	L	1)	OFF	1)	L	1)
	H	H		OFF		L	
Overload Channel 2	L		X		OFF		L
	H	1)	L	1)	OFF	1)	L
	H		H		OFF		L

1) see normal function

Test Circuit

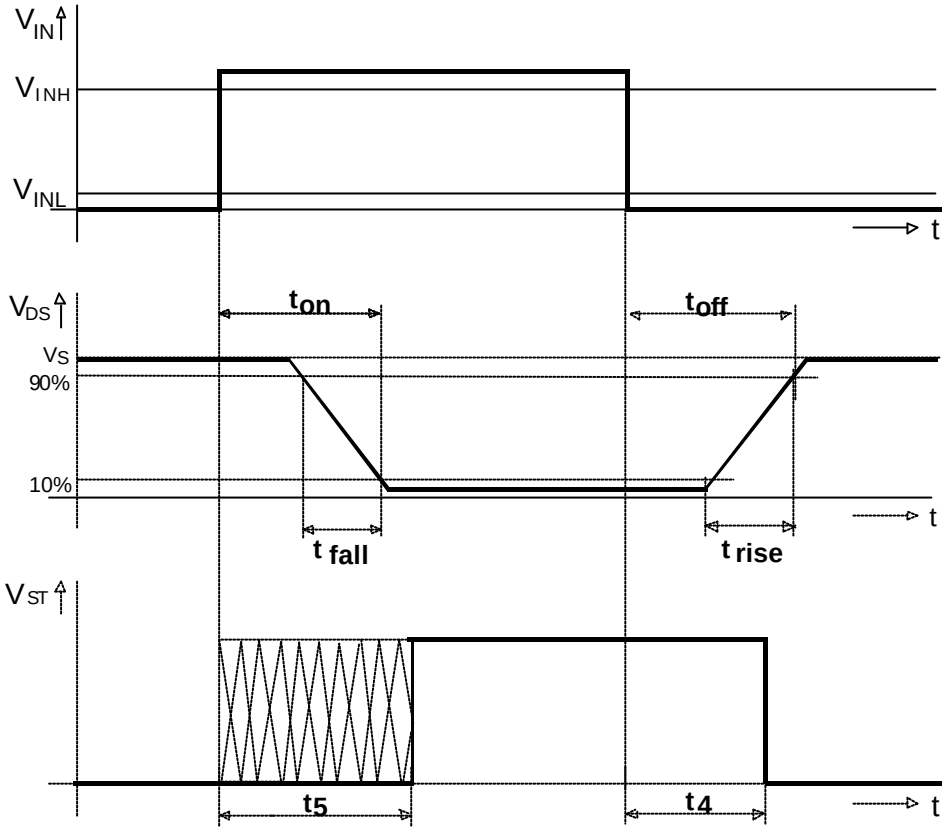


Application Circuit



The blocking capacitor C is recommended to avoid critical negative voltage spikes on V_S in case of battery interruption during OFF-commutation.

Timing Diagram

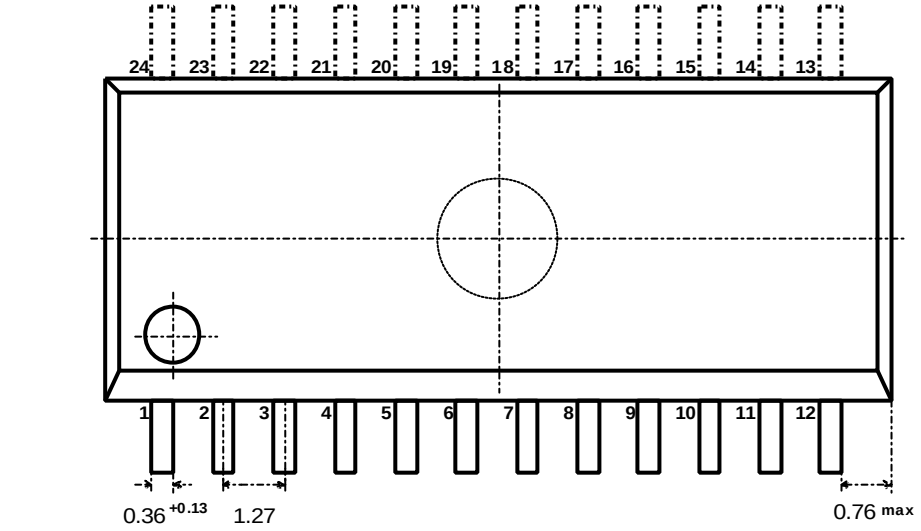


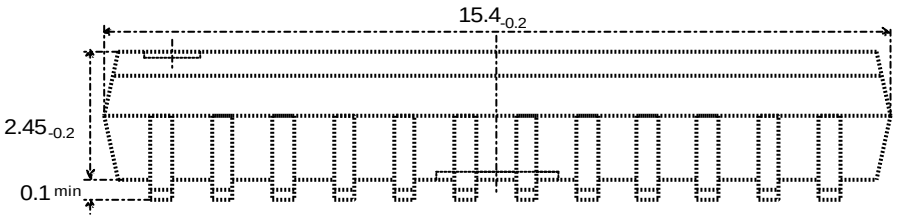
Package and ordering code

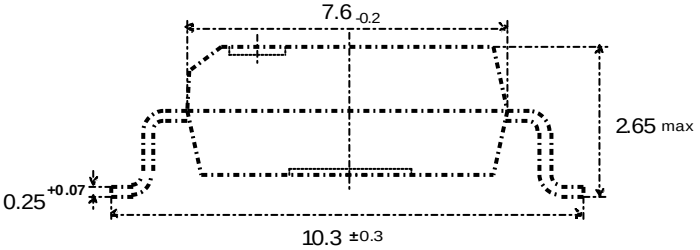
all dimensions in mm

P - DSO - 24 - L16	Ordering code

(Dual-in-line package, small-outline)
24 B 24 DIN 41870 T17







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Revision List:

19.06.2001	Target Datasheet	V1
30.11.2001	First revision	V3
01.03.2002	Second revision	V4
28.04.2002	Preliminary Datasheet	V5