

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Gain, DC 2×10^6 V/V (Typ)
- Acquisition Time $1.0\mu\text{s}$ (0.01%) (Typ)
- Droop Rate $0.08\mu\text{V}/\mu\text{s}$ (+25°C) (Typ)
 $17\mu\text{V}/\mu\text{s}$ (Full Temperature) (Typ)
- Aperture Time..... 25ns (Typ)
- Hold Step Error 1.0mV (Typ)
- Internal Hold Capacitor
- Fully Differential Input
- TTL Compatible

Applications

- High Bandwidth Precision Data Acquisition Systems
- Inertial Navigation and Guidance Systems
- Ultrasonics
- SONAR / RADAR
- Digital to Analog Converter Deglitcher

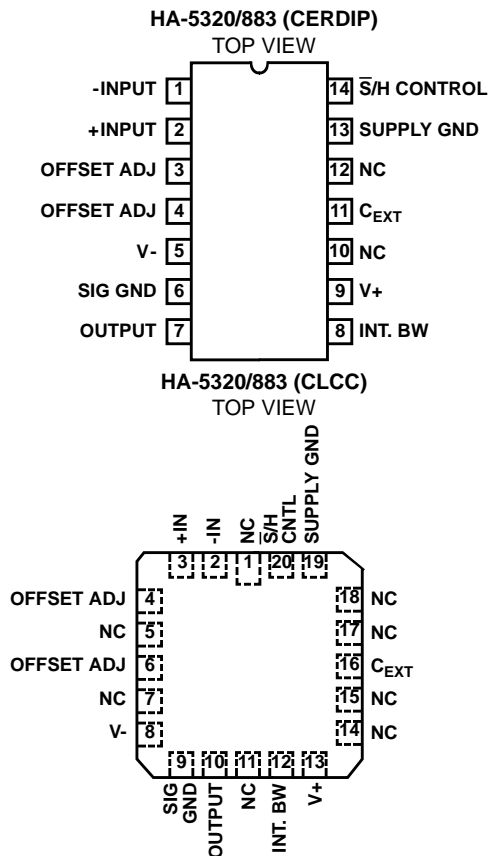
Description

The HA-5320/883 was designed for use in precision, high speed data acquisition systems.

The circuit consists of an input transconductance amplifier capable of providing large amounts of charging current, a low leakage analog switch, and an output integrating amplifier. The analog switch sees virtual ground as its load; therefore, charge injection on the hold capacitor is constant over the entire input/output voltage range. The pedestal voltage resulting from this charge injection can be adjusted to zero by use of the offset adjust inputs. The device includes a hold capacitor. However, if improved droop rate is required at the expense of acquisition time, additional hold capacitance may be added externally.

This monolithic device is manufactured using the Intersil Dielectric Isolation Process, minimizing stray capacitance and eliminating SCR's. This allows higher speed and latch-free operation. For further information, please see Application Note AN538.

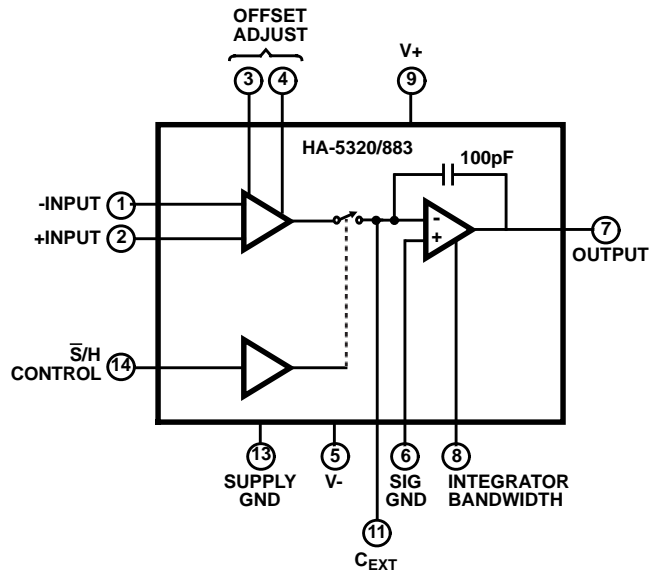
Pinouts



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA1-5320/883	-55°C to +125°C	14 Lead CerDIP
HA4-5320/883	-55°C to +125°C	20 Lead Ceramic LCC

Functional Diagram



Specifications HA-5320/883

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals	40V
Differential Input Voltage	24V
Digital Input Voltage (S/H Pin)	+8V, -15V
Output Current, Continuous (Note 1)	±20mA
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+175°C
Lead Temperature (Soldering 10s)	+300°C
ESD Classification	<2000V

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CerDIP Package	66°C/W	16°C/W
Ceramic LCC Package	57°C/W	9°C/W
Package Power Dissipation at +75°C		
CerDip Package	1.5W	
Ceramic LCC Package	1.75W	
Package Power Dissipation Derating Factor Above +75°C		
CerDip Package	15mW/°C	
Ceramic LCC Package	17mW/°C	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	Logic Level Low (V_{IL})	0V to 0.8V
Operating Supply Voltage ($\pm V_S$)	±15V	Logic Level High (V_{IH})	2.0V to 5.0V
Analog Input Voltage	±10V		

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $V_+ = +15\text{V}$; $V_- = -15\text{V}$; $V_{IL} = 0.8\text{V}$ (Sample); $V_{IH} = 2.0\text{V}$ (Hold); $C_H = \text{Internal} = 100\text{pF}$; Signal GND = Supply GND, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Offset Voltage	V_{IO}		1	+25°C	-1	+1	mV
			2, 3	+125°C, -55°C	-2	+2	mV
Input Bias Current	+ I_B		1	+25°C	-200	+200	nA
			2, 3	+125°C, -55°C	-200	+200	nA
	- I_B		1	+25°C	-200	+200	nA
			2, 3	+125°C, -55°C	-200	+200	nA
Input Offset Current	I_{IO}		1	+25°C	-100	+100	nA
			2, 3	+125°C, -55°C	-100	+100	nA
Open Loop Voltage Gain	+ A_{VS}	$R_L = 1\text{k}\Omega, V_{OUT} = +10\text{V}$	1	+25°C	120	-	dB
			2, 3	+125°C, -55°C	110	-	dB
	- A_{VS}	$R_L = 1\text{k}\Omega, V_{OUT} = -10\text{V}$	1	+25°C	120	-	dB
			2, 3	+125°C, -55°C	110	-	dB
Common Mode Rejection Ratio	+CMRR	$V_+ = 10\text{V}, V_- = -20\text{V}, V_{OUT} = -5\text{V}, V_{S/H} = -4.2\text{V}, V_{GND} = -5\text{V}$	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	-CMRR	$V_+ = 20\text{V}, V_- = -10\text{V}, V_{OUT} = +5\text{V}, V_{S/H} = 5.8\text{V}, V_{GND} = +5\text{V}$	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
Output Current	+ I_O	$V_{OUT} = +10\text{V}$	1	+25°C	10	-	mA
			2, 3	+125°C, -55°C	10	-	mA
	- I_O	$V_{OUT} = -10\text{V}$	1	+25°C	-10	-	mA
			2, 3	+125°C, -55°C	-10	-	mA

Specifications HA-5320/883

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: $V_+ = +15V$; $V_- = -15V$; $V_{IL} = 0.8V$ (Sample); $V_{IH} = 2.0V$ (Hold); $C_H = \text{Internal} = 100pF$; Signal GND = Supply GND,
Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Voltage Swing	+V _{OP}	R _L = 1kΩ	1	+25°C	10	-	V
			2, 3	+125°C, -55°C	10	-	V
	-V _{OP}	R _L = 1kΩ	1	+25°C	-	-10	V
			2, 3	+125°C, -55°C	-	-10	V
Power Supply Current	+I _{CC}	V _{OUT} = 0V, I _{OUT} = 0mA	1	+25°C	-	13	mA
			2, 3	+125°C, -55°C	-	13	mA
	-I _{CC}	V _{OUT} = 0V, I _{OUT} = 0mA	1	+25°C	-13	-	mA
			2, 3	+125°C, -55°C	-13	-	mA
Power Supply Rejection Ratio	+PSRR	V ₊ = 14.5V, 15.5V V ₋ = -15V, -15V	1	+25°C	80	-	dB
			2, 3	+125°C, -55°C	80	-	dB
	-PSRR	V ₊ = +15V, +15V, V ₋ = -14.5V, -15.5V	1	+25°C	65	-	dB
			2, 3	+125°C, -55°C	65	-	dB
Digital Input Current	I _{INL}	V _{IN} = 0V	1	+25°C	-	4	μA
			2, 3	+125°C, -55°C	-	10	μA
	I _{INH}	V _{IN} = 5V	1	+25°C	-	0.1	μA
			2, 3	+125°C, -55°C	-	0.1	μA
Digital Input Voltage	V _{IL}		1	+25°C	-	0.8	V
			2, 3	+125°C, -55°C	-	0.8	V
	V _{IH}		1	+25°C	2.0	-	V
			2, 3	+125°C, -55°C	2.0	-	V
Output Voltage Droop Rate	V _D	V _{OUT} = 0V	2	+125°C	-	100	μV/μs

NOTE:

1. Internal power dissipation may limit output current below 20mA.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 2 Intentionally Left Blank. See AC Specifications in Table 3.

Specifications HA-5320/883

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Hold Mode Feedthrough	V_{HMF}	$V_{IN} = 10V_{P-P}$, 100kHz	1	+25°C	-	3	mV
Hold Step Error	V_{ERROR}	$V_{IH} = 3.5V$, $V_{IL} = 0V$, $T_{RISE} (V_{IL} \text{ to } V_{IH}) = 10ns$	1	+25°C	-11	11	mV
Sample Mode Noise Voltage	$E_{N(SAMPLE)}$	DC to 10MHz, $V_{S/H} = 0V$, $R_{LOAD} = 2k\Omega$	1	+25°C	-	200	μV_{RMS}
Hold Mode Noise Voltage	$E_{N(HOLD)}$	DC to 10MHz, $V_{S/H} = 5V$, $R_{LOAD} = 2k\Omega$	1	+25°C	-	200	μV_{RMS}
Input Capacitance	C_{IN}	$V_{S/H} = 0V$	1	+25°C	-	5	pF
Input Resistance	R_{IN}	$V_{S/H} = 0V$, Delta $V_{IN} = 20V$	1	+25°C	1	-	M Ω
Slew Rate	+SR	$C_L = 50pF$, $R_L = 2k\Omega$, $V_{OUT} = -5V \text{ to } +5V$ Step 10%, 90% pts	1	+25°C	30	-	V/ μs
	-SR	$C_L = 50pF$, $R_L = 2k\Omega$, $V_{OUT} = +5V \text{ to } -5V$ Step 10%, 90% pts	1	+25°C	30	-	V/ μs
Rise and Fall Times	T_R	$C_L = 50pF$, $R_L = 2k\Omega$, $V_{OUT} = 0V \text{ to } +200mV$ Step 10%, 90% pts	1	+25°C	-	150	ns
	T_F	$C_L = 50pF$, $R_L = 2k\Omega$, $V_{OUT} = 0V \text{ to } -200mV$ Step 10%, 90% pts	1	+25°C	-	150	ns
Overshoot	+OS	$C_L = 50pF$, $R_L = 2k\Omega$, $V_{OUT} = 0V \text{ to } +200mV$ Step	1	+25°C	-	25	%
	-OS	$C_L = 50pF$, $R_L = 2k\Omega$, $V_{OUT} = 0V \text{ to } -200mV$ Step	1	+25°C	-	25	%
0.1% Acquisition Time	$T_{ACQ} 0.1\%$	$C_L = 50pF$, $R_L = 2k\Omega$, $V_{OUT} = 0V \text{ to } 10V$ Step	1	+25°C	-	1.2	μs

NOTE:

- The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLE 1)
Interim Electrical Parameters (Pre Burn-In)	-
Final Electrical Test Parameters	1(Note 1), 2, 3
Group A Test Requirements	1, 2, 3
Groups C and D Endpoints	1

NOTE:

- PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

HA-5320/883

Die Characteristics

DIE DIMENSIONS:

92 x 152 x 19 ± 1mils

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:

Type: Nitride (Si₃N₄) over Silox (SiO₂, 5% Phos)
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1.5kÅ

WORST CASE CURRENT DENSITY:

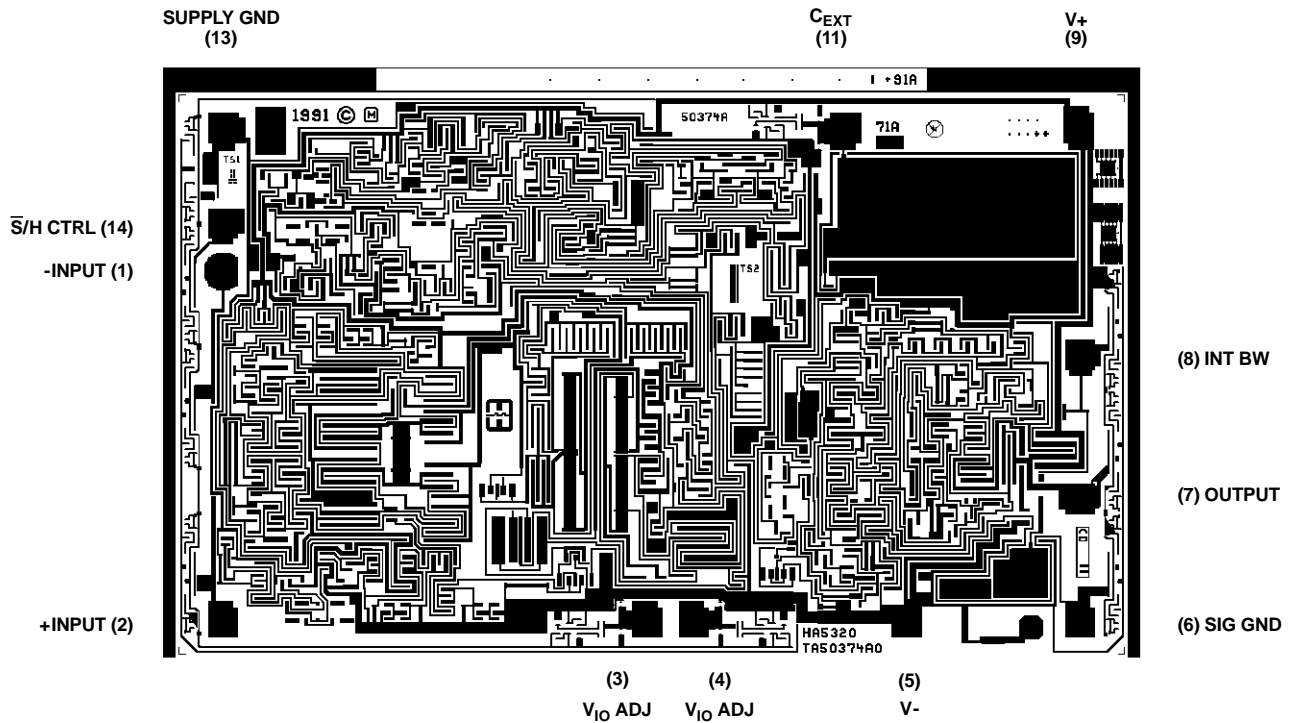
1.742 x 10⁵ A/cm²

TRANSISTOR COUNT: 184

SUBSTRATE POTENTIAL: V-

Metallization Mask Layout

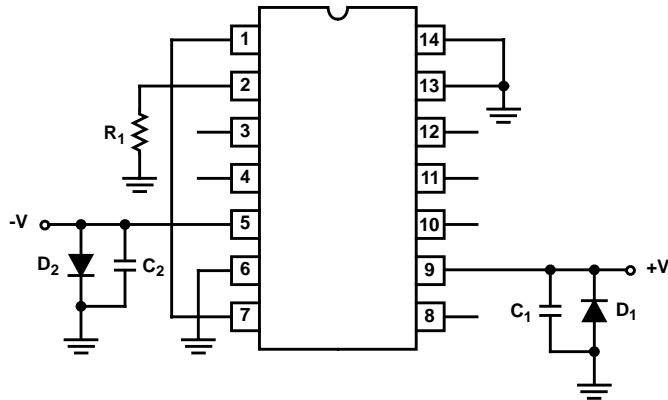
HA-5320/883



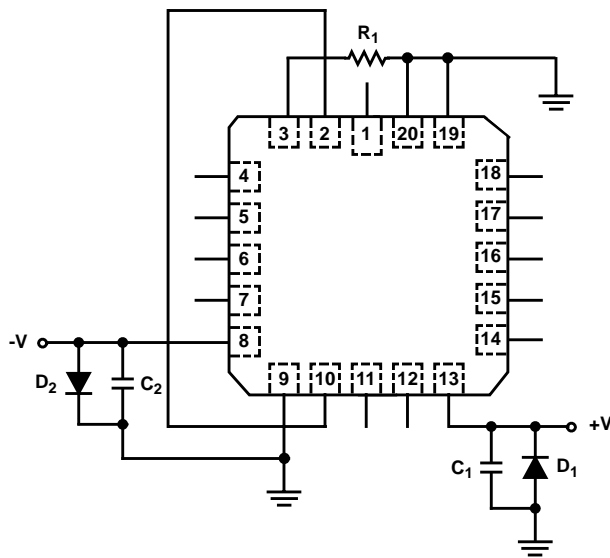
HA-5320/883

Burn-In Circuits

HA-5320/883 DIP BURN-IN/LIFE TEST CIRCUIT



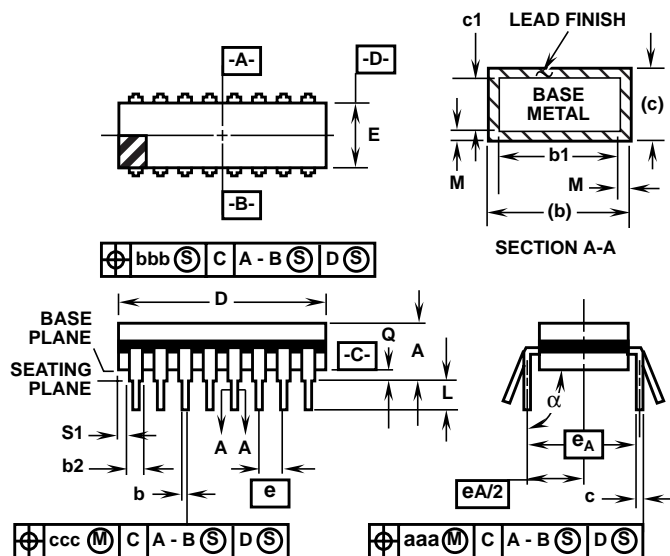
HA-5320/883 LCC BURN-IN/LIFE TEST CIRCUIT



NOTES:

1. $R_1 = 100k\Omega$, 5%, (per socket).
2. $C_1, C_2 = 0.01\mu F$ minimum per socket or $0.1\mu F$ minimum per row.
3. $D_1, D_2 = 1N4002$ or equivalent (per board).
4. $+V = +15.5V \pm 0.5V$, $-V = -15.5V \pm 0.5V$.

Packaging



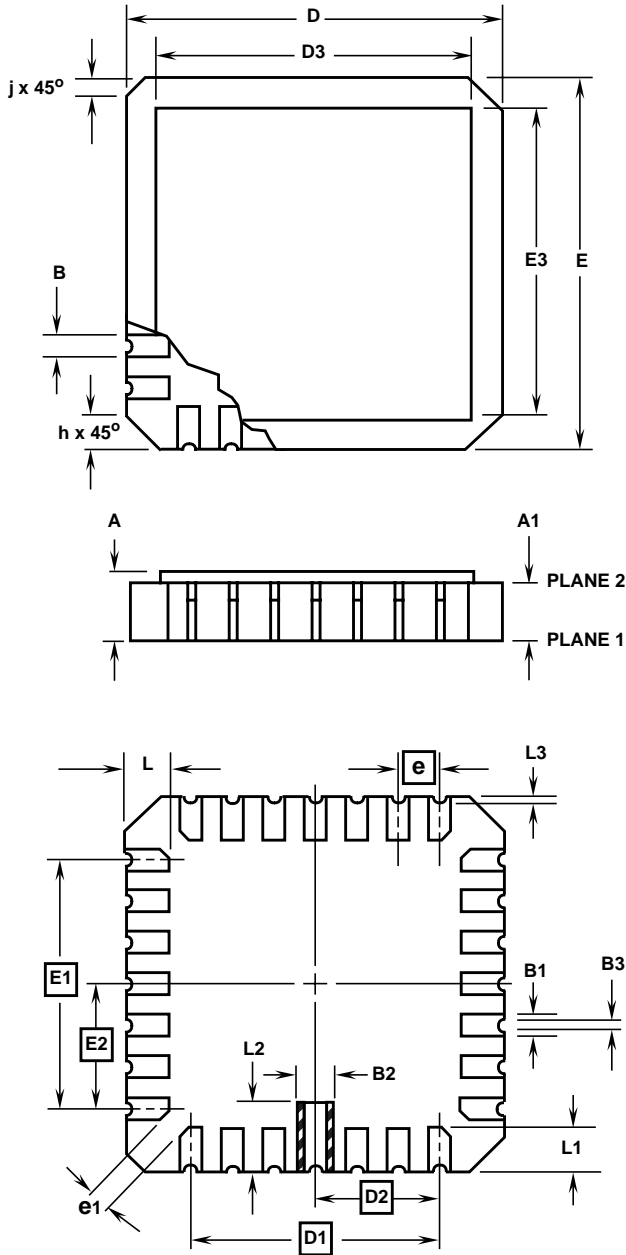
**F14.3 MIL-STD-1835 GDIP1-T14 (D-1, CONFIGURATION A)
14 LEAD DUAL-IN-LINE FRIT-SEAL CERAMIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	-
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	14		14		8

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling Dimension: Inch.
11. Materials: Compliant to MIL-I-38535.

Packaging (Continued)



J20.A MIL-STD-1835 CQCC1-N20 (C-2)
20 PAD METAL SEAL LEADLESS CERAMIC CHIP CARRIER

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.060	0.100	1.52	2.54	6, 7
A1	0.050	0.088	1.27	2.23	7
B	-	-	-	-	4
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.342	0.358	8.69	9.09	-
D1	0.200 BSC		5.08 BSC		-
D2	0.100 BSC		2.54 BSC		-
D3	-	0.358	-	9.09	2
E	0.342	0.358	8.69	9.09	-
E1	0.200 BSC		5.08 BSC		-
E2	0.100 BSC		2.54 BSC		-
E3	-	0.358	-	9.09	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.91	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	5		5		3
NE	5		5		3
N	20		20		3

NOTES:

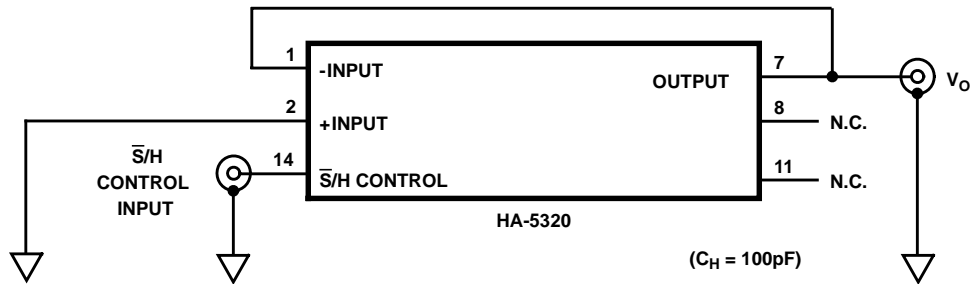
1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.381mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E", respectively.
4. The required plane 1 terminals and optional plane 2 terminals shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Maximum limits allows for 0.007 inch solder thickness on pads.
8. Materials: Compliant to MIL-I-38535.

DESIGN INFORMATION (Continued)

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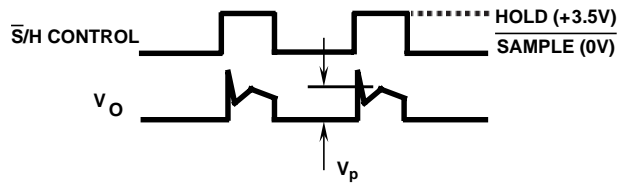
Test Circuits

CHARGE TRANSFER AND DRIFT CURRENT



CHARGE TRANSFER TEST

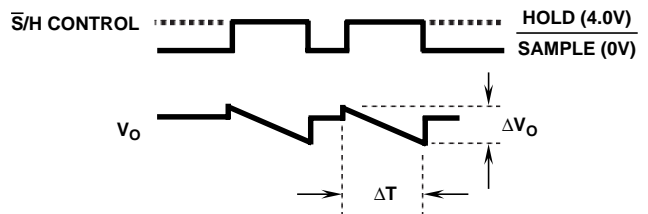
1. Observe the "hold step" voltage V_p :



2. Compute charge transfer: $Q = V_p C_H$

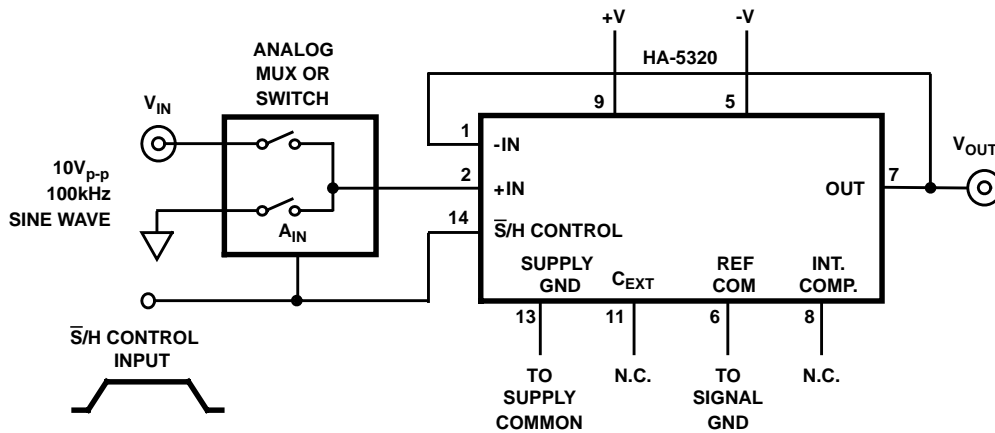
DRIFT CURRENT TEST

1. Observe the voltage "droop", $\Delta V_O / \Delta T$:



2. Measure the slope of the output during hold, $\Delta V_O / \Delta T$, and compute drift current: $I_D = C_H \Delta V_O / \Delta T$.

HOLD MODE FEED THROUGH ATTENUATION



$$\text{Feedthrough in dB} = 20 \text{ Log } \frac{V_{OUT}}{V_{IN}} \text{ where:}$$

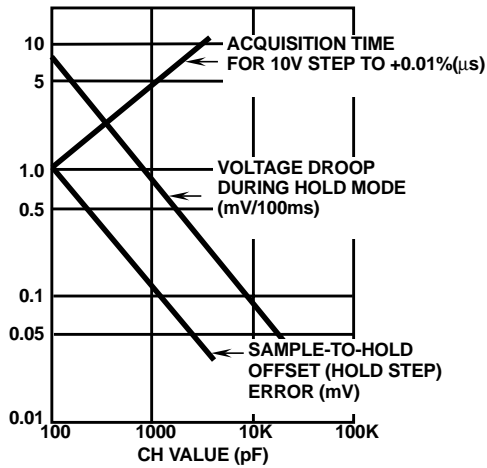
V_{OUT} = Volts_{p-p}, Hold Mode,
 V_{IN} = Volts_{p-p}.

DESIGN INFORMATION (Continued)

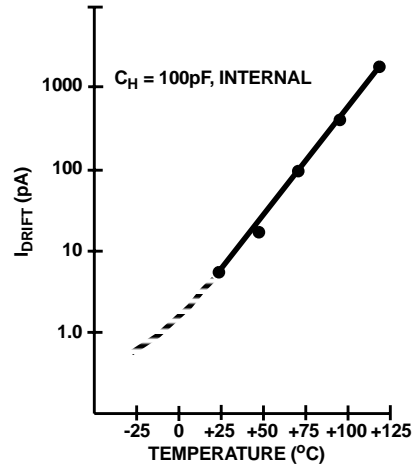
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Performance Curves $V_{SUPPLY} = \pm 15VDC$

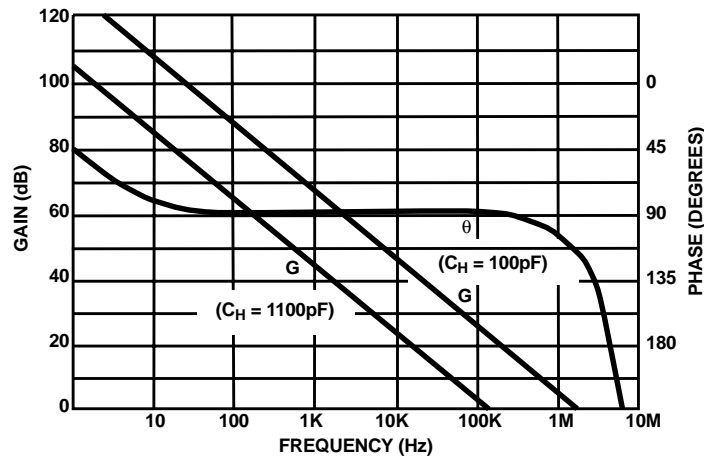
TYPICAL SAMPLE AND HOLD PERFORMANCE AS FUNCTION OF HOLDING CAPACITOR



DRIFT CURRENT vs TEMPERATURE

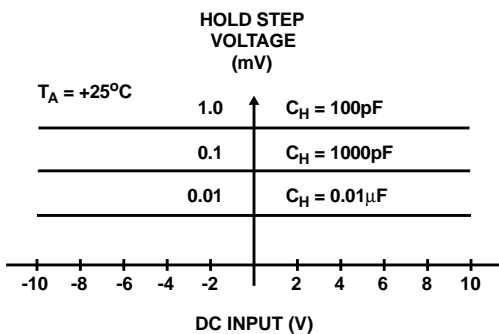


OPEN LOOP GAIN AND PHASE RESPONSE

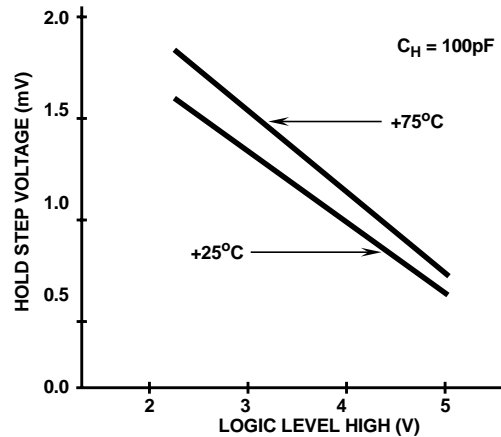


TYPICAL SAMPLE-TO-HOLD OFFSET (HOLD STEP) ERROR

HOLD STEP vs. INPUT VOLTAGE



HOLD STEP vs. LOGIC (V_{IH}) VOLTAGE



DESIGN INFORMATION (Continued)

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Glossary of Terms

Acquisition Time

The time required following a "sample" command, for the output to reach its final value within $\pm 0.1\%$ or $\pm 0.01\%$. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

Charge Transfer

The small charge transferred to the holding capacitor from the inter-electrode capacitance of the switch when the unit is switched to the HOLD mode. Charge transfer is directly proportional to sample-to-hold offset pedestal error, where:

$$\text{Charge Transfer (pC)} = C_H (\text{pF}) \times \text{Offset Error (V)}$$

Aperture Time

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is the interval between the conditions of 10% open and 90% open.

Hold Step Error

Hold Step Error is the output error due to Charge Transfer (see above). It may be calculated from Charge Transfer, using the following relationship:

$$\text{HOLD STEP (V)} = \frac{\text{CHARGE TRANSFER (pC)}}{\text{HOLD CAPACITANCE (pF)}}$$

See Performance Curves.

Effective Aperture Delay Time (EADT)

The difference between propagation time from the analog input to S/H switch, and digital delay time between the Hold command and opening of the switch.

EADT may be positive, negative or zero. If zero, the \bar{S}/H amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of V_{IN} that occurred before the Hold command.

Aperture Uncertainty

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

Drift Current

The net leakage current from the hold capacitor during the hold mode. Drift current can be calculated from the droop rate using the formula:

$$I_D (\text{pA}) = C_H (\text{pF}) \times \frac{\Delta V (\text{V/s})}{\Delta T}$$

TYPICAL PERFORMANCE CHARACTERISTICS

PARAMETER	CONDITIONS	TEMPERATURE	TYP	UNITS
Input Voltage Range		Full	± 10	V
Offset Voltage Drift		Full	5	$\mu\text{V}/^\circ\text{C}$
Gain Bandwidth Product ($C_H = 100\text{pF}$)	$A_v = +1, V_O = 200\text{mV}_{P-P}, R_L = 2\text{K}, C_L = 50\text{pF}$	$+25^\circ\text{C}$	2	MHz
Gain Bandwidth Product ($C_H = 1000\text{pF}$)	$A_v = +1, V_O = 200\text{mV}_{P-P}, R_L = 2\text{K}, C_L = 50\text{pF}$	$+25^\circ\text{C}$	0.18	MHz
Full Power Bandwidth	$V_O = 20\text{V}_{P-P}, R_L = 2\text{K}, C_L = 50\text{pF}$	$+25^\circ\text{C}$	600	kHz
Output Resistance (Hold Mode)		$+25^\circ\text{C}$	1.0	Ω
0.1% Acquisition Time	$V_O = 10\text{V Step}, R_L = 2\text{K}, C_L = 50\text{pF}$	$+25^\circ\text{C}$	0.8	μs
0.01% Acquisition Time	$V_O = 10\text{V Step}, R_L = 2\text{K}, C_L = 50\text{pF}$	$+25^\circ\text{C}$	1.0	μs
Effective Aperture Delay Time		$+25^\circ\text{C}$	-25	ns
Aperture Uncertainty		$+25^\circ\text{C}$	0.3	ns
0.01% Hold Mode Settling Time		$+25^\circ\text{C}$	165	ns

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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