Data Sheet | March 2000 | File Number 4823.1

3.3V Dual 8-Bit, 40MSPS A/D Converter with Internal Reference and Digital Clamp

The HI2325 is a monolithic, dual 8-bit, 40MSPS analog-to-digital converter fabricated in an advanced CMOS process. It is designed for high speed applications where integration, bandwidth and accuracy are essential. The HI2325 features a 2-stage parallel architecture. Only one external clock is necessary to drive both converters and an internal voltage reference is provided allowing the system designer to realize an increased level of system integration resulting in decreased cost and power dissipation.

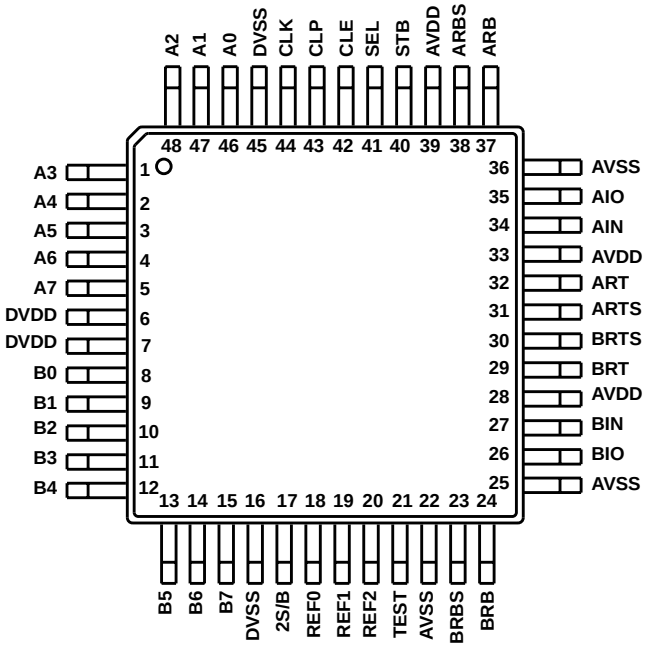
The HI2325 has excellent dynamic performance while consuming less than 100mW power at 40MSPS. The A/D only requires a single +3.3V power supply and encode clock. Data output latches are provided which present valid data to the output bus with a latency of 2 clock cycles.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI2325IN	-20 to 85	48 Ld MQFP/PQFP	Q48.7x7-S

Pinout

48 LEAD LQFP
TOP VIEW



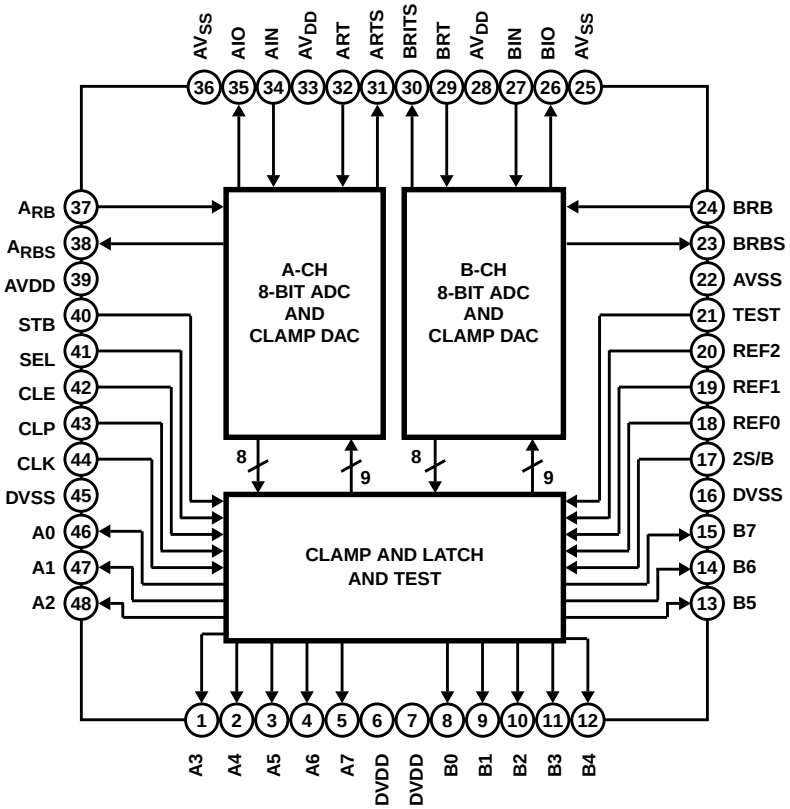
Features

- Sampling Rate 40MSPS
- 6.5 Bits at f_{IN} = 1MHz
- Low Power at 40MSPS. 100mW
- Power Down Mode 8mW
- Wide Full Power Input Bandwidth. 250MHz
- Excellent Channel-to-Channel Isolation . . . . . >75dB
- Internal Digital Clamp
- Internal Voltage Reference
- Single Supply Voltage Operation . . . . . +3.3V
- TTL/CMOS Compatible Digital Inputs
- CMOS Compatible Digital Outputs. 3.3V
- Offset Binary or 2's Complement Output Format
- Dual 8-Bit A/D Converters on a Monolithic Chip

Applications

- Wireless Local Loop
- PSK and QAM I&Q Demodulators
- Medical Imaging and Instrumentation
- Portable Communications
- Power Metering
- Hand-Held Data Collection Instruments

Functional Block Diagram



Pin Descriptions

PIN NO.	SYMBOL	I/O	EQUIVALENT CIRCUIT	DESCRIPTION
46, 47, 48, 1- 5	A0 - A7	O		Digital Output. A0(LSB) - A7(MSB)
8 - 15	B0 - B7	O		Digital Output. B0(LSB) - B7(MSB)
6, 7	DVDD			Digital power supply.
16	DVSS			Digital ground.
17	2S/B	I	Pull-down resistors are incorporated.	Selects output code. H: 2's Compliment Code L: Binary Code
18, 19, 20	REF0 ~ 2	I	Pull-down resistors are incorporated.	Determines the clamp circuit reference data. See the table "Digital Clamp Reference Level".
21	TEST	I	Pull-down resistors are incorporated.	Normally open.
22, 25	DVSS			Digital ground.
22, 25, 36	AVSS			Analog ground.
23 38	BRBS ARBS			Shorting these pins to AVSS generates voltage of about 0.5V at the BRB and ARB pins.
24 37	BRB ARB			Reference voltage (bottom).
29 32	BRT ART			Reference voltage (top).
30 31	BRTS ARTS			Shorting these pins to AVDD generates voltage of about 2.5V at the BRT and ART pins.
26 35	BIO AIO	O		Analog output. The digital clamp circuit comprises a D/A converter whose outputs are available on these pins.
27 34	BIN AIN	I		Analog input.
28, 33, 39	AVDD			Analog power supply.
40	STB	I	Pull-down resistors are incorporated.	Stand-by input. H: Stand-by mode L: Operation mode.
41	SEL	I	Pull-down resistors are incorporated.	Controls the CLP signal polarity. H: CLP is High active L: CLP is Low active.
42	CLE	I	Pull-down resistors are incorporated.	Clamp enable input. H: Enable L: Disable.
43	CLP	I	Pull-down resistors are incorporated.	Clamp pulse input. The polarity can be set to either High or Low by setting SEL.
44	CLK	I	Pull-down resistors are incorporated.	Clock input.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage, AV_{CC} or DV_{CC} to AGND or DGND 4V
DGND to AGND 0.3V
Digital I/O Pins . . . . . DGND to DV_{CC}
Analog I/O Pins . . . . . AGND to AV_{CC}

Operating Conditions

Temperature Range
HI2325IN . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
48 Ld MQFP	84

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$A_{VDD} = D_{VDD} = +3.3V$; $V_{IN} = 1.50V$; $f_S = 40MSPS$ at 50% Duty Cycle; $C_L = 10pF$; $T_A = 25^oC$; Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY					
Resolution		8	-	-	Bits
Integral Linearity Error, INL	f_{IN} = 1MHz	-	0.2	-	LSB
Differential Linearity Error, DNL (Guaranteed No Missing Codes)	f_{IN} = 1MHz	-	±0.7	-	LSB
Offset Error, V_{OS}	f_{IN} = DC	-50	-	50	mV
Full Scale Error, FSE	f_{IN} = DC	-	1	-	LSB
DYNAMIC CHARACTERISTICS					
Minimum Conversion Rate	No Missing Codes	1	-	-	MSPS
Maximum Conversion Rate	No Missing Codes	40	-	-	MSPS
Effective Number of Bits, ENOB	f_{IN} = 1MHz	-	6.5	-	Bits
Signal to Noise and Distortion Ratio, SINAD $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	f_{IN} = 1MHz	-	41	-	dB
Signal to Noise Ratio, SNR $= \frac{\text{RMS Signal}}{\text{RMS Noise}}$	f_{IN} = 1MHz	-	42.5	-	dB
Total Harmonic Distortion, THD	f_{IN} = 1MHz	-	-46	-	dBc
2nd Harmonic Distortion	f_{IN} = 1MHz	-	-48	-	dBc
3rd Harmonic Distortion	f_{IN} = 1MHz	-	-52	-	dBc
Spurious Free Dynamic Range, SFDR	f_{IN} = 1MHz	-	48.5	-	dBc
Intermodulation Distortion, IMD	f_1 = 1MHz, f_2 = 1.02MHz	-	-	-	dBc
I/Q Channel Crosstalk		-	-75	-	dBc
I/Q Channel Offset Match		-	1.0	-	LSB
I/Q Channel Full Scale Error Match		-	0.25	-	LSB
Transient Response	(Note 2)	-	1	-	Cycle
Over-Voltage Recovery	0.2V Overdrive (Note 2)	-	1	-	Cycle
ANALOG INPUT					
Maximum Peak-to-Peak Single-Ended Analog Input Range		-	1.0	-	V
Analog Input Resistance, R_{INA} or R_{INB}	V_{INA}, V_{INB} = V_{REF}, DC	-	-	-	MΩ
Analog Input Capacitance, C_{INA} or C_{INB}	V_{INA}, V_{INB} = 1.5V, DC	-	-	-	pF

Electrical Specifications $A_{VDD} = D_{VDD} = +3.3V$; $V_{IN} = 1.50V$; $f_S = 40MSPS$ at 50% Duty Cycle; $C_L = 10pF$; $T_A = 25^oC$; Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Analog Input Bias Current, I_BA or I_BB	V_{INA}/V_{INB} = ART/BRT, ARB/BRB, DC (Notes 2, 3)	-	-	-	µA
Full Power Input Bandwidth, FPBW	f_S = 40MHz, (Note 2)	-	-	-	MHz
REFERENCE VOLTAGE INPUT					
Reference Voltage Input Range		-	-	-	V
Total Reference Resistance, R_{RIN}		-	370	-	kΩ
Reference Current, I_{RIN}		-	5.4	-	mA
Self Bias	V_{RB}	-	0.54	-	
	V_{RT}	-	1.9	-	
SAMPLING CLOCK INPUT					
Input Logic High Voltage, V_{IH}	CLK	2.0	-	-	V
Input Logic Low Voltage, V_{IL}	CLK	-	-	0.8	V
Input Logic High Current, I_{IH}	CLK, V_{IH} = 3.3V	-	-	-	µA
Input Logic Low Current, I_{IL}	CLK, V_{IL} = 0V	-	-	-	µA
Input Capacitance, C_{IN}	CLK	-	-	-	pF
DIGITAL OUTPUTS					
Output Logic High Voltage, V_{OH}	I_{OH} = 100µA; D_{VDD} = 3.3V	-	-	-	V
Output Logic Low Voltage, V_{OL}	I_{OL} = 1.5mA; D_{VDD} = 3.3V	-	-	-	V
Output Logic High Voltage, V_{OH}	I_{OH} = 100µA; D_{VDD} = 3.0V	-	-	-	V
Output Logic Low Voltage, V_{OL}	I_{OL} = 100µA; D_{VDD} = 3.0V	-	-	-	V
Output Capacitance, C_{OUT}		-	-	-	pF
TIMING CHARACTERISTICS					
Aperture Delay, t_{AP}		-	4	-	ns
Aperture Jitter, t_{AJ}		-	5	-	ps_{RMS}
Data Output Hold, t_H		-	10.7	-	ns
Data Output Delay, t_{OD}		-	11.7	-	ns
Data Latency, t_{LAT}	For a Valid Sample (Note 2)	2	2	2	Cycles
Power-Up Initialization	Data Invalid Time (Note 2)	-	-	-	Cycles
Sample Clock Pulse Width (Low)	(Note 2)	11.25	12.5	-	ns
Sample Clock Pulse Width (High)	(Note 2)	11.25	12.5	-	ns
Sample Clock Duty Cycle Variation		-	±5	-	%
POWER SUPPLY CHARACTERISTICS					
Analog Supply Voltage, A_{VDD}	(Note 2)	3.0	3.3	3.6	V
Digital Supply Voltage, D_{VDD}	(Note 2)	3.0	3.3	3.6	V
Supply Current, I_{DD}	f_S = 40MSPS	-	30.3	-	mA
Power Dissipation		-	100	-	mW
Offset Error Sensitivity, ΔV_{OS}	A_{VDD} or D_{VDD} = 3.3V ±5%	-	±0.125	-	LSB
Gain Error Sensitivity, ΔFSE	A_{VDD} or D_{VDD} = 3.3V ±5%	-	±0.15	-	LSB

NOTES:

2. Parameter guaranteed by design or characterization and not production tested.
3. With the clock low and DC input.

TABLE 1. OUTPUT MODE

INPUT			OUTPUT							
TEST	STB	2S/B	A7 B7	A6 B6	A5 B5	A4 B4	A3 B3	A2 B2	A1 B1	A0 B0
L	L	L	Binary Code							
L	L	H	2's Compliment Code							
L	H	X	Hi-Z							
H	X	X	Test Mode							

TABLE 2. DIGITAL OUTPUT

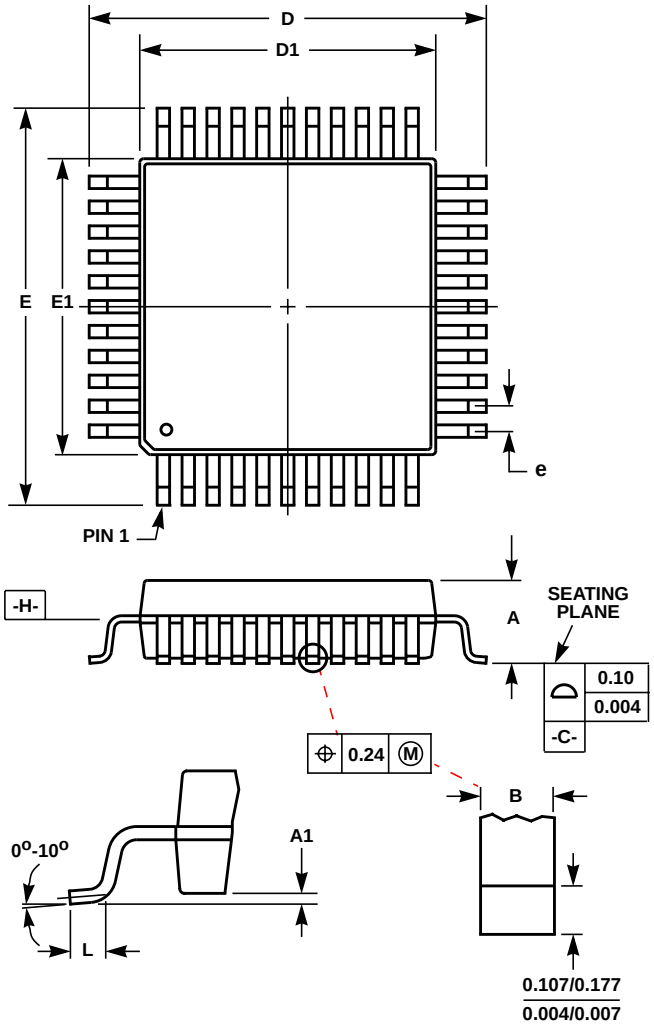
The following table shows the relationship between analog input voltage and digital output code.

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE			
		BINARY CODE		2's COMPLIMENT CODE	
		MSB	LSB	MSB	LSB
VART, VBRT	255	11111111		011111111	
:	:	:		:	
:	128	10000000		00000000	
:	127	01111111		11111111	
:	:	:		:	
VARB, VBRB	0	00000000		10000000	

TABLE 3. DIGITAL CLAMP REFERENCE LEVEL

SETTING			REFERENCE LEVEL			
REF2	REF1	REF0	MODE	DECIMAL	BINARY	2's COMPLIMENT
L	L	L	0	1	00000001	10000001
L	L	H	1	16	00010000	10010000
L	H	L	2	32	00100000	10100000
L	H	H	3	128	10000000	00000000
H	L	L	4	254	11111110	01111110
H	L	H	5	239	11101111	01101111
H	H	L	6	223	11011111	01011111
H	H	H	7	127	01111111	11111111

Metric Plastic Quad Flatpack Packages (MQFP/PQFP)



Q48.7x7-S

48 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.056	0.066	1.40	1.70	-
A1	0.000	0.007	0.00	0.20	-
B	0.006	0.010	0.15	0.26	5
D	0.347	0.362	8.80	9.20	2
D1	0.272	0.279	6.90	7.10	3, 4
E	0.347	0.362	8.80	9.20	2
E1	0.272	0.279	6.90	7.10	3, 4
L	0.012	0.027	0.30	0.70	-
N	48		48		6
e	0.020 BSC		0.500 BSC		-

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NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. Dimensions D and E to be determined at seating plane -C-.
3. Dimensions D1 and E1 to be determined at datum plane -H-.
4. Dimensions D1 and E1 do not include mold protrusion.
5. Dimension B does not include dambar protrusion.
6. “N” is the number of terminal positions.

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