16-port Dual-Speed Ethernet Switch Controller

FEATURES

- Single chip 16-port 10/100M wire speed Ethernet switching controller with all memory embedded
- Integration of 16-port dual speed, full/half duplex capable Media Access Controllers (MACs) with RMII interfaces
- Support IEEE 802.3x compliant flow control for FDX and back-pressure flow control for HDX
- Auto-negotiation through MDC/MDIO
- Support source/destination MAC address lookup and aging within built-in storage of 8K MAC address (4K entries each entry table)
- Self address learning, forwarding, and filtering schemes
- Store-and-Forward switching operation
- 12-group port base VLAN with port overlapping
- IEEE 802.1q CoS and two priority queues support based on port, tagging, and TOS configurations
- Address table and PHY register access allowed through CPU processor
- Dynamic buffer management
- No head-of-line blocking system support
- Power on self diagnostic
- Serial EEPROM (93C46) interface for auto-configuration
- Broadcast storm prevention
- Serial CPU interface support for system configuration required
- Three alter/self-diagnostic LED interface
- CMOS, 1.8/3.3V I/O tolerance
- 208 PQFP package

GENERAL DESCRIPTION

MX98216EC is a stand-alone 10/100M Ethernet switch controller with SRAM embedded which saves at least one 64KX64 SRAM cost. Any standalone desktop or enterprising Ethernet switches can be achieved by simply combining MX98216EC and quad/octal physical devices. All 16 ports are full duplex capable to provide dedicated 20/200M bandwidth connections each port. MX98216EC basically supports store-and-forward switching scheme with two address entry tables, 4K size each. The function modules integrated in controller include 16-port half/full-duplex compatible media access controller with RMII interface, address resolution logic (ARL) for address learning, filtering, recognition, priority queue manager, port base VLAN. It fully complies with IEEE Std. 802.3/802.3u/802.1q specifications and supports MDC/MDIO interface for physical layer management with industrial standard physical devices.

The switch architecture adopting dynamic buffer management shared by 16 ports can reach full-line speed of high performance application. To save system cost, single 50Mhz clock is for RMII and system requirement. MX98216EC proceeds in advanced foundry and smaller package which consumes lower power dissipation.

The smart features with low power CPU or EEPROM are for system configuration and ALR access required. Also, it emphasizes at Class of Service (CoS) which extracts various packet types in appropriate forwarding scheme. Now, Voice over IP (VoIP) is applied the feature for cutting voice packet latency and promise the quality of service. In addition, port-base VLAN is another valuable feature for the switches. MX98216EC offers 12 groups with port overlapping allowed. The feature can add on more security and data flow in the same switch with different groups should get connection through router. The powerful switching architecture and robust design can easily reach high performance, non-blocking data flow.

Head-of-line blocking prevents switch performance, and operation defective from other port impacts. The switch architecture provides a clean port independent operation. It guarantees port transmission or receive is not affected by other ports.

Moreover, user can discard broadcast packets regarding the threshold of system overload. This prevents potential broadcast storming from abnormal events. After buffer fullness drops in the safe margin, the switch controller jumps into flow control state to allow physical ports work as normal condition.

MX98216EC provides self on test as soon as power on or reset. It will detect all buffer memory and address table and others. If defective, LED is automatically on. Several LEDs are defined in switch controller like status of broadcast storm, packet loss, and buffer full.

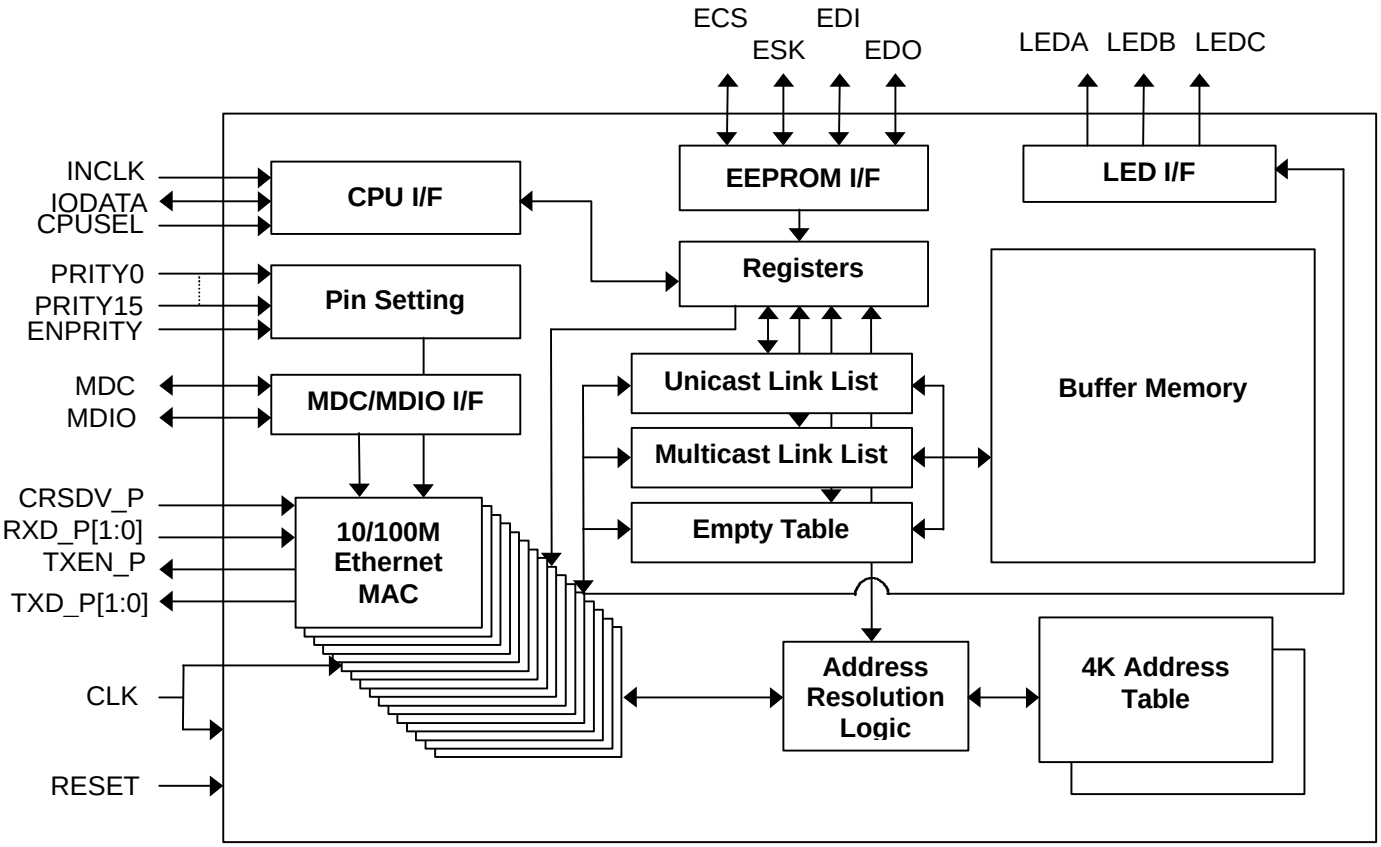


Figure 1. MX98216EC Functional Block Diagram

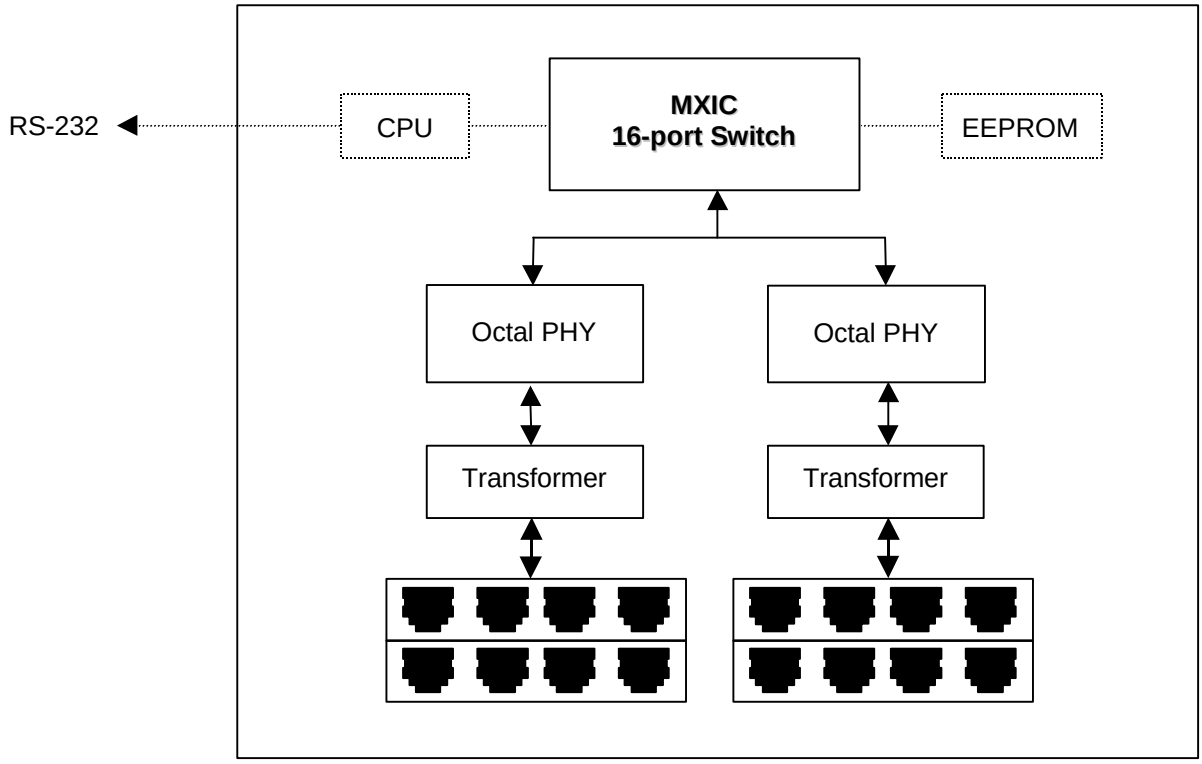


Figure 2. MX98216EC System Block Diagram

Optional Components

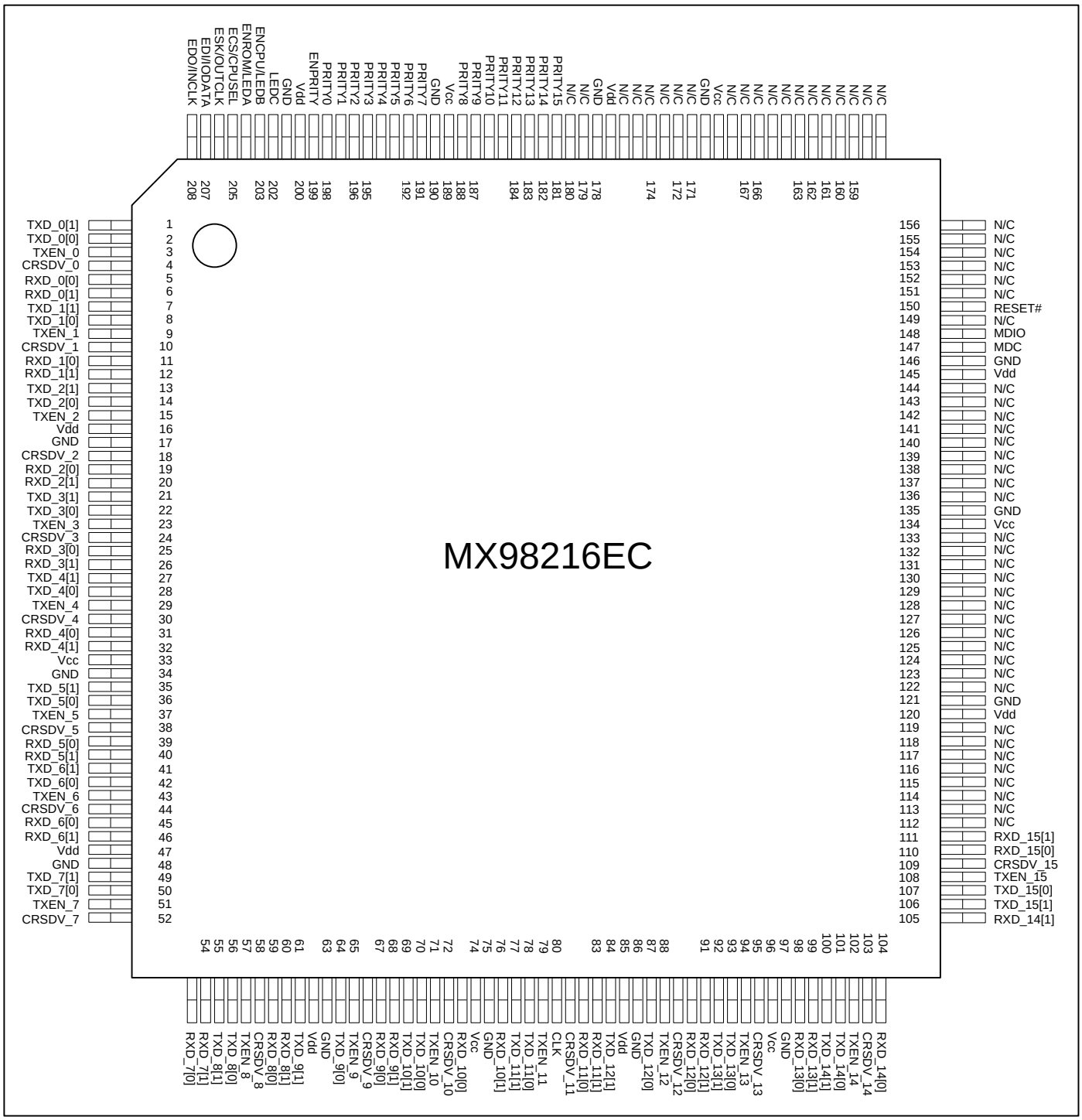


Figure 3. MX98216EC Pin Diagram Top View

PIN DESCRIPTION

10/100Mbps RMII INTERFACE

PIN#	PIN NAME	I/O	DESCRIPTION
4 10 18 24 30 38 44 52 58 66 72 81 89 95 103 109	CRSDV_0 CRSDV_1 CRSDV_2 CRSDV_3 CRSDV_4 CRSDV_5 CRSDV_6 CRSDV_7 CRSDV_8 CRSDV_9 CRSDV_10 CRSDV_11 CRSDV_12 CRSDV_13 CRSDV_14 CRSDV_15	I	Carrier Sense/Receive Data Valid Active high, indicate receive medium is non-idle. CRSDV is asserted asynchronously with respect to CLK.
6, 5 12, 11 20, 19 26, 25 32, 31 40, 39 46, 45 54, 53 60, 59 68, 67 76, 73 83, 82 91, 90 99, 98 105, 104 111, 110	RXD_0[1:0] RXD_1[1:0] RXD_2[1:0] RXD_3[1:0] RXD_4[1:0] RXD_5[1:0] RXD_6[1:0] RXD_7[1:0] RXD_8[1:0] RXD_9[1:0] RXD_10[1:0] RXD_11[1:0] RXD_12[1:0] RXD_13[1:0] RXD_14[1:0] RXD_15[1:0]	I	Receive Data From Port 0 to Port 23, synchronous to CLK and RXD[1] is MSB. While CRSDV is deasserted, RXD[1:0] is "00".
3 9 15 23 29 37 43 51 57 65 71 79 88 94 102 108	TXEN_0 TXEN_1 TXEN_2 TXEN_3 TXEN_4 TXEN_5 TXEN_6 TXEN_7 TXEN_8 TXEN_9 TXEN_10 TXEN_11 TXEN_12 TXEN_13 TXEN_14 TXEN_15	O 4mA	Transmit Enable Active high, assertion indicates the MAC is presenting di-bits on TXD[1:0] for transmission. TXEN is asserted synchronously with first nibble of preamable and remained asserted while all di-bits transmitted are presented on RMII. TXEN is negated prior to 1st CLK rising edge following the final di-bit of frame.

1, 2 7, 8 13, 14 21, 22 27, 28 35, 36 41, 42 49, 50 55, 56 61, 64 69, 70 77, 78 84, 87 92, 93 100, 101 106, 107	TXD_0[1:0] TXD_1[1:0] TXD_2[1:0] TXD_3[1:0] TXD_4[1:0] TXD_5[1:0] TXD_6[1:0] TXD_7[1:0] TXD_8[1:0] TXD_9[1:0] TXD_10[1:0] TXD_11[1:0] TXD_12[1:0] TXD_13[1:0] TXD_14[1:0] TXD_15[1:0]	O 4mA	Transmit Data From Port 0 to Port 23, synchronous to CLK and TXD[1] is MSB. When TXEN is asserted, TXD[1:0] are accepted fro transmission. TXD[1:0] is "00" when TXEN is deasserted.
80	CLK	I	Reference Clock For RMII and system clock use. 50MHz.
Subtotal			97

EEPROM INTERFACE

PIN#	PIN NAME	I/O	DESCRIPTION
204	ENROM	I	EEPROM Enable Internally pull down. Default disable. Active high; indicated configuration data is auto-loaded from EEPROM after reset. Tying this pin to ground disables EEPROM interface and prevents auto-configuration.
205	ECS	O 4mA	EEPROM Chip Select Active high.
206	ESK	O 8mA	EEPROM Clock 390KHz derived from system clock.
207	EDI	O 4mA	EEPROM Data Input Output data to the corresponding EDI pin of EEPROM.
208	EDO	I	EEPROM Data Output Input data to the corresponding EDO pin of EEPROM.
Subtotal			5

CoS PRIORITY SETTING

PIN#	PIN NAME	I/O	DESCRIPTION
199	ENPRITY	I	Priority Queue Enable Internally pull down. Per port base pin setting priority function enable. If the pin is enabled, per port base priority settings used by EEPROM or CPU is invalid. Port base priority settings controlled by EEPROM or CPU will be valid when the pin is pull down.

198-191 188-181	PRITY0 PRITY1 PRITY2 PRITY3 PRITY4 PRITY5 PRITY6 PRITY7 PRITY8 PRITY9 PRITY10 PRITY11 PRITY12 PRITY13 PRITY14 PRITY15	I	Per Port Priority Enable Active low. If pin pull high, the mapped port will act as high priority.
Subtotal			17

CPU INTERFACE

PIN#	PIN NAME	I/O	DESCRIPTION
203	ENCPU	I	CPU Interface Enable Internally pull down. At reset, the pin is latched as CPU interface enable.
205	CPUSEL	I	CPU Selection The selected chip enable from CPU.
206	OUTCLK	O 8mA	CPU Input Clock The switch generates 8.3MHz serial clock to CPU.
207	IODATA	I/O 4mA	CPU Data Input/Output CPU read/write data & command.
208	INCLK	I	CPU Output Clock CPU generates 8.3MHz serial clock to Ethernet switch.
Subtotal			5

LED INTERFACE

PIN#	PIN NAME	I/O	DESCRIPTION
204	LEDA	O 8mA	Address Table Self-test/Buffer Full LED Internally pull down. Initially, after power on or reset, address table will be tested and LEDC (Reset function) is keeping on until internal test finished. If any error found in address table, LEDA will keep on. After LEDC off, the switch is functional. If global buffer utilization is full within previous 40ms intervals, LEDA will be on 40ms. It will keep on if the buffer utilization keeps full within current intervals.

203	LEDB	O 8mA	Buffer Memory Test/Packet Loss LED Internally pull down. If power on or reset, LEDC (Reset function) is keeping on and all buffer memory will be tested. If buffer memory has an error found, LEDB will be on. After LEDB and LEDC off, switch self-test is done. If packet loss found, LEDB is keeping on 40ms within each 40ms time intervals.
202	LEDC	O 8mA	Reset/Broadcast Storm LED Internally pull up. If reset, LEDC is on until all internal memory test finished. Then, the pin will show the status of broadcast storm packets. If the number of broadcast packets stored in switch over threshold within 40ms time intervals, LEDC will be on 40ms. It will be shown until broadcast storm released.
Subtotal			3

MISCELLANEOUS

PIN#	PIN NAME	I/O	DESCRIPTION
147	MDC	I/O 16mA	Management Data Clock Internal pull down. The pin provides 2.5MHz clock for MDIO.
148	MDIO	I/O 16mA	Management Data Bi-directional RMII management port data pin. MDIO is synchronous with respect to MDC and is sampled on the rising edge of MDC.
150	RESET#	I	Chip Reset Active low; be held low for some time after power-on.
33, 74, 96, 134, 169, 189,	Vcc		1.8V Core Power
16, 47, 62, 85, 120, 145, 177, 200	Vdd		3.3V I/O Power
17, 34, 48, 63, 75, 86, 97, 121, 135, 146, 170, 178, 190, 201	GND		Ground
Subtotal			31

EEPROM AND CPU CONTROL REGISTERS

OFFSET	REGISTER	OFFSET	REGISTER
0x00H	Port Base VLAN Group 0 (0-11)	0x1AH	Configuration 1
0x01H	Port Base VLAN Group 0 (12-15)	0x1BH	Aging Timer
0x02H	Port Base VLAN Group 1 (0-11)	0x1CH	Reserved
0x03H	Port Base VLAN Group 1 (12-15)	0x1DH	802.3x Pause Frame Timer
0x04H	Port Base VLAN Group 2 (0-11)	0x1EH	MAC Address 0
0x05H	Port Base VLAN Group 2 (12-15)	0x1FH	MAC Address 1
0x06H	Port Base VLAN Group 3 (0-11)	0x20H	MAC Address 2
0x07H	Port Base VLAN Group 3 (12-15)	0x21H	IP/VLAN Tagging Base Priority (0-7)
0x08H	Port Base VLAN Group 4 (0-11)	0x22H	IP/VLAN Tagging Base Priority (8-15)
0x09H	Port Base VLAN Group 4 (12-15)	0x23H	Reserved
0x0AH	Port Base VLAN Group 5 (0-11)	0x24H	Reserved
0x0BH	Port Base VLAN Group 5 (12-15)	0x25H	Reserved
0x0CH	Port Base VLAN Group 6 (0-11)	0x26H	Reserved
0x0DH	Port Base VLAN Group 6 (12-15)	0x27H	LED Control & VLAN Group Reset
0x0EH	Port Base VLAN Group 7 (0-11)	0x28H	CPU Access Data
0x0FH	Port Base VLAN Group 7 (12-15)	0x29H	PHY/Address Table Operation Command
0x10H	Port Base VLAN Group 8 (0-11)	0x2AH	Flow Control Enable (8-15)
0x11H	Port Base VLAN Group 8 (12-15)	0x2BH	Reserved
0x12H	Port Base VLAN Group 9 (0-11)	0x2CH	Flow Control Enable (0-7)
0x13H	Port Base VLAN Group 9 (12-15)	0x2DH	Reserved
0x14H	Port Base VLAN Group 10 (0-11)	0x2EH	Reserved
0x15H	Port Base VLAN Group 10 (12-15)	0x2FH	Reserved
0x16H	Port Base VLAN Group 11 (0-11)	0x30H	Auto-negotiation Disable (0-15)
0x17H	Port Base VLAN Group 11 (12-15)	0x31H	Force Speed Setting (0-7)
0x18H	Configuration 0 & Port Base Priority (0-7)	0x32H	Force Speed Setting (8-15)
0x19H	Port Base Priority (8-15)	0x33H	Force Half/Full Duplex Setting (0-15)

Note : 1. 93C46 EEPROM must be in 16-bit mode
2. The contents of EEPROM and CPU access registers are the same as following descriptions
3. (A-B) means port number setting from A to B

Port Base VLAN Group 0 (0-11) (Reg00H), default = 0x0FFFH

BIT	DESCRIPTION	TYPE	DEFAULT
0.11-0	Port 0-11 VLAN Group 0 Default 1; all ports are into single group. One bit per port; e.g. bit 0 for port 0 and bit 11 for port 11. 0 : disable; to be treat as an isolated port 1 : enable; to be a group 0 member	R/W	0xFFF
0.15-12	N/A		

Port Base VLAN Group 0 (12-15) (Reg01H), default = 0x0FFFH

BIT	DESCRIPTION	TYPE	DEFAULT
1.3-0	Port 12-15 VLAN Group 0 Default 1; all ports are into single group. One bit per port; e.g. bit 0 for port 12 and bit 3 for port 15. 0 : disable; to be treat as an isolated port 1 : enable; to be a group 0 member	R/W	0xF
1.15-4	N/A		

Port Base VLAN Group 1 (0-11) (Reg02H), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
2.11-0	Port 0-11 VLAN Group 1 Default 0; group 1 not in use if all zero. One bit per port; e.g. bit 0 for port 0 and bit 11 for port 11. 0 : disable; to be treat as an isolated port 1 : enable; to be a group 1 member	R/W	0x000
2.15-12	N/A		

Port Base VLAN Group 1 (12-15) (Reg03H), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
3.3-0	Port 12-15 VLAN Group 1 Default 0; group 1 not in use if all zero. One bit per port; e.g. bit 0 for port 12 and bit 3 for port 15. 0 : disable; to be treat as an isolated port 1 : enable; to be a group 1 member	R/W	0x0
3.15-4	N/A		

Port Base VLAN Group 2 (0-11) (Reg04H), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
4.11-0	Port 0-11 VLAN Group 2 Default 0; group 2 not in use if all zero. One bit per port; e.g. bit 0 for port 0 and bit 11 for port 11. 0 : disable; to be treat as an isolated port 1 : enable; to be a group 2 member	R/W	0x000
4.15-12	N/A		

Port Base VLAN Group 2 (12-15) (Reg05H), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
5.3-0	Port 12-15 VLAN Group 2 Default 0; group 2 not in use if all zero. One bit per port; e.g. bit 0 for port 12 and bit 3 for port 15. 0 : disable; to be treat as an isolated port 1 : enable; to be a group 2 member	R/W	0x0
5.15-4	N/A		

Port Base VLAN Group 3 (0-11) (Reg06H), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
6.11-0	Port 0-11 VLAN Group 3 Default 0; group 3 not in use if all zero. One bit per port; e.g. bit 0 for port 0 and bit 11 for port 11. 0 : disable; to be treat as an isolated port 1 : enable; to be a group 3 member	R/W	0x000
6.15-12	N/A		

Port Base VLAN Group 3 (12-15) (Reg07H), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
7.3-0	Port 12-15 VLAN Group 3 Default 0; group 3 not in use if all zero. One bit per port; e.g. bit 0 for port 12 and bit 3 for port 15. 0 : disable; to be treat as an isolated port 1 : enable; to be a group 3 member	R/W	0x0
7.15-4	N/A		

Port Base VLAN Group 4 (0-11) (Reg08H), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
8.11-0	Port 0-11 VLAN Group 4 Default 0; group 4 not in use if all zero. One bit per port; e.g. bit 0 for port 0 and bit 11 for port 11. 0 : disable; to be treat as an isolated port 1 : enable; to be a group 4 member	R/W	0x000
8.15-12	N/A		

Port Base VLAN Group 4 (12-15) (Reg09H), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
9.3-0	Port 12-15 VLAN Group 4 Default 0; group 4 not in use if all zero. One bit per port; e.g. bit 0 for port 12 and bit 3 for port 15. 0 : disable; to be treat as an isolated port 1 : enable; to be a group 4 member	R/W	0x0
9.15-4	N/A		

Port Base VLAN Group 5 (0-11) (Reg0AH), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
A.11-0	Port 0-11 VLAN Group 5 Default 0; group 5 not in use if all zero. One bit per port; e.g. bit 0 for port 0 and bit 11 for port 11. 0 : disable; to be treat as an isolated port 1 : enable; to be a group 5 member	R/W	0x000
A.15-12	N/A		

Port Base VLAN Group 5 (12-15) (Reg0BH), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
B.3-0	Port 12-15 VLAN Group 5 Default 0; group 5 not in use if all zero. One bit per port; e.g. bit 0 for port 12 and bit 3 for port 15. 0 : disable; to be treat as an isolated port 1 : enable; to be a group 5 member	R/W	0x0
B.15-4	N/A		

Port Base VLAN Group 6 (0-11) (Reg0CH), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
C.11-0	Port 0-11 VLAN Group 6 Default 0; group 6 not in use if all zero. One bit per port; e.g. bit 0 for port 0 and bit 11 for port 11. 0 : disable; to be treat as an isolated port 1 : enable; to be a group 6 member	R/W	0x000
C.15-12	N/A		

Port Base VLAN Group 6 (12-15) (Reg0DH), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
D.3-0	Port 12-15 VLAN Group 6 Default 0; group 6 not in use if all zero. One bit per port; e.g. bit 0 for port 12 and bit 3 for port 15. 0 : disable; to be treat as an isolated port 1 : enable; to be a group 6 member	R/W	0x0
D.15-4	N/A		

Port Base VLAN Group 7 (0-11) (Reg0EH), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
E.11-0	Port 0-11 VLAN Group 7 Default 0; group 7 not in use if all zero. One bit per port; e.g. bit 0 for port 0 and bit 11 for port 11. 0 : disable; to be treat as an isolated port 1 : enable; to be a group 7 member	R/W	0x000
E.15-12	N/A		

Port Base VLAN Group 7 (12-15) (Reg0FH), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
F.3-0	Port 12-15 VLAN Group 7 Default 0; group 7 not in use if all zero. One bit per port; e.g. bit 0 for port 12 and bit 3 for port 15. 0 : disable; to be treat as an isolated port 1 : enable; to be a group 7 member	R/W	0x0
F.15-4	N/A		

Port Base VLAN Group 8 (0-11) (Reg10H), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
10.11-0	Port 0-11 VLAN Group 8 Default 0; group 8 not in use if all zero. One bit per port; e.g. bit 0 for port 0 and bit 11 for port 11. 0 : disable; to be treat as an isolated port 1 : enable; to be a group 8 member	R/W	0x000
10.15-12	N/A		

Port Base VLAN Group 8 (12-15) (Reg11H), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
11.3-0	Port 12-15 VLAN Group 8 Default 0; group 8 not in use if all zero. One bit per port; e.g. bit 0 for port 12 and bit 3 for port 15. 0 : disable; to be treat as an isolated port 1 : enable; to be a group 8 member	R/W	0x0
11.15-4	N/A		

Port Base VLAN Group 9 (0-11) (Reg12H), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
12.11-0	Port 0-11 VLAN Group 9 Default 0; group 9 not in use if all zero. One bit per port; e.g. bit 0 for port 0 and bit 11 for port 11. 0 : disable; to be treat as an isolated port 1 : enable; to be a group 9 member	R/W	0x000
12.15-12	N/A		

Port Base VLAN Group 9 (12-15) (Reg13H), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
13.3-0	Port 12-15 VLAN Group 9 Default 0; group 9 not in use if all zero. One bit per port; e.g. bit 0 for port 12 and bit 3 for port 15. 0 : disable; to be treat as an isolated port 1 : enable; to be a group 9 member	R/W	0x0
13.15-4	N/A		

Port Base VLAN Group 10 (0-11) (Reg14H), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
14.11-0	Port 0-11 VLAN Group 10 Default 0; group 10 not in use if all zero. One bit per port; e.g. bit 0 for port 0 and bit 11 for port 11 0 : disable; to be treat as an isolated port 1 : enable; to be a group 10 member	R/W	0x000
14.15-12	N/A		

Port Base VLAN Group 10 (12-15) (Reg15H), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
15.3-0	Port 12-15 VLAN Group 10 Default 0; group 10 not in use if all zero. One bit per port; e.g. bit 0 for port 12 and bit 3 for port 15. 0 : disable; to be treat as an isolated port 1 : enable; to be a group 10 member	R/W	0x0
15.15-4	N/A		

Port Base VLAN Group 11 (0-11) (Reg16H), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
16.11-0	Port 0-11 VLAN Group 11 Default 0; group 11 not in use if all zero. One bit per port; e.g. bit 0 for port 0 and bit 11 for port 11 0 : disable; to be treat as an isolated port 1 : enable; to be a group 11 member	R/W	0x000
16.15-12	N/A		

Port Base VLAN Group 11 (12-15) (Reg17H), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
17.3-0	Port 12-15 VLAN Group 11 Default 0; group 11 not in use if all zero. One bit per port; e.g. bit 0 for port 12 and bit 3 for port 15 0 : disable; to be treat as an isolated port 1 : enable; to be a group 11 member	R/W	0x0
17.15-4	N/A		

Configuration 0 and Port Base Priority (0-7) (Reg18H), default = 0x0022H

BIT	DESCRIPTION	TYPE	DEFAULT
18.0	Continuous 16-time Collision Drop Disable 0 : packet that runs into 16 consecutive collision will be dropped 1 : packet that runs into 16 consecutive collision will NOT be dropped	R/W	0
18.1	Timeout disable 0 : packet will NOT be dropped if packet has been queued over 1 second 1 : packet will be dropped in spite of packet being queue over 1 second	R/W	1
18.3-2	CRC Hashing Selection 48-bit DA/SA address is translated separated into 12-bit entry pointer of address table for address learning and recognition. The translation is by aid of CRC generator within the switch controller. The index of entry pointer selection is defined by: 00 : bit [11:0] of CRC are selected 01 : bit [16:5] of CRC are selected 10 : bit [24:13] of CRC are selected 11 : bit [30:19] of CRC are selected	R/W	00
18.4	Direct Mapping It means bit [63:52] of DA/SA address directly as an index of address table. 0 : CRC calculation to get the hashing index of address table 1 : direct mapping enable	R/W	1
18.5	Reserved	R/W	0
18.6	N/A		
18.7	Reserved	R/W	1
18.15-8	Port 0-7 Priority Port base priority settings from port 0 to port 7. If external pins of port base priority are set, the content of EEPROM or CPU will be overridden. One bit per port; e.g. bit 8 for port 0 and bit 15 for port 7. 0 : disable 1 : enable, the port of packets always in high priority	R/W	0x00H

Port Base Priority (8-15) (Reg19H), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
19.7-0	Port 8-15 Priority Port base priority settings from port 8 to port 15. If external pins of port base priority are set, the content of EEPROM or CPU will be overridden. One bit per port; e.g. bit 0 for port 8 and bit 7 for port 15. 0 : disable 1 : enable, the port of packets always in high priority	R/W	0x00H
19.15-8	N/A		

Configuration 1 (Reg1AH), default = 0x502EH

BIT	DESCRIPTION	TYPE	DEFAULT
1A.3-0	Reserved	R/W	0xFH
1A.5-4	Backoff Operation Mode In normal backoff algorithm, packet transmission delays a random time within 2^n –1 slot time (1 slot time = 512 bit times) when collision occurs. The switch provides some modification of backoff algorithm to improve Ethernet performance on half- duplex connection. 00 : standard operation. 01 : first two collisions follow standard backoff. More than two collisions in transmission, packet resend delays 0-3 slot times. 10 : packet resend delays 0 slot time only when port buffer full. 11 : packet resend delays 0 slot time all the time.	R/W	00
1A.6	Back Pressure Disable Enable back pressure on half duplex connection for all ports 0 : enable 1 : disable	R/W	0
1A.7	N/A		
1A.8	Reserved	R/W	0
1A.14-9	High/Low Priority Ratio Bit 9 to 11 means a decimal value for low priority packets to be transmitted whereas bit 12 to 14 to a decimal value for high priority packets. Followings are some example of high to low priority value.	R/W	0x28H

High Priority Value Bit 14	Bit 13	Bit 12	Low Priority Value Bit 11	Bit 10	Bit 9	Meaning
0/1	0/1	0/1	0	0	0	High priority port packets need to be sent first until empty; then, low priority packets
0	1	1	0	0	1	The transmission ratio of high to low priority packets is 3 : 1

1A.15	Aging Out Enable the function of aging out from address table. 0 : enable 1 : disable	R/W	0

Aging Timer (Reg1BH), default = 0x0005H

BIT	DESCRIPTION	TYPE	DEFAULT
1B.15-0	Aging timer provides for address table. The timer period is defined to age out the least unused entries on address table. The formula is age_timer (bit 0-15) X 65536 X 1ms. Here are some examples:	R/W	0x0005H

Bit 15 – Bit 0	Aging Timer	
0x0001H	65.5 sec	(around 1 min)
0x0005H	327.7 sec	(around 5.5 min)
0x001BH	1769.5 sec	(around 30 min)
0x0037H	3604.5 sec	(around 1 hr)

Reserved (Reg1CH), default = 0xC350H

BIT	DESCRIPTION	TYPE	DEFAULT
1C.15-0	Reserved	R/W	0xC350H

802.3x Pause Frame Timer (Reg1DH), default = 0x01FFH

BIT	DESCRIPTION	TYPE	DEFAULT
1D.4-0	Reserved	R/W	0x1FH
1D.15-5	Flow Control Counter The timer determines the period, namely "pause time", to inhibit packet transmission from attached host for flow control. The variable pause time of pause frame is equal to the decimal value times 32 plus 31 slot time.	R/W	0x1E0H

MAC Address 0 (Reg1EH), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
1E.15-0	Switch's MAC ID for address bit [15:0]	R/W	0x0000H

MAC Address 1 (Reg1FH), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
1F.15-0	Switch's MAC ID for address bit [31:16]	R/W	0x0000H

MAC Address 2 (Reg20H), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
20.15-0	Switch's MAC ID for address bit [47:32]	R/W	0x0000H

IP/VLAN Tagging Base Priority (0-7) (Reg21H), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
21.7-0	TOS (IP Base) Enable for port 0-7 to recognize the TOS field of IP priority packets. One bit per port; e.g. bit 0 for port 0 and bit 7 for port 7. 0 : disable 1 : enable	R/W	0x00H
21.15-8	TCI (VLAN Tagging Base) Enable for port 0-7 to recognize the TCI field of VLAN priority packets. One bit per port; e.g. bit 8 for port 0 and bit 15 for port 7. 0 : disable 1 : enable	R/W	0x00H

IP/VLAN Tagging Base Priority (8-15) (Reg22H), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
22.7-0	TOS (IP Base) Enable for port 8-15 to recognize the TOS field of IP priority packets. One bit per port; e.g. bit 0 for port 8 and bit 7 for port 15. 0 : disable 1 : enable	R/W	0x00H
22.15-8	TCI (VLAN Tagging Base) Enable for port 8-15 to recognize the TCI field of VLAN priority packets. One bit per port; e.g. bit 8 for port 8 and bit 15 for port 15. 0 : disable 1 : enable	R/W	0x00H

Reserved (Reg23H), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
23.15-0	Reserved	R/W	0x0000H

Reserved (Reg24H), default = 0xB081H

BIT	DESCRIPTION	TYPE	DEFAULT
24.15-0	Reserved	R/W	0xB081H

Reserved (Reg25H), default = 0x0040H

BIT	DESCRIPTION	TYPE	DEFAULT
25.15-0	Reserved	R/W	0x0040H

Reserved (Reg26H), default = 0x0082H

BIT	DESCRIPTION	TYPE	DEFAULT
26.15-0	Reserved	R/W	0x0082H

LED Control and VLAN Group Reset (Reg27H), default = 0x0200H

BIT	DESCRIPTION	TYPE	DEFAULT
27.0	Port Grouping Command When, initially, the execution of default values of the VLAN registers (Reg00H-17H) or VLAN grouping settings required via CPU/EEPROM, VLAN grouping contents need to write into the registers; then, grouping command is put into action. After grouping command is done, the bit will be self-clean to 0. 0 : Idle 1 : Port regrouping enable	R/W	0
27.2-1	Reserved	R/W	00
27.3	Broadcast Storm LED 0 : LED displays the broadcast storm symptom in high priority packets 1 : LED displays the broadcast storm symptom of all packets	R/W	1
27.4	Packet Loss LED 0 : LED displays the high priority packet loss 1 : LED displays all packet loss	R/W	1
27.15-5	N/A		0x010H

CPU Access Data (Reg28H), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
28.15-0	Access Data Generally, bit 15-0 is the access data for PHY registers and address table. In case, CPU requires to select PHY ID and register number before PHY register access. The starting PHY ID for the switch is 0. Bit 4-0 can be presented for PHY register number and bit 9-5 for PHY ID in address selection of PHY registers operation.	R/W	0x0000H

PHY/Address Table Operation Command (Reg29H), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
29.0	CPU Action If CPU takes read/write actions to address table or PHY registers, set the bit on. After action done, the bit will be self-clean to 0. 0 : Idle 1 : CPU action	R/W	0
29.1	CPU Read/Write Read or write action set to address table or PHY registers. 0 : Read operation 1 : Write operation	R/W	0
29.2	PHY/ALR Selection CPU access to PHY or address table 0 : PHY access 1 : Address table access	R/W	0

29.5-3	PHY/ALR Command In PHY register access 000 : A searching function for PHY ID and PHY register number when CPU access data filled relevant information. 001 : A command for switch internal control register to CPU access data based on read operation or a command for CPU access data to register to switch internal control register based on write operation. 100 : A command for content of PHY register to switch internal control register based on read operation or a command for switch internal control register to PHY register based on write operation. In address table access 000 : MAC ID for address bit [15:0] access from CPU access data to switch internal control register based on CPU write operation. It also can be MAC ID access bit [15:0] from switch internal control register to CPU access data based on CPU read operation. 001 : MAC ID for address bit [31:16] access from CPU access data to internal control register and based on CPU write operation; and vice versa. 010 : MAC ID for address bit [47:32] access from CPU access data to switch internal control register based on CPU write operation; and vice versa. 011 : Status of address table entry access like port number bit [8:4], aging timer bit [3:1], and valid bit [0] from switch internal control register to CPU access data based on CPU read operation. 100 : Based on read operation from content of an address table entry to switch internal control register or write operation from switch internal control register to content of an address table entry.	R/W	0x0H
29.10-6	Frozen Port The switch provides frozen function for an entry in address table; that is, an entry with learned MAC address and port number as an input will protect not to be aging out when the port number and assigned MAC have been set. Frozen function can only work on the first layer of address table. It's because the entry of second-layer of address table should be for dynamic MAC address. If frozen port sets to all one and CPU read/write command is one, the frozen MAC address will be released. If frozen port sets all one and CPU read/write command is zero, the host processor will read the content of second layer of address table.	R/W	0x00H
29.15-11	Reserved	R/W	0x00H

Flow Control Enable (8-15) (Reg2AH), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
2A.7-0	Flow Control Enable IEEE 802.3x flow control for port 8-15. One bit per port; e.g. bit 0 for port 8 and bit 7 for port 15. 0 : disable 1 : enable	R/W	0x00H
2A.15-8	N/A		

Reserved (Reg2BH), default = 0xFFFFH

BIT	DESCRIPTION	TYPE	DEFAULT
2B.15-0	Reserved	R/W	0xFFFFH

Flow Control Enable (0-7) (Reg2CH), default = 0x00FFH

BIT	DESCRIPTION	TYPE	DEFAULT
2C.7-0	Reserved	R/W	0xFFH
2C15-8	Flow Control Enable IEEE 802.3x flow control for port 0-7. One bit per port; e.g. bit 8 for port 0 and bit 15 for port 7. 0 : disable 1 : enable	R/W	0x00H

Reserved (Reg2DH), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
2D.15-0	Reserved	R/W	0x0000H

Reserved (Reg2EH), default = N/A

BIT	DESCRIPTION	TYPE	DEFAULT
2E.15-0	Reserved	RO	N/A

Reserved (Reg2FH), default = N/A

BIT	DESCRIPTION	TYPE	DEFAULT
2F.15-0	Reserved	RO	N/A

Auto-negotiation (0-15) (Reg30H), default = 0x0000H

BIT	DESCRIPTION	TYPE	DEFAULT
30.15-0	Auto-negotiation Disable Auto-negotiation operation of MDIO. When port base auto-negotiation disable, the switch port will not listen the final response from PHY. One bit per port; e.g. bit 0 for port 0 and bit 15 for port 15. 0 : enable auto-negotiation 1 : disable auto-negotiation	R/W	0x0000H

Force Speed Setting (0-7) (Reg31H), default = 0xFF00H

BIT	DESCRIPTION	TYPE	DEFAULT
31.7-0	N/A		
31.15-8	Force Speed Operation When auto-negotiation off, the port will be set at fixed speed. In EEPROM, force settings will be automatically written into PHY registers at initialization. Force settings by CPU requires extra CPU write operation into PHY; so port-base speed operations can keep consistency. One bit per port; e.g. bit 8 for port 0 and bit 15 for port 7. 0 : force 10Mbps 1 : force 100Mbps	R/W	0xFFH

Force Speed Setting (8-15) (Reg32H), default = 0xFFFFH

BIT	DESCRIPTION	TYPE	DEFAULT
32.7-0	Force Speed Operation One bit per port; e.g. bit 0 for port 8 and bit 7 for port 15. 0 : force 10Mbps 1 : force 100Mbps	R/W	0xFFH
32.15-8	N/A		

Force Half Duplex Setting (0-15) (Reg33H), default = 0xFFFFH

BIT	DESCRIPTION	TYPE	DEFAULT
33.15-0	Force Half Duplex Operation When auto-negotiation off, the port will be set at fixed duplex. In EEPROM, force settings will be automatically written into PHY registers at initialization. Force settings by CPU requires extra CPU write operation into PHY; so port-base duplex operations can keep consistency. One bit per port; e.g. bit 0 for port 0 and bit 15 for port 15. 0 : force half duplex 1 : force full duplex	R/W	0xFFFFH

FUNCTIONAL DESCRIPTION

Clocks

MX98216EC requires a unique 50MHz clock signal for both RMII and system requirement at CLK input pin. Also, the switch generates an 8.3MHz output clock to CPU and the processor feedback the same clock rate back to the switch. The 2.5MHz clock applies on MDC/MDIO interface and 390KHz refers EEPROM interface.

Reset

When power on, a hard reset is initiated by an active low pulse on RESET# pin. The initialization process loads all ports configurable parameters, resets internal state machines to idle, initializes embedded memory and address table. At the completion of the reset sequence, all ports are presented for packet transmission and reception.

RMII Interface

Reduced Media Independent Interface (RMII) comprises a low pin count intended for use between Ethernet PHYs and switch ASICs. The management interface (MDC/MDIO) is assumed to be identical to that defined in IEEE 802.3u. The RMII specification has been optimized for using in high port density interconnect devices which require independent treatment of the data paths. The primary motivator is a switch ASIC which requires independent data streams between the MAC and PHY.

CLK
CLK is a continuous clock that provides the timing reference for CRSDV_0-15, RXD_0-15[1:0], TXEN_0-15, and TXD_0-15[1:0]. The switch choose to provide CLK as an input for system and RMII use and each PHY device shall have an input corresponding to this clock but may use a single clock input for multiple PHYs implemented on a single IC.

Carrier Sense/Receive Data Valid
CRSDV_0-15 shall be asserted by the PHY when the receive medium is non-idle. The specifics of the definition of idle for 10BASE-T and 100BASE-X are contained in IEEE 802.3 and IEEE 802.3u. CRSDV0-15 is asserted asynchronously on detection of carrier due to the criteria relevant to the operating mode. That is, in 10BASE-T mode, when squelch is passed or, in 100BASE-X mode, when 2 non-contiguous zeroes in 10 bits are detected carrier is said to be detected. If the PHY has additional bits to be presented on RXD_0-15[1:0] following the initial deassertion of CRSDV_0-15, then the PHY shall assert CRSDV_0-15 on cycles of CLK which present the second di-bit of each nibble and deassert CRSDV_0-15 on cycles of CLK which present the first di-bit of a nibble.

Receive Data
RXD_0-15[1:0] shall transition synchronously to CLK. For each clock period in which CRSDV_0-15 is asserted, RXD_0-15[1:0] transfers two bits of recovered data from the PHY. In some cases, for example before data recovery or during error conditions, a pre-determined value for RXD_0-15[1:0] is transferred instead of recovered data. RXD_0-15[1:0] shall be “00” to indicate idle when CRSDV_0-15 is deasserted. Values other than “00” on RXD_0-15[1:0] while recovered from CRSDV_0-15 is de-asserted shall be ignored by the MAC. Upon assertion of CRSDV_0-15, the PHY shall ensure that RXD_0-15[1:0] is equal to ”00” until proper receive decoding takes place.

Transmit Enable
TXEN_0-15 indicates that the MAC is presenting di-bits on TXD_0-15[1:0] for transmission. TXEN_0-15 shall be asserted synchronously with the first nibble of the preamble and shall remain asserted while all di-bits to be transmitted are presented. TXEN_0-15 shall be negated prior to the first CLK rising edge following the final di-bit of a frame. TXEN_0-15 shall transition synchronously with respect to CLK.

Transmit Data
TXD_0-15[1:0] shall transition synchronously with respect to CLK. When TXEN_0-15 is asserted, TXD[1:0] are accepted for transmission by the PHY. TXD_0-15[1:0] shall be “00” to indicate idle when TXEN_0-15 is deasserted. Values other than “00” on TXD_0-15[1:0] while TXEN_0-15 is deasserted shall be ignored by the PHY.

PHY Management

The PHY determines the operation mode of each port, which are classified as 10Mbps-half duplex, 10Mbps-full duplex, 100Mbps-half duplex, 100Mbps-full duplex. The MAC of each port is connected to the PHY through RMII interface. The PHY starting ID mapped to the switch is zero. The switch supports PHY management through the serial MDC/MDIO interface. The switch will continuously read the registers of each PHY based on PHY ID to get the latest information such as link status, speed, operation mode of each port while it is in auto-negotiation. When a port of the switch forced at fixed operation mode, it will not listen any response from the PHY through MDC/MDIO so that consistent speed and duplex in PHY as well as switch is required in force operation mode.

Frame Reception

The frame received on 2-bit wide receive channel of RMII interface is queued in receive FIFO, and then stored into embedded buffer memory. Several error conditions will be identified during data reception.

1.Runt frame error, if the frame size is less than 64 bytes;
2.CRC error, if FCS is not matched to the result of CRC calculation;
3.Long frame error, if frame size is larger than 1536 bytes;
4.Alignment error, if frame length is of non-integral number of octets;

The above frames will be discarded. If no errors have been detected, the frame is stored and forwarded to egress port at wire speed. Several pages of buffer memory could be occupied for frame storage, on each page free memory is allocated. The data link management frames, namely IEEE 802.3x "pause" frame is recognized and no frame storage occurs.

Frame Transmission

Frame transmission begins while the output queue of physical port is not empty. The frame data is moved to output FIFO from embedded buffer memory, and converted to 2-bit stream through transmit channel of RMII interface. MX98216EC transmits frames in accordance to IEEE 802.3 standard. The egress port is responsible for preamble insertion, collision back-off, and inter packet gap keeping. While late collision happens on half-duplex port, the transmitted frame is aborted. If a packet has continuously met 16-time collisions, it will be dropped and the packet will be recovered by upper protocol. In full-duplex mode, the egress port ignores the signaling of carrier activity and collision detection on channel media.

Broadcast Storm Control

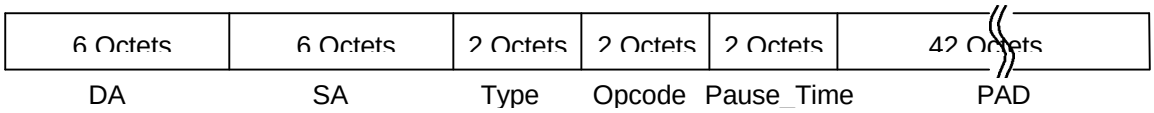
Three types of frames are viewed as broadcast frames in MX98216EC:

1. Received frame with DL_DA as FF-FF-FF-FF-FF-FF
2. Received frame with DL_DA as 1?-??-??-??-??-??
3. Received frame with unknown destination (unicast or multicast) address

To prevent network melted down, a state of complete network overload, due to broadcast storm (incorrect packet broadcast on a network that cause almost all hosts respond at once and hence storming the network with broadcast packets), users can program to restrict the storage amount of broadcast frames in MX98216EC. While the storage of broadcast frame goes over the threshold, the next coming broadcast frame(s) is dropped.

Flow Control

Flow control is implemented to avoid abnormal packet drop due to traffic congestion on egress ports. Basically, alternative back-pressure mechanism uses jam packet in half-duplex and 802.3x pause frame does in full-duplex mode. Flow control is active or inactive based on the internal per port and global reception thresholds in buffer. The switch implements standard 802.3x flow control whose frame is defined as follow.



802.3x PAUSE Frame Format

The diagram shown above is IEEE 802.3x pause frame format whereas DA presented for destination MAC adress, SA for source MAC address, pause frame type defined as 0x8808, opcode for pause operation (0x0001), default pause time for the switch to be 0x1FFF, and pad for all zero. The value of pause timer is changable by EEPROM or CPU. DA field of pause frame should be 0x0180C2000001 before transmission.

Address Learning and Recognition

After a good packet is received, address resolution logic begins address lookup. The destination MAC address and source MAC address associated are retrieved. The source MAC address is used to build up an address table. By searching the address table, if a unicast destination MAC address is recognized, the stored frame is forwarded to destined port. Initially, a unicast destination MAC address of a packet does not know the outgoing port number so that the stored frame is forwarded as a broadcast packet. In both of address learning and recognition, 48-bit MAC address is converted into a 12-bit search index via hash transformation. The switch offers two different hashing schemes; one is called direct mapping and the other is CRC mapping. In learning, an entry designated by the search index is checked to be valid or not. If non-valid, a new entry is generated with putting the information of source MAC address and ingress port number. A 2-layer structure is provided in learning mechanism. If valid, the 2-layer mechanism can keep 2 different MAC addresses in one certain entry to increase hashing resolution. If congestion found for an entry of the 2-layer structure, switch will compare the two numbers of the aging timer and replace the MAC record with older aging time to the new MAC. In recognition, the MAC address in table entry designated by search index is used to compare with destination MAC address. If both are matched, the associated port number in address table entry is the destination port. Otherwise, the received frame will be classified as a broadcast frame, and be flooded through every port (except source port). The memory space within MX98216EC can keep up to 8K MAC addresses. Aging mechanism is supported, namely the address information is aged out if not be referred in 300sec (default, the parameter is programmable). And, the entry of the record can be for newly learnt MACs kept in table.

2-priority Queue Class of Service (CoS)

Class of Service denotes the classification of traffic used to differentiate services among traffic classes. MX98216EC offers 2-level priority (High and Low) queues, which catch the priority information in the TOS field, port base, or VLAN tag in the incoming frames as standard IEEE 802.1Q defines. In this way, the switch controller guarantees the service for high priority frames to some extent, depending on the load condition of incoming traffic. (At least, the high priority service offers better than that of best effort service.) It also provides different service ratio settings for users to shape the prioritized frames on the streams in the incoming traffic.

Port-based VLAN

A Virtual LAN (VLAN) is a broadcast domain or a network segment which enables multiple stations on different physical locations to communicate with each other as if they were on the same LAN. With all the advantages such as increasing performance, bandwidth utilization efficiency and security as well as preventing broadcast storm, Port-Based VLAN is the most practical and economical form of VLAN.

MX98216EC supports up to 12 port-based VLAN groups which applies the overlapped VLAN scheme. That is, the 16 switch ports can be divided into 12 VLAN port-groups. By configuring the port with its VLAN membership, each port is assigned to one or more (up to 12) groups. Ports belonging to different groups are independent, which means

their network activity or fundamental network broadcasting will not affect or get distributed across those VLAN groups to each other. In this way, it can reduce the need for unwanted traffic in the network. Moreover, the damaged/abnormal ports can be isolated by removing them from VLAN groups' list, so as to prevent network meltdown. Port-based VLAN in MX98216EC is also very flexible that every port can be shared by multiple groups as the "trunk port" while the other unshared ports are remained independent.

Queue Management

MX98216EC utilizes the store-and-forward switching scheme, which needs memory for frame reception and transmission buffering. In MX98216EC, the embedded buffer memory is partitioned into pages which dynamically allocates the related frame data and switching information. The buffer management control unit dispatches pointers pointing to those pages upon frames reception of the egress ports.

For unicast frames, the occupied buffer pages are released after the corresponding ports complete transmission. Their pointers are returned to buffer management control unit for reuse. For broadcast frames, the switch controller count the times of transmission of the same broadcast frame till all ports finish the broadcast transmission, then the occupied memory space are released to the free buffer pool.

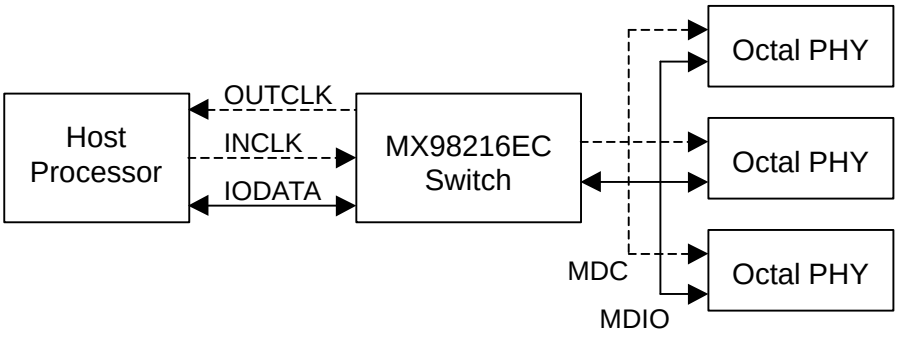
Since there are various kinds of page/pointer requests for the buffer management, a queue manager is used in MX98216EC to handle those access requests. Via a proprietary arbitration method, the queue manager grants fair enough throughput for each port to transmit at wire speed.

93C46 EEPROM Interface

Provide serial interface to load the values of external EEPROM which switch can configure in advance. At initial stage, switch will loads the data to internal registers and operates as expected. Either EEPROM or CPU interface can be used once a time.

CPU Interface

MX98216EC provides another powerful way to configure the value of register via CPU, which can access its as well as PHY registers and the address table at any time. Basically, MAC address look up, content of address table status and frozen a dedicated address are the major function for CPU access through address table. Following is the basic system diagram for the connection of host processor, switch, and PHY.



Serial Management Block Diagram via Switch and PHY

The switch generates an OUTCLK clock to host processor and the same frequency will be back to the switch via INCLK pin. There is a data format defined under below table which specifies a communication between the host processor and switch at serial IODATA pin. IODATA and MDIO are bi-direction I/O. The serial management format starts with start bit, then, follows operator, 10-bit register address, turn around, 16-bit content of data, and an idle bit. A command/response from host processor to the switch registers, Reg28H and Reg29H, can be given based on read/write operation, register address selection, and data.

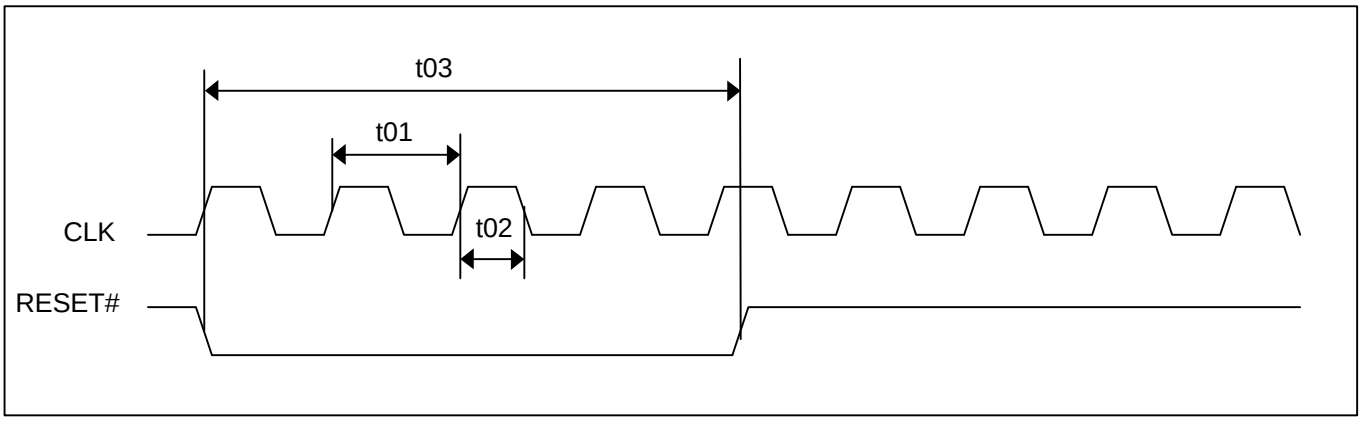
Command	Start Bit	Operator	Register Address	Turn Around	Data	Idle
Read	01	10	AAAAAAAAAA	Z0	DDDDDDDDDDDDDDDD	Z
Write	01	01	AAAAAAAAAA	10	DDDDDDDDDDDDDDDD	Z

LED Interface

MX98216EC has three LEDs. At initial stage, these represent address table self-test, memory test, and reset status respectively. And at normal state, these represent buffer full, packet loss, and broadcast storm status. Users can monitor the status of switch network via the LEDs.

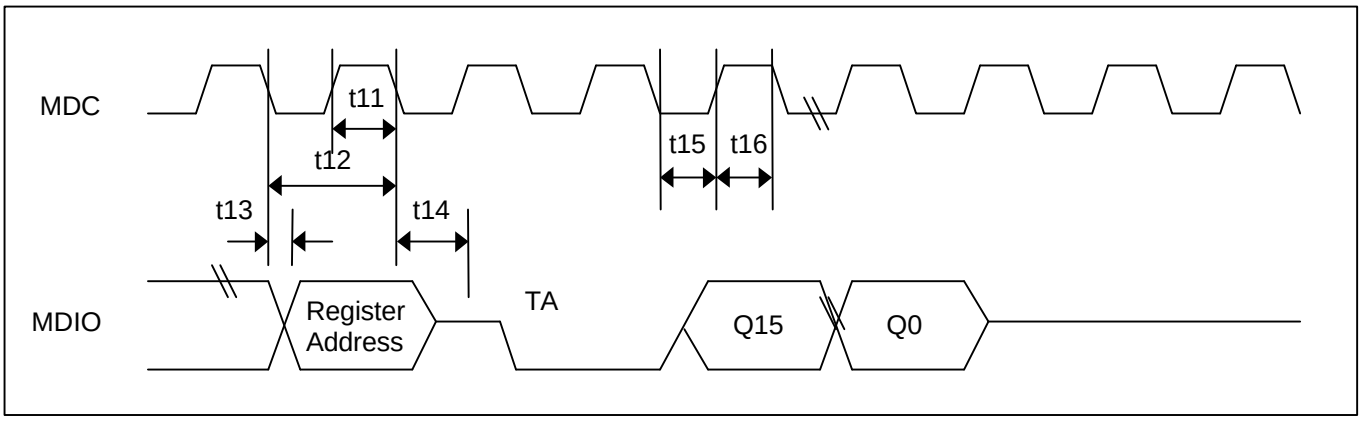
TIMING DIAGRAM

Reset and Clock Timing



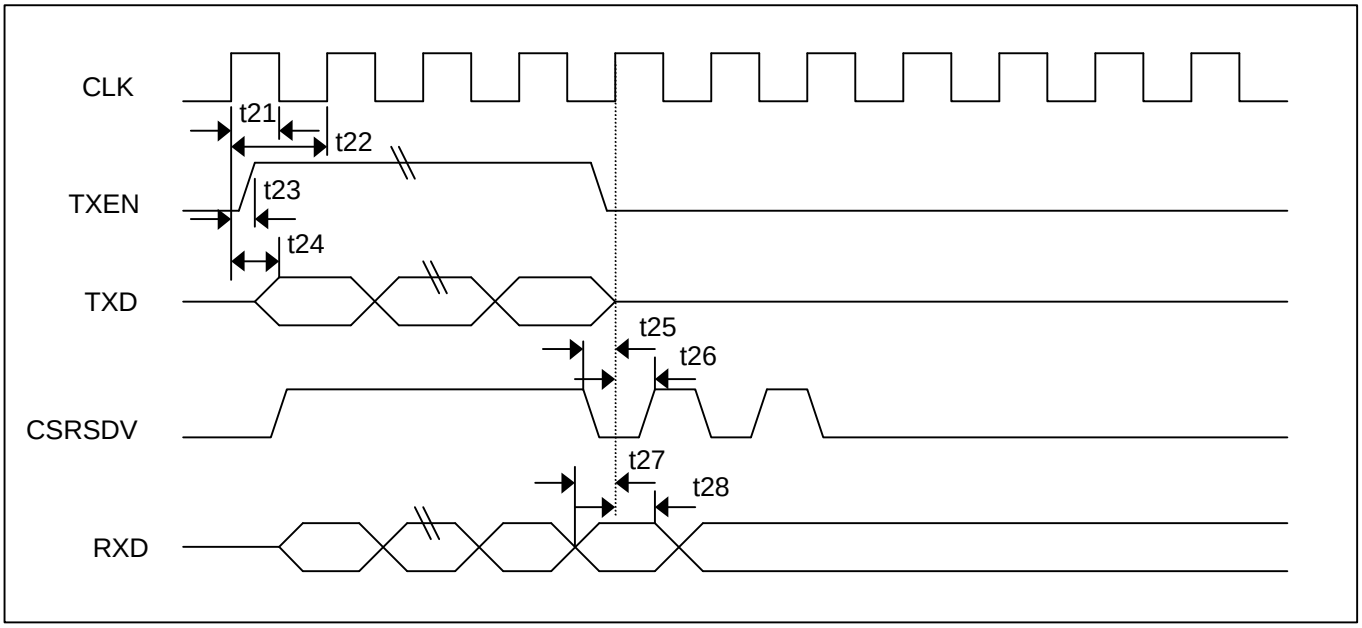
T#	DESCRIPTION	MIN	TYP	MAX	UNIT
.t01	System clock period	20	20.2		ns
.t02	System clock high time	9	10	11	ns
.t03	RESET# low pulse duration	1			ms

PHY Management (MDIO) Reading Timing



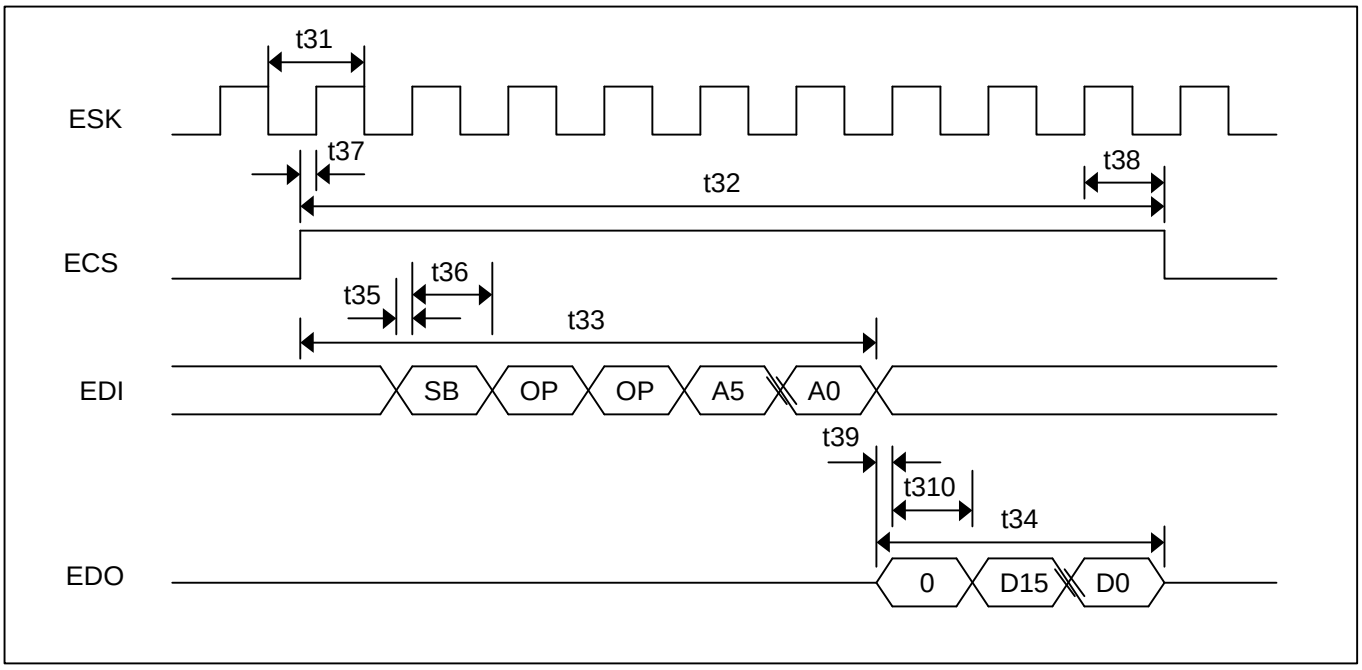
T#	DESCRIPTION	MIN	TYP	MAX	UNIT
.t11	MDC high time		200		ns
.t12	MDC clock period		400		ns
.t13	MDC falling edge to MDIO delay	3		8	ns
.t14	MDC falling edge to MDIO Hi-Z	3		8	ns
.t15	MDIO setup time	2			ns
.t16	MDIO hold time	2			ns

RMII Interface Timing



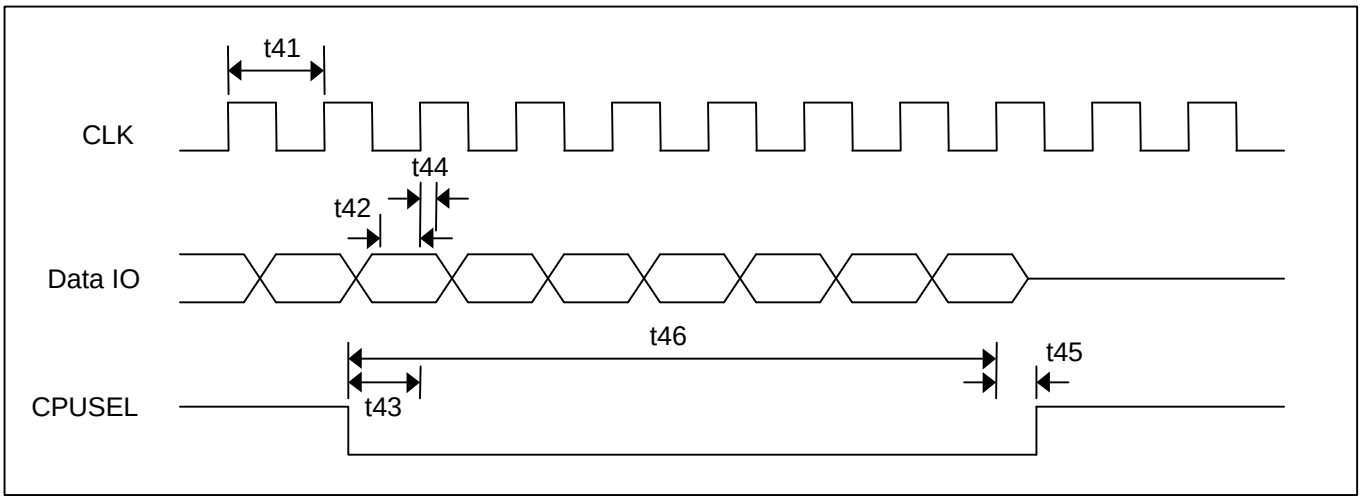
T#	DESCRIPTION	MIN	TYP	MAX	UNIT
.t21	CLK high time	9	10	11	ns
.t22	CLK clock period		20		ns
.t23	CLK to TXEN delay	3.5		10.5	ns
.t24	CLK to TXD delay	3.5		11.5	ns
.t25	CRSDV setup time	0			ns
.t26	CRSDV hold time	4			ns
.t27	RXD setup time	0			ns
.t28	RXD hold time	4			ns

EEPROM Interface Timing



T#	DESCRIPTION	MIN	TYP	MAX	UNIT
.t31	ESK clock		2560		ns
.t32	93C46 chip enable		27		ESK
.t33	93C46 command input cycle		10		ESK
.t34	93C46 data output cycle		17		ESK
.t35	93C46 data input setup time		3		ns
.t36	93C46 data input hold time				ns
.t37	93C46 chip select setup time		3		ns
.t38	93C46 chip select hold time				ns
.t39	93C46 data output setup time		3		ns
.t310	93C46 data output hold time				ns

CPU Interface Timing



T#	DESCRIPTION	MIN	TYP	MAX	UNIT
.t41	CPU clock period		120		ns
.t42	Data IO setup timing		10		ns
.t43	Chip select setup timing		10		ns
.t44	Data IO hold timing		10		ns
.t45	Chip select hold timing		10		ns
.t46	Chip select period		3840		ns

ELECTRONICAL SPECIFICATION

Absolute Maximum Rating

Parameter	SYMBOL	MIN	MAX	UNIT
I/O Supply Voltage	V_{dd}	-0.5	4.6	V
Core Supply Voltage	V_{CC}	-0.5	2.5	V
Input Voltage	V_I	-0.5	6	V
Output Voltage	V_O	-0.5	6	V
Storage Temperature	T_{STG}	-65	150	˚C
Operation Temperature	T_{OPR}	-40	125	˚C
latch-up Current	T_{LAT}			mA

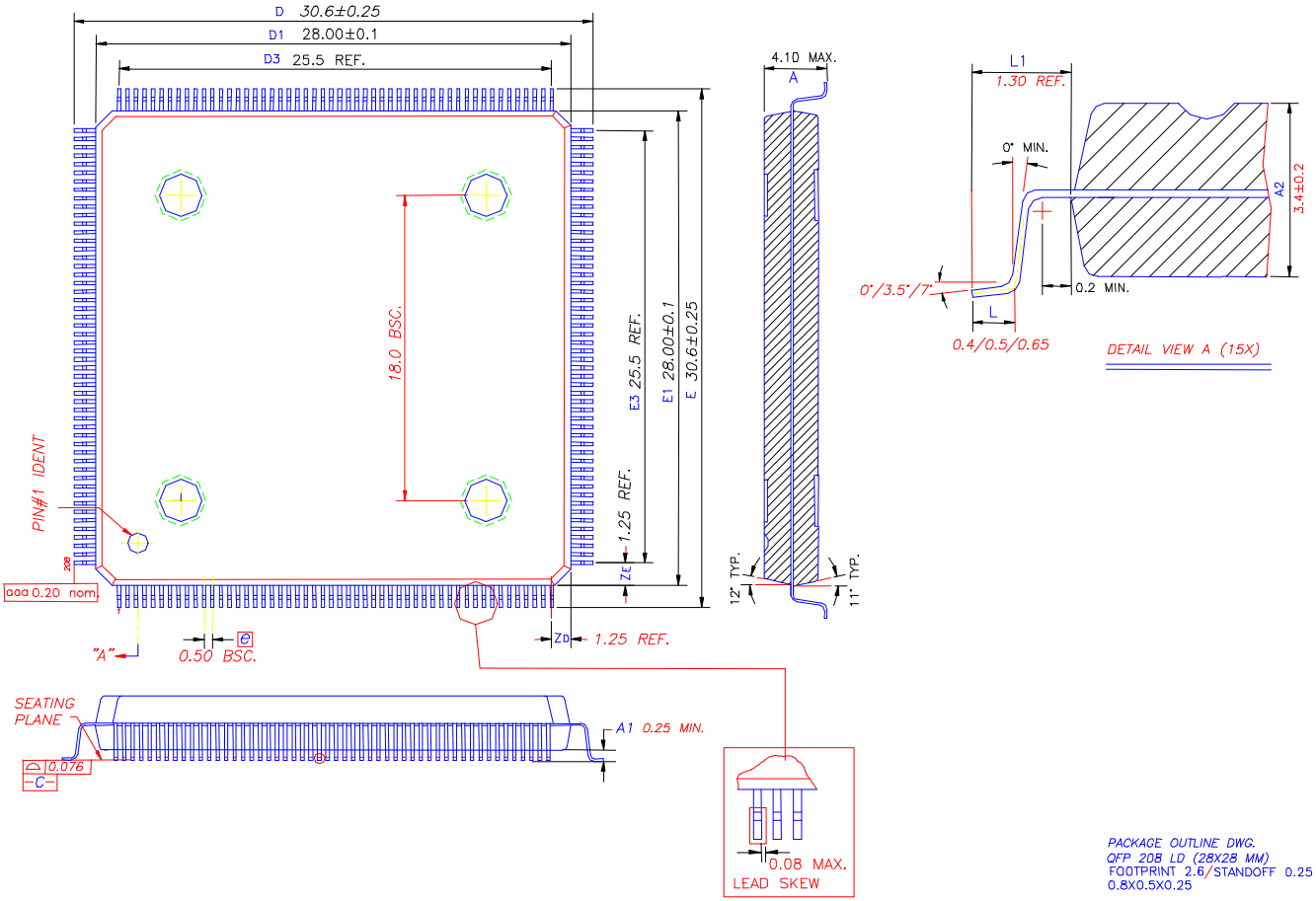
Recommended Operating Conditions

Parameter	SYMBOL	MIN	MAX	UNIT
I/O Supply Voltage	V_{dd}	3.0	3.6	V
Core Supply Voltage	V_{CC}	1.62	1.98	V
Operating Temperature	T_{OPR}	0	70	˚C
Power Dissipation				
Junction Temperature	T_j	0	125	˚C
Low-level Input Voltage	V_{IL}	-0.3	0.8	V
High-level Input Voltage	V_{IH}	2.0	5.5	V

DC Characteristics

Parameter	SYMBOL	MIN	MAX	UNIT
Output High Voltage	V_{OH}	2.4		V
Output Low Voltage	V_{OL}		0.4	V
High Impedance State Output Current	I_{OZ}		±1	µA
Output High Current (@V_{OH} = 2.4V)	I_{OH}	6.2	76.0	mA
Output Low Current (@V_{OL} = 0.4V)	I_{OL}	4.5	30.3	mA
Input High Voltage	V_{IH}			
Input Low Voltage	V_{IL}			
Supply Current	I_{CC}			mA

PACKAGE INFORMATION



REVISION HISTORY

Revision	Description	Page	Date
0.2	Speed/duplex settings change to FORCE from REG31H to REG33H	23	04/18/2001

TOP SIDE MARKING

MX98216EC	line 1 : MX98216EC is MXIC part No. "E" : PQFP "C" : Commercial grade
C0013	line 2 : Assembly Date Code.
F40044937B1	line 3 : Wafer Lot No.
36CAX	line 4 : "36C" : Revision code "A" : Bonding option "X" : Not used
TAIWAN	line 5 : State

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