

SIEMENS

ICs for Communications

1-Chip Car Radio

TUA 4306

Specification 16.3.99

Edition 16.3.99

Published by Siemens AG,
Bereich Halbleiter, Marketing-
Kommunikation, Balanstraße 73,
81541 München

© Siemens AG 1995.

All Rights Reserved.

Attention please!

As far as patents or other rights of third parties are concerned, liability is only assumed for components, not for applications, processes and circuits implemented within components or assemblies.

The information describes the type of component and shall not be considered as assured characteristics.

Terms of delivery and rights to change design reserved.

For questions on technology, delivery and prices please contact the Semiconductor Group Offices in Germany or the Siemens Companies and Representatives worldwide (see address list).

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Siemens Office, Semiconductor Group.

Siemens AG is an approved CECC manufacturer.

Packing

Please use the recycling operators known to you. We can also help you – get in touch with your nearest sales office. By agreement we will take packing material back, if it is sorted. You must bear the costs of transport.

For packing material that is returned to us unsorted or which we are not obliged to accept, we shall have to invoice you for any costs incurred.

Components used in life-support devices or systems must be expressly authorized for such purpose!

Critical components¹ of the Semiconductor Group of Siemens AG, may only be used in life-support devices or systems² with the express written approval of the Semiconductor Group of Siemens AG.

- 1 A critical component is a component used in a life-support device or system whose failure can reasonably be expected to cause the failure of that life-support device or system, or to affect its safety or effectiveness of that device or system.
- 2 Life support devices or systems are intended (a) to be implanted in the human body, or (b) to support and/or maintain and sustain human life. If they fail, it is reasonable to assume that the health of the user may be endangered.

Ausgabe 16.3.99

Herausgegeben von Siemens AG,
Bereich Halbleiter, Marketing-
Kommunikation, Balanstraße 73,
81541 München

© Siemens AG 1995.

Alle Rechte vorbehalten.

Wichtige Hinweise!

Gewähr für die Freiheit von Rechten Dritter leisten wir nur für Bauelemente selbst, nicht für Anwendungen, Verfahren und für die in Bauelementen oder Baugruppen realisierten Schaltungen.

Mit den Angaben werden die Bauelemente spezifiziert, nicht Eigenschaften zugesichert.

Liefermöglichkeiten und technische Änderungen vorbehalten.

Fragen über Technik, Preise und Liefermöglichkeiten richten Sie bitte an den Ihnen nächstgelegenen Vertrieb Halbleiter in Deutschland oder an unsere Landesgesellschaften im Ausland.

Bauelemente können aufgrund technischer Erfordernisse Gefahrstoffe enthalten.

Auskünfte darüber bitten wir unter Angabe des betreffenden Typs ebenfalls über den Vertrieb Halbleiter einzuholen.

Die Siemens AG ist ein Hersteller von CECC-qualifizierten Produkten.

Verpackung

Bitte benutzen Sie die Ihnen bekannten Verwerter. Wir helfen Ihnen auch weiter – wenden Sie sich an Ihren für Sie zuständigen Vertrieb Halbleiter. Nach Rücksprache nehmen wir Verpackungsmaterial sortiert zurück. Die Transportkosten müssen Sie tragen.

Für Verpackungsmaterial, das unsortiert an uns zurückgeliefert wird oder für das wir keine Rücknahmepflicht haben, müssen wir Ihnen die anfallenden Kosten in Rechnung stellen.

Bausteine in lebenserhaltenden Geräten oder Systemen müssen ausdrücklich dafür zugelassen sein!

Kritische Bauelemente¹ des Bereichs Halbleiter der Siemens AG dürfen nur mit ausdrücklicher schriftlicher Genehmigung des Bereichs Halbleiter der Siemens AG in lebenserhaltenden Geräten oder Systemen² eingesetzt werden.

- 1 Ein kritisches Bauelement ist ein in einem lebenserhaltenden Gerät oder System eingesetztes Bauelement, bei dessen Ausfall berechtigter Grund zur Annahme besteht, daß das lebenserhaltende Gerät oder System ausfällt bzw. dessen Sicherheit oder Wirksamkeit beeinträchtigt wird.
- 2 Lebenserhaltende Geräte und Systeme sind (a) zur chirurgischen Einpflanzung in den menschlichen Körper gedacht, oder (b) unterstützen bzw. erhalten das menschliche Leben. Sollten sie ausfallen, besteht berechtigter Grund zur Annahme, daß die Gesundheit des Anwenders gefährdet werden kann.

Table of Contents		Page
1	Features	2
1.1	AM/FM-Receiver	2
1.2	FM-Mode	2
1.2.1	FM-Receiver	2
1.2.2	FM-IF Demodulator	2
1.3	Stereodecoder	3
1.4	AM Mode	3
2	Pinning	4
3	Ordering Information	4
4.1	AM/FM-Receiver	5
4.2	FM-MODE	5
4.3	Stereodecoder	5
4.4	AM - MODE	6
5	Pin Configuration	7
6	Pin Description	8
7	Blockdiagram 1	10
8	Blockdiagram 2	11
9	Blockdiagram 3	12
10	Blockdiagram 4	13
11	Absolute Maximum Ratings	14
12	Operational Range	15
13	AC / DC Characteristics	16
14	Truthtables	25
15	Test Circuit	26
16	Application Circuit	27
17	Diagram 1	28
18	Diagram 2	29
19	Diagram 3	30

Last Edition: DOK-Nr. V66047

from July 22nd 1998

1 Features

1.1 AM/FM-Receiver

- High flexibility with an external preamplifier stage for AM and FM
- Strictly symmetrical RF parts
- Separate mixers for AM and FM mode
- Sym. or asym. mixer inputs
- Only one 2-pin-oscillator for the 1st LO; in AM mode the oscillator frequency is divided
- 1st LO with LC-tank circuit
- 1st LO at 100 MHz range
- 1st LO decoupled counter output
- 1st LO decoupled divided counter output
- Improved low phase noise
- FM/AM field strength output combined

1.2 FM-Mode

1.2.1 FM-Receiver

In this mode, the receiverpart is comprised of a mixer, an oscillator, a prestage control and an IF post amplification.

- Integrated AGC generation for PIN Diodes and MOSFETs
- High level mixer input
- High input/output 3rd order interceptpoint

1.2.2 FM-IF Demodulator

The FM-IF-demodulator has been developed especially for car radio applications.

- 7stage limiter amplifier
- Coincidence demodulator
- Field strength output (combined with AM)
- Fixed mute depth (with full muting typ 80dB)
- Multipath detector with analog output

1.3 Stereodecoder

This part provides the stereo decoder function and noise blanking for FM car radio applications.

- Internal reference voltage source
- Adjustment free oscillator with ceramic resonator 456 kHz
- Pilot dependent mono/stereo switching with hysteresis
- Stereo indicator output
- Analog mono/stereo blend control (stereo noise control, SNC)
- Pilot canceller (19 kHz)
- Adjacent channel noise suppression (114 kHz)
- Mute facility
- Analog deemphasis control (high cut control, HCC)
- Interference noise detector with integrated high-pass filter (IF level signal or MPX input)
- MPX-input low-pass filter
- Noise blanking at MPX -demodulator outputs- L, R audio is common to AM Mode

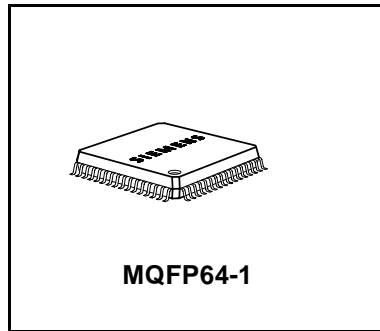
1.4 AM Mode

In this mode, the IC is comprised of a mixer, an oscillator with a divider by 4, 6, 8 or 10, a prestage control, 2nd mixer to convert the 1st IF to the 2nd IF, 2nd local force oscillator (buffer for external source), automatic gain controlled amplifier and quasisynchronous demodulator.

The same oscillator is used in AM and FM mode.

- 2nd mixer with force input for mixing frequency
- Output for AM IF counter
- Wide range 2nd IF AGC amplifier
- Quasi synchronous demodulator for AM mode
- Fast AM search tuning stop feature
- HCC for AM

2 Pinning



Pin	Function	Pin	Function	Pin	Function
1	MP det in	23	IF amp bias	45	Deem L
2	MP det cap	24	IF amp in	46	AF out L
3	MP det out	25	+V rf	47	AF out R
4	AM seek m	26	GND rf	48	Vref H/S
5	AM IF count	27	SEL A	49	Contr. HCC
6	GND IF	28	SEL B	50	Contr. SNC
7	FM IF bias	29	1st mix out	51	Pil ind out
8	FM IF in	30	1st mix out	52	Pil det cap
9	AM IF bias	31	Pre cap AM	53	MPX in
10	AM IF in	32	Pre cap FM	54	Stereo PLL
11	AM IF bias	33	RF in FM	55	Stereo osc
12	2nd mix out	34	RF in FM	56	Iref stereo
13	2nd mix out	35	RF in AM	57	N det in
14	AM IF cap	36	RF in AM	58	MPX out
15	2nd LO	37	Vref RF	59	GND stereo
16	2nd mix in	38	1st LO	60	Mute FM
17	2nd mix in	39	1st LO	61	Dem FM
18	IF gain cap	40	Div count	62	Dem FM
19	IF amp out	41	Dir count	63	+Vif
20	V pre AM	42	Ng cap AM/FM	64	Fieldstr.
21	I pre FM	43	Nlev cap		
22	IF gain adj	44	Deem R		

3 Ordering Information

Type	Package	Ordering Code
TUA 4306	MQFP-64-1	Q67037-A1009

4. Circuit Description

General Description

The TUA 4306 is a one chip car radio system consisting of AM/FM receiver, AM-Up/Down conversion, AGC amplifier / demodulator, FM-IF limiter amplifier / demodulator and stereodecoder / noiseblanker.

4.1 AM/FM-Receiver

The AM/FM-receiver part includes a 2-pin varactor tuned oscillator. In the FM mode the direct oscillator frequency is fed into the double balanced FM mixer, in the AM mode the divided by 4, 6, 8 or 10 oscillator frequency is fed into the AM mixer.

The two separate symmetrical input stages of the IC, one optimized for FM-, the other for AM- mode allow symmetrical and unsymmetrical prestage configuration.

The AM and FM input frequencies are converted to a fix 1st IF in the 10.7 MHz range. The FM-IF is post amplified in a separate IF amplifier with DC adjustable gain, the AM-IF is fed directly to the 2nd mixer.

The TUA 4306 has been designed to work with a PLL in the 100MHz range in both modes or in the AM- mode with the divided frequency.

Depending on the input signal strength, the integrated AGC stage for prestage control drives PIN-Diodes as well as MOSFETs.

4.2 FM-MODE

FM-IF Demodulator

The FM-IF amplifier includes a 7 stage capacitive coupled limiter amplifier with coincidence demodulator and AF output. The AF output signal can be continuously attenuated to decrease the noise.

There is a field strength output (with min. 76 dB dynamic range, typ. ± 1 dB nonlinearity and typ. ± 3 dB temperature drift) and a fixed muting (with full muting typ 80 dB).

A multipath detector with analog output is available. Its input signal is fed from the high pass filter of the stereo-decoder/noiseblanker and a second 80 kHz 1-pole high pass filter.

4.3 Stereodecoder

Power supply, reference current:

A temperature-stable, low noise reference voltage generator is used for better ripple rejection and to generate a reference current. This current is used as a time base for the deemphasis, the gate time of the pulse former, and the pilot cancellation, avoiding temperature and tolerance effects .

MPX input, MPX filter:

A 4-pole low-pass filter determines the bandwidth of the MPX signal.

Voltage Controlled Oscillator, Phase Detector:

The 456 kHz oscillator and the frequency dividers are used as walsh function generators (suppression of 3rd order harmonics) for:

38 kHz for the stereo decoder

19 kHz inphase for phase detector and pilot cancellation

19 kHz quadrature for the phase detector.

The phase detector locks the on chip 19 kHz signal to the pilot tone in the MPX signal at 90 deg phase.

Pilot Detector, Pilot Indicator, Pilot Cancellation:

The voltage at the pilot detector output is proportional to the pilot tone input level. If that level is high enough, the pilot indicator output is activated and the pilot cancellation turned on: a 19 kHz signal proportional to the voltage at the pilot detector output is added to the MPX signal with inverse polarity, cancelling the 19 kHz pilot tone.

Interference Detector , Noise Detector, Pulse Former:

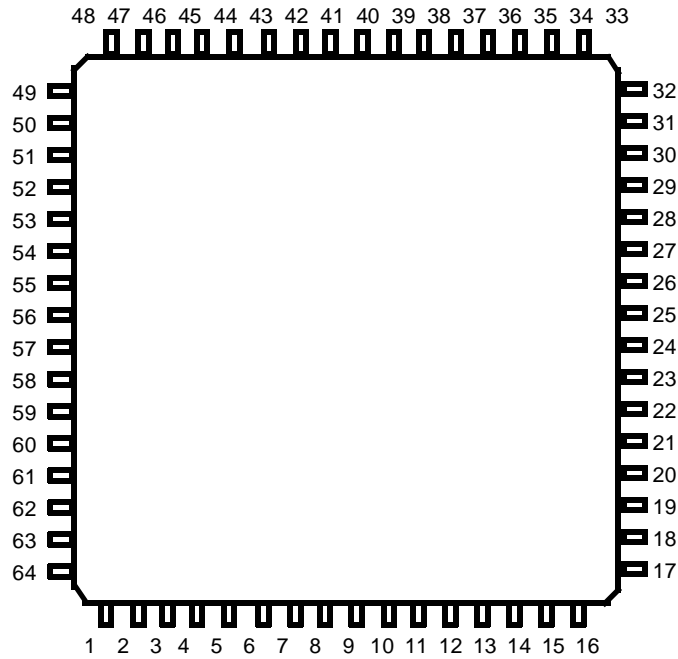
The signal from the interference input (MPX or field strength signal) passes a 4-pole high-pass filter to the noise blanking circuitry. The average noise level is stored in an external capacitor. The interference detector compares the actual noise level with that stored on the capacitor and triggers the pulse former if there is a sig-

nificant difference. The pulse former generates a gate pulse for the HCC block. During that pulse time the outputs of the deemphasis circuit are switched to hold mode.

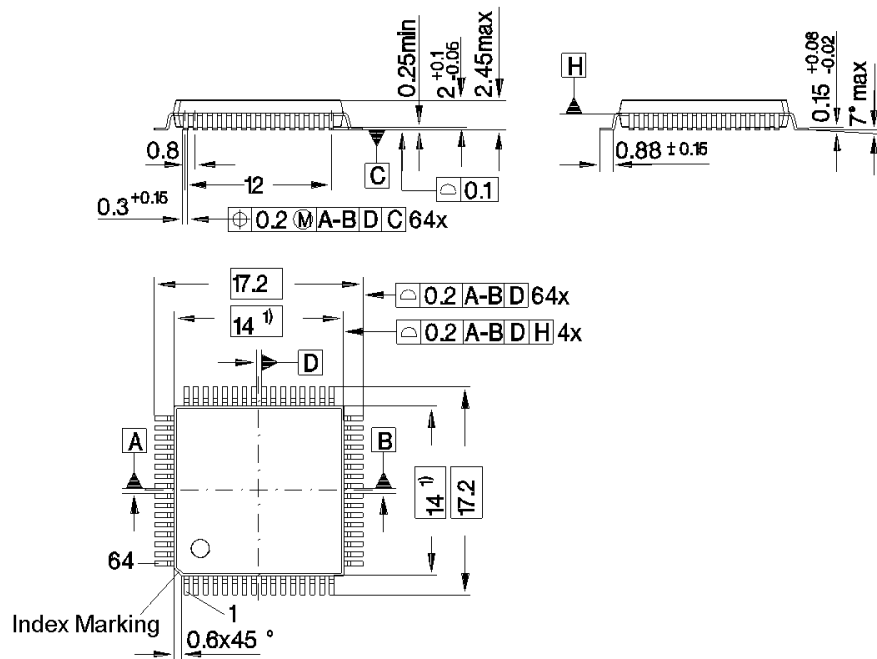
4.4 AM - MODE

In the AM mode the 1st IF is converted by the 2nd mixer into the 2nd IF in the 450 kHz range. Therefore a 2nd LO force input is part of the IC. The 2nd IF signal passes an automatic gain controlled IF amplifier and is then demodulated to the AF in a quasisynchronous demodulator. Switching to seek mode, the AGC time constant is reduced by a factor of 5, the AM IF counter output is switched on and the AF is muted. The AGC voltage is used as AM field strength and is fed to the combined field strength output.

5 Pin Configuration



P-MQFP 64-1



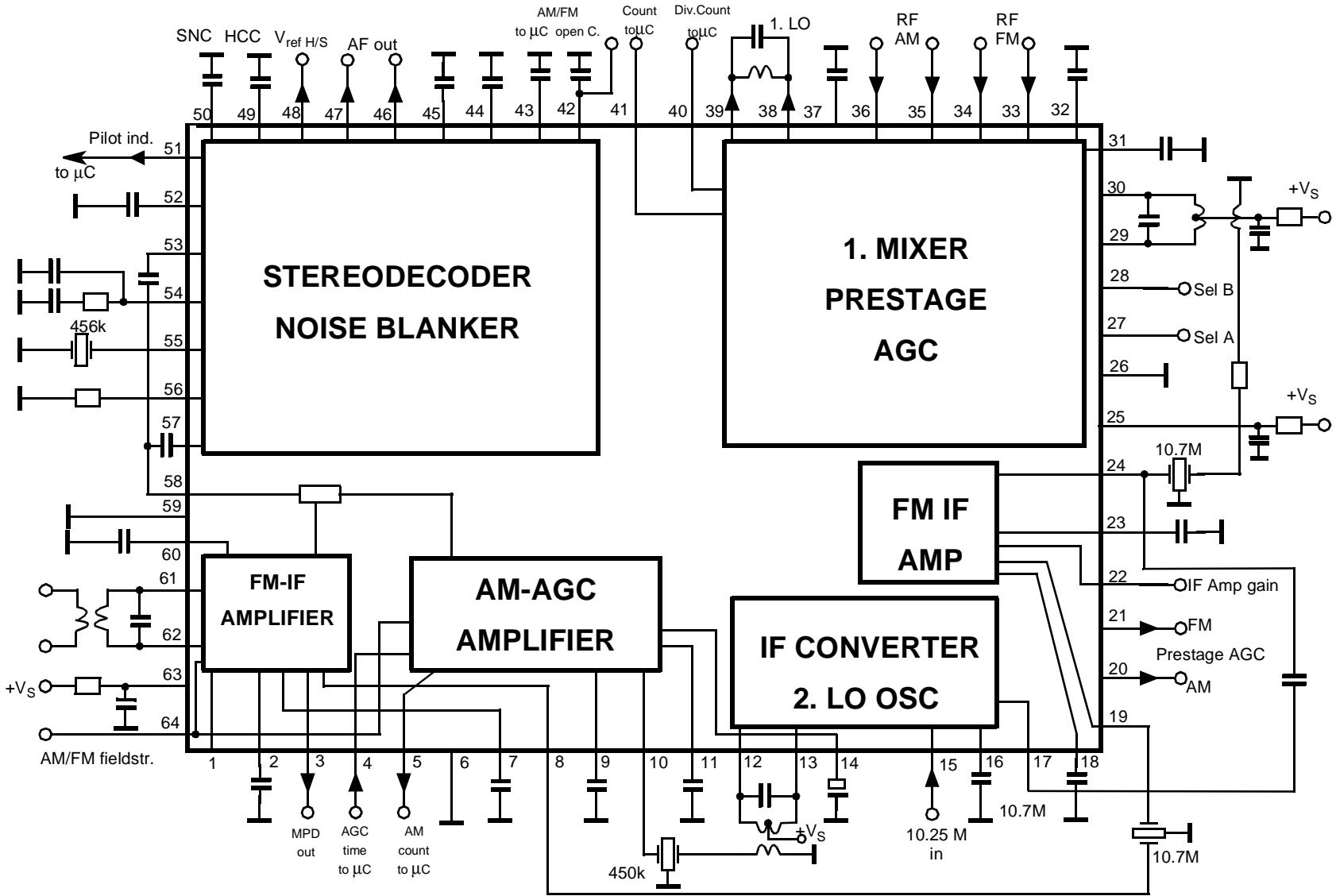
Does not include plastic or metal protrusion of 0.25 max. per side

6 Pin Description

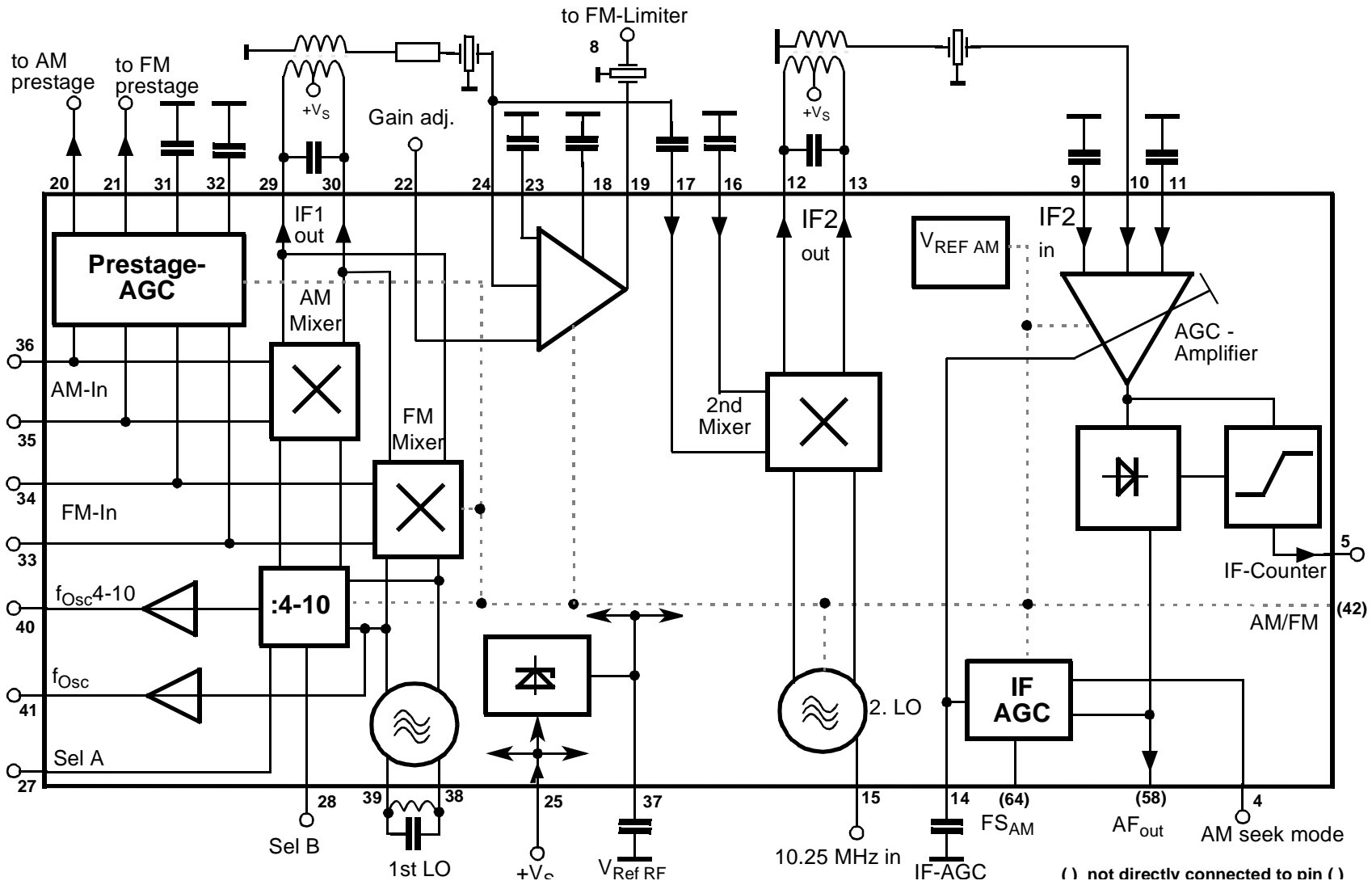
Pin No.	Symbol	Function
1	MP det in	Auxiliary multipath detector input (in parallel to internal connection)
2	MP det cap	Multipath detector rectifier capacitor
3	MP det out	Analog multipath detector output
4	AM seek m	AM seek mode switch; AM IF counter on, AM-AGC fast and AF-mute
5	AM IF count	AM-IF counter output for search tuning
6	GND IF	Ground IF
7	FM IF bias	FM limiter input bias decoupling capacitor
8	FM IF in	FM limiter input
9	AM IF bias	AM AGC amplifier bias decoupling capacitor
10	AM IF in	AM AGC amplifier input
11	AM IF bias	AM AGC amplifier bias decoupling capacitor
12	2nd mix out	2nd AM mixer output (open collector)
13	2nd mix out	2nd AM mixer output (open collector)
14	AM IF cap	AM AGC amplifier time constant capacitor
15	2nd LO	Frequency force input for 2nd mixer
16	2nd mix in	2nd AM mixer bias decoupling capacitor
17	2nd mix in	2nd AM mixer input
18	IF gain cap	10.7 MHz FM IF amplifier gain adjust blocking capacitor
19	IF amp out	10.7 MHz FM IF amplifier output
20	V pre AM	AM prestage AGC buffered voltage output
21	I pre FM	FM prestage AGC current output for PIN diode
22	IF gain adj	10.7 MHz FM IF amplifier DC controlled gain adjust
23	IF amp bias	10.7 MHz FM IF amplifier operation point
24	IF amp in	10.7 MHz FM IF amplifier input
25	+V rf	Supply voltage RF section
26	GND rf	Ground RF section
27	SEL A	AM divided counter ratio select A
28	SEL B	AM divided counter ratio select B
29	1st mix out	1st mixer output (open collector)
30	1st mix out	1st mixer output (open collector)
31	Pre cap AM	AM prestage AGC time constant capacitor
32	Pre cap FM	FM prestage AGC time constant capacitor; output for MOS FET Gate 2
33	RF in FM	FM 1st mixer symmetrical inputs

Pin No.	Symbol	Function
34	RF in FM	FM 1st mixer symmetrical inputs
35	RF in AM	AM 1st mixer symmetrical inputs
36	RF in AM	AM 1st mixer symmetrical inputs
37	Vref RF	Reference voltage RF section (4.8 V)
38	1st LO	1st local AM/FM oscillator circuit
39	1st LO	1st local AM/FM oscillator circuit
40	Div count	1st local oscillator divided by 4, 6, 8 or 10 counter output (disabled in FM mode)
41	Dir count	1st local oscillator counter output
42	Ng cap AM/FM	Timing capacitor for Noisedetector monoflop (gate time) AM/FM mode control; low voltage activates AM section and disables stereodecoder VCO, Phase detector, Pilot detector, SNC and FM section
43	Nlev cap	Hold capacitor for Noise detector average level low voltage applied mutes the stereo decoder outputs
44	Deem R	HCC timing / hold capacitor, deemphasis right
45	Deem L	HCC timing / hold capacitor, deemphasis left
46	AF out L	AF output left
47	AF out R	AF output right
48	Vref H/S	Reference voltage SNC / HCC
49	Contr. HCC	Control voltage HCC (high cut control)
50	Contr. SNC	Control voltage SNC (stereo noise control), external decreasing of stereo separation possible
51	Pil ind out	Pilot indicator output, active high (open collector)
52	Pil det cap	Pilot detector capacitor, low voltage activates mono state
53	MPX in	Stereo decoder MPX signal input
54	Stereo PLL	Stereo decoder PLL phasedetector, loop filter
55	Stereo osc	VCO pin for ceramic resonator
56	Iref stereo	Reference current pin, external reference resistor
57	N det in	Noise detector input
58	MPX out	FM MPX signal and AM demodulator signal output
59	GND stereo	Ground stereodecoder
60	Mute FM	Dynamic FM mute control blocking capacitor
61	Dem FM	Demodulator circuit FM
62	Dem FM	Demodulator circuit FM
63	+Vif	Supply voltage IF and stereodecoder section
64	Fieldstr.	AM/FM fieldstrength combined output

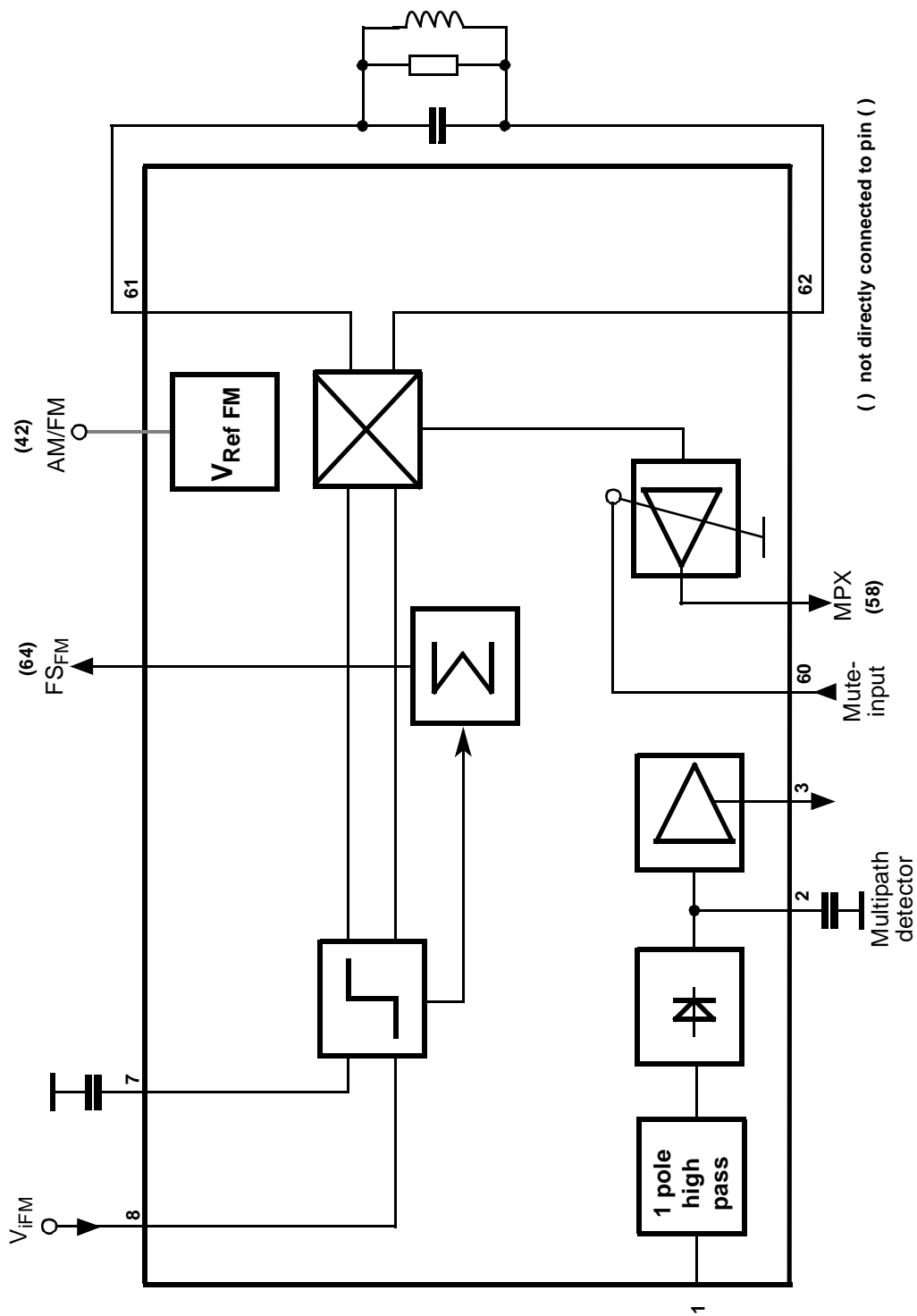
7 Blockdiagram 1



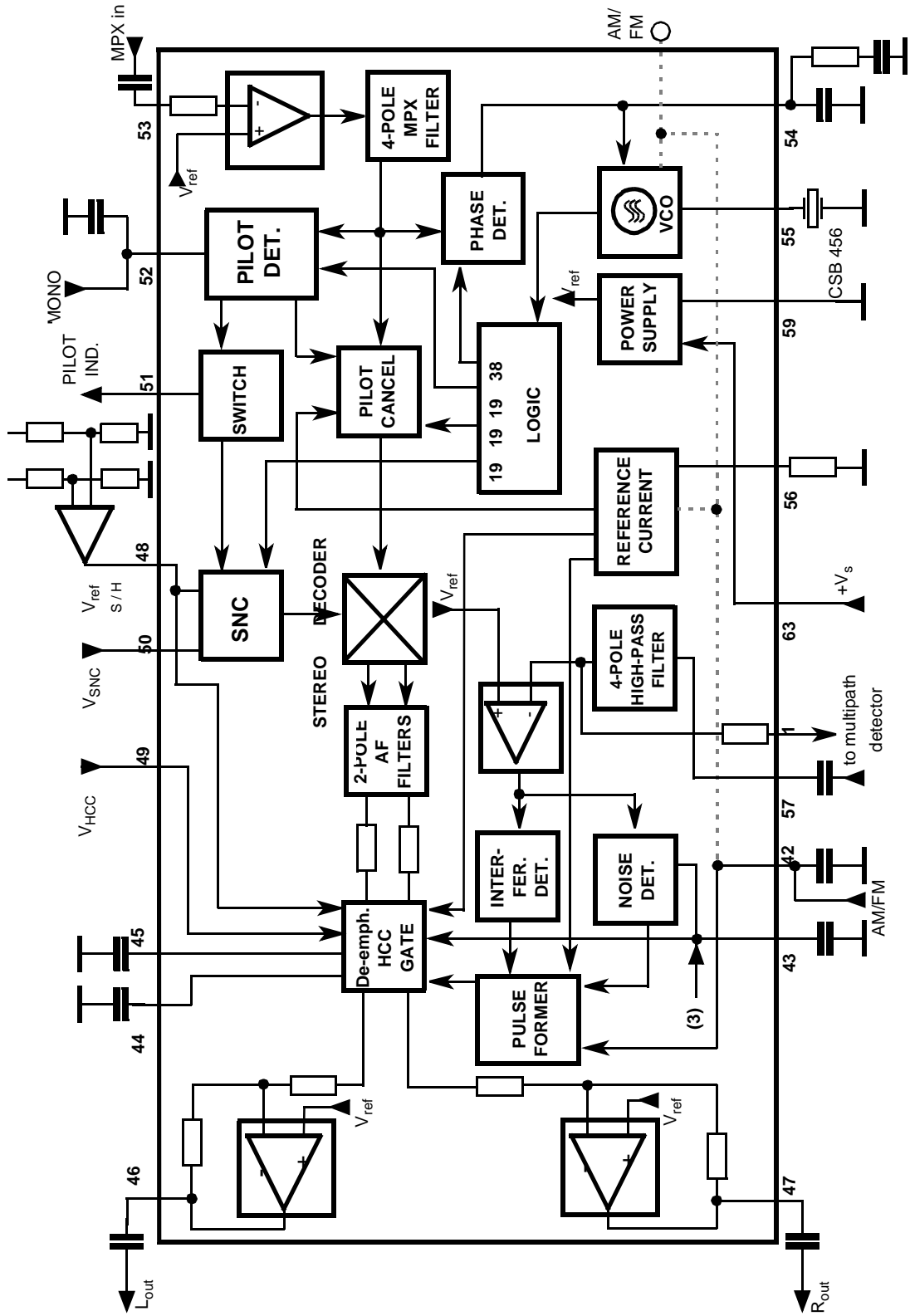
8 Blockdiagram 2



9 Blockdiagram 3



10 Blockdiagram 4



11 Absolute Maximum Ratings

The AC / DC characteristic limits are not guaranteed the maximal ratings may not be exceeded under any circumstances, not even momentary and individual, as permanent damage to the IC will result.

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min	max		
Junction temperature	T_J	-40	150	°C	
Storage temperature	T_S	-40	125	°C	
Thermal resistance	R_{thSA}		54	K/W	
ESD-voltage, HBM	V_{ESD}	-4	+4	kV	100pF, 1500 Ω

Ambient Temperature under bias: $T_A = -40$ to $+85^\circ\text{C}$

12 Operational Range

Within the operational range the IC operates as described in the circuit description. The AC / DC characteristic limits are not guaranteed

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min	max		
Supply voltage	V_S	8	9	V	
Ambient temperature	T_A	-40	85	°C	

13 AC / DC Characteristics

AC / DC characteristics involve the spread of values guaranteed within the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production.

Supply Voltage $V_S = 8.5 \text{ V}$
 Ambient temperature $T_{\text{amb}} = 25 \text{ °C}$

Parameter	Test Circuit	Symbol	Limit Values			Unit	Test conditions
			min	typ	max		
1. Current consumption	1	I_{SFM}	80	100	120	mA	FM mode
	1	I_{SAM}	65	80	105	mA	AM mode
1.AM/FM-Receiver							
1st LO							
1. Frequency range	1	$f_{1\text{st LO}}$	80		140	MHz	
2. Frequency range	Lab	$f_{1\text{st LO}}$	50		150	MHz	$Q_{\text{factor of coil}} > 90$
3. Counter output	1	V_{41}	70	100		mV_{rms}	$R_{L41} = 330\Omega$; Ref. Appl. board
4. Divided counter output	1	V_{40}	28	40		mV_{rms}	$R_{L40} = 330\Omega$; Ref. Appl. board
4a. Divided counter output	Lab	V_{40}		150		mV_{rms}	$R_{L40} = 10\text{k}\Omega$; Ref. Appl. board
5. Output impedance	Lab	R_{40}	0.8	1	1.2	$\text{k}\Omega$	
6. Output impedance	Lab	R_{41}	240	300	360	Ω	
7. Frequency	1	$f_{1\text{st LO}}$	10			MHz	$V_{\text{tuning}} = 0\text{V}$
10.7 MHz IF amplifier $f_{\text{IF1}} = 10.7 \text{ MHz}$							
8. DC input voltage	1	V_{24}	3.5	3.9	4.3	V	
9. Input resistance	1	R_{24}	270	330	390	Ω	AM
10. Output resistance	1	R_{19}	270	330	390	Ω	
11. Max. voltage gain	1	A_{24-19}	23	26	29	dB	$V_{22} = 1.5\text{V}$
12. Min. voltage gain	1	A_{24-19}	13	16	19	dB	$V_{22} = 3.5\text{V}$
13. Noise figure	Lab	F_{FM}		7		dB	$\text{RG} = 330\Omega$
14. Reference voltage	1	V_{37}	4.5	4.8	5.1	V	
15. Output Current	1	I_{37}			1	mA	

Parameter	Test Circuit	Symbol	Limit Values			Unit	Test conditions
			min	typ	max		
AM mode							
f _{IF1} = 10.7 MHz							
f _{IF2} = 450 kHz							
f ₃₅₋₃₆ = 1 MHz							
V ₄₂ =1V							
Mixer 1							
1. Interceptpoint 3rd order	Lab	I _{P3}		134		dBμV	Special testcircuit necessary
2. Mixer gain	1	A _{M1}	2	6	10	dB	V _{35,36} =80mV _{rms} (R _L =330Ω)
3. Max. input voltage	1	V ₃₅₋₃₆	1100	1400		mV _{pp}	SINAD> 34dB;m=80%
4. Noise figure (10 MHz)	Lab	F		7		dB	R _{g opt} =700Ω
5. Input impedance	Lab	R ₃₅₋₃₆	3.2	4	4.8	kΩ	sym.
6. Input impedance	Lab	C ₃₅₋₃₆	1.6	2	2.4	pF	sym.
7. Input impedance	Lab	R ₃₅₋₃₆	1.6	2	2.4	kΩ	asym.
8. Input impedance	Lab	C ₃₅₋₃₆	3.2	4	4.8	pF	asym.
9. Divider select low	1	V _{27,28L}	0		1.3	V	
10. Divider select high	1	V _{27,28H}	3.0		V _s	V	
Prestage AGC output							
11. AGC-voltage AM	1	V ₂₀	6.5	7.5		V	V _{35,36} =50mV _{rms}
12. AGC-voltage AM	1	V ₂₀	0		0.5	V	V _{35,36} =200mV _{rms}
13. AGC-voltage FM	1	V ₃₂	0		0.15	V	V _{35,36} =50mV _{rms}
14. AGC-current FM	1	I ₂₁	0		0.1	mA	V _{35,36} =50mV _{rms}
15. Integrator Current	1	I ₃₁ *	-12	-25	-45	μA	V _{35,36} =50mV _{rms} V _m =3V
16. Integrator Current	1	I ₃₁ *	+10	+25	+40	μA	V _{35,36} =150mV _{rms} V _m =3V
17. Integrator Current	1	I ₃₁ *	-17	-35	-55	μA	V _{35,36} =0mV _{rms} V _m =3V
18. Integrator Current	1	I ₃₁ *	+50	+70	+90	μA	V _{35,36} =400mV _{rms} V _m =3V

Parameter	Test Circuit	Symbol	Limit Values			Unit	Test conditions
			min	typ	max		
2 nd AM IF section Mixer 2							
1. Mixer gain	1	A_{M2}	7	10	13	dB	$V_{17}=1\text{mV};$ $V_{\text{out}}=V_{\text{IF}450}$ $f_{17}=10.7\text{ MHz};$ $f_{15}=10.25\text{ MHz}$
2. Noise figure	Lab	F		10		dB	
3. Max Input Voltage	1	V_{16-17}		1400		mV_{pp}	SINAD> 34dB;m=80%
4. Input impedance	Lab	R_{16-17}		1.8	-	$\text{k}\Omega$	
Frequency force input							
5. Operational frequency	Lab	f_{15}	10	10.25	25	MHz	
6. External force voltage	1	V_{15}	60			mV_{rms}	$R_g=600\Omega;$ $C_k=100\text{pF}$

Parameter	Test Circuit	Symbol	Limit Values			Unit	Test conditions
			min	typ	max		
FM mode							
f _{IF} =10.7 MHz							
f ₃₃₋₃₄ =100 MHz							
V ₄₂ =open							
Mixer 1							
1. Intercept point 3rd order	Lab	I _{P3}		125		dB μV	special testcircuit necessary
2. Noise figure (10 MHz)	Lab	F		6		dB	R _{g opt} =500Ω
3. Mixer gain	1	A _{M1}	5	9	13	dB	V ₃₃₋₃₄ =10mV _{rms} ; R _L =330Ω
4. Input impedance	Lab	R ₃₃₋₃₄	3.2	4	4.8	kΩ	sym.
5. Input impedance	Lab	C ₃₃₋₃₄	1.6	2	2.4	pF	sym.
6. Input impedance	Lab	R ₃₃₋₃₄	1.6	2	2.4	kΩ	asym.
7. Input impedance	Lab	C ₃₃₋₃₄	3.2	4	4.8	pF	asym.
Prestage AGC output							
8. AGC voltage FM	1	V ₃₂	5.6	6.4	7.2	V	V _{33,34} =0mV _{rms}
9. AGC voltage FM	1	V ₃₂	0		0.1	V	V _{33,34} =50mV _{rms}
10. AGC current FM	1	I ₂₁	9.5	12	14.5	mA	V _{33,34} =0mV _{rms} V _m =0.7V
11. AGC current FM	1	I ₂₁	0		0.1	mA	V _{33,34} =50mV _{rms} V _m =0.7V
12. AGC voltage AM	1	V ₂₀	0		0.5	V	V _{33,34} =0
13. AGC sink current AM	1	I ₂₀	3			mA	V _{33,34} =0
14. AGC voltage AM integrator	1	V ₃₁		6	7.5	V	V _{33,34} =0
15. Integrator Current	1	I ₃₂ *	- 12	- 25	- 46	μA	V _{33,34} =0 V _m =4.8V
16. Integrator Current	1	I ₃₂ *	+15	+30	+50	μA	V _{33,34} =60mV _{rms} V _m =4.8V
17. Integrator Current	1	I ₃₂ *	+50	+70	+90	μA	V _{33,34} =150mV _{rms} V _m =4.8V

*) Integrator currents are measured between the output pin (- Pole of the measurement equipment) and a voltage source V_m (+ Pole)

2.FM Demodulator

Measuring condition:

f_{IF}=10.7 MHz; Δf= ±75 kHz; f_{mod}= 1 kHz; V₈=10 mV_{rms}

V₄₂=open; Deemphasis= 100 μs

Fieldstrength dynamic range	1	V ₆₄	66	72		dB	see Diagram D1
Fieldstrength nonlinearity	1	V ₆₄		±1		dB	see Diagram D2
Fieldstrength temperature drift	1	V ₆₄			±3	dB	see Diagram D3

Parameter	Test Circuit	Symbol	Limit Values			Unit	Test conditions
			min	typ	max		
Fieldstrength load capacitance	Lab				50	pF	
Fieldstrength load resistance	Lab		1			kΩ	
Fieldstrength voltage	1	V ₆₄	4	4.6	5.2	V	V ₈ =200mV _{rms}
Fieldstrength voltage	1	V ₆₄	1.5	1.9	2.3	V	V ₈ =1mV _{rms}
Fieldstrength voltage	1	V ₆₄	0		1	V	V ₈ =0mV _{rms}
2. AF-output voltage	1	V ₅₈	400	500	600	mV _{rms}	R _L >10kΩ; Deemph.=100 μs
3. AF-output voltage	Lab	V ₅₈		600		mV _{rms}	R _L >10kΩ; no Deemph.
4. Input voltage for limiter threshold	1	V ₈		33	45	μV _{rms}	V ₅₈ =V ₅₈ - 3dB
5. Total harmonic distortion	1	THD ₅₈		0.9	1.2	%	
6. AM-suppression	1	a _{AM}	70	80		dB	m=30 %
7. Signal-to-noise ratio	1	a _{S/N}	72	80		dB	
8. AF mute	1	a _{AF}	12	14	16	dB	V ₆₀ =0
Multipath detector f ₅₇ =200 kHz							
10. Attack current	1	I ₂ *)	600	800	1070	μA	V _{57AC} =1V _{pp} , V _m =5.0 V
11. Recovery current	1	I ₂ *)	- 6	- 9	-12	μA	V _{57AC} =0; V _m =3.6V
12. Start voltage	1	V _{3Def}	4.4	4.7		V	V _{57AC} =0V
13. Detector characteristic	1	V ₃	V _{3Def0.14V}	V _{3Def-0.1V}	V _{3Def}	V	f ₅₇ =25kHz; V ₅₇ =160mV _{pp}
14. Detector characteristic	1	V ₃	V _{3Def-3.3V}	V _{3Def-2.8V}	V _{3Def-2.3V}	V	f ₅₇ =200kHz; V ₅₇ =160mV _{pp}

*) Integrator currents are measured between the output pin (- Pole of the measurement equipment) and a voltage source V_m (+ Pole)

Parameter	Test Circuit	Symbol	Limit Values			Unit	Test conditions
			min	typ	max		

3. Stereodecoder

Measuring condition:

$V_{53}=600\text{mV}_{\text{rms}}$; $f=1\text{ kHz}$; 15kHz LP with 19kHz Notch; see appendix

1. Total harmonic distortion	1	$\text{THD}_{46,47}$		0.1	0.3	%	$f=1\text{ kHz}$
2. Signal to noise ratio	1	$\text{S/N}_{46,47}$	65	75		dB	Stereo
3. Channel separation	1	a_{Sep}	28	40		dB	
4. AF output voltage	1	$V_{46,47}$	650	780	900	mV_{rms}	Stereo/Mono
5. Overdrive margin	1	$V_{46,47\text{ max}}$		2		dB	THD= 1%
6. AF output DC voltage	1	$V_{\text{DC }46,47}$	2.5	3	3.5	V	
7. Difference of output voltage levels	1	$\Delta V_{46,47}$			2	dB	
8. Muting depth	1	$A_{46,47}$	70	75		dB	$V_{43}=0$
9. Muting depth	1	$A_{46,47}$	70	75		dB	$V_4=0.7\text{V}$
10. DC-offset at mute	1	$\Delta_{\text{DC }46,47}$	-100	0	100	mV	
11. DC-offset stereo on/off	1	$\Delta_{\text{DC }46,47}$	-100	0	100	mV	

Carrier and harmonic suppression (referenced to $V_{46,47}=780\text{ mV}_{\text{rms}}$)

1. Pilotsignal (f=19kHz) subcarrier	1	α_{19}	40	45		dB	
2. (f=38kHz)	1	α_{38}	40	50		dB	
3. (f=57kHz)	1	α_{57}	40	50		dB	

Mono/Stereo control

Pilot threshold voltage:

1. For stereo "on"	1	V_{PILon}		20	30	mV_{rms}	
2. For stereo "off"	1	V_{PILoff}	5	14		mV_{rms}	
3. Hysteresis	Lab			3		dB	$V_{\text{PILon}} / V_{\text{PILoff}}$

Stereo-indicator output

4. Pilot off		$V_{51\text{off}}$			0.5	V	$I_{51}=1\text{mA}$
5. Pilot on					10	μA	

external control voltages (active low)

6. Operational voltage for external mono control (pin 52)	1	$V_{52\text{ thr}}$			1	V	
7. Operational voltage for AM/FM (pin 42)	1	$V_{42\text{thr}}$			1	V	AM on

Deemphasis

Reference frequency = 400Hz

 $C_{deemph}=10nF$; $\tau_{nom}=75 \mu s$

8. Minimum FM attenuation	1	$A_{min FM}$	5	7	9	dB	$V_{49} \geq 3.8V$; $f_m=5kHz$
9. Maximum FM attenuation	1	$A_{max FM}$	12	15	18	dB	$V_{49}=1.5 V$ V ; $f_m=5kHz$
10. Minimum AM attenuation	1	$A_{min AM}$	5	7	9	dB	$V_{49} \geq 3.4V$; $f_m=5kHz$
11. Maximum AM attenuation	1	$A_{max AM}$	12	15	18	dB	$V_{49}=1.5V$; $f_m=5kHz$

Stereo/Mono blend control :

1. Channel separation	1	a_{Sep}	28			dB	$V_{50}=3.8V$
2. Channel separation	1	a_{Sep}			3	dB	$V_{50}=3.3V$

Oscillator

3. Max. Osc. frequency	1	f_{oscmax}	0.7	1.0	2.0	%	$100 \% \times (f_{max} / 456kHz-1)$
4. Min. Osc. frequency	1	f_{oscmin}	-2.0	-1.0	-0.7	%	$100 \% \times (f_{max} / 456kHz-1)$
5. VCO-gain	1		-12	-8	-4	kHz/V	$\Delta f / \Delta V_{54}$
6. Oscillator voltage	1		2.5	4	5.5	V	$V_{55 DC}$
7. Oscillator swing	1		260	370	470	mV_{rms}	$V_{55 AC}$

PLL

8. PD-gain	note 1	$\Delta i / \Delta \phi$	6.0	8.2	10.2	$\mu A / rad$	$V_{pilot} = 54 mV_{rms}$
------------	--------	--------------------------	-----	-----	------	---------------	---------------------------

Noise detector

9. Input resistance	Lab	R_{57}	80	99	120	k Ω	
10. Input high-pass filter	Lab	f_{in57}	80	100	120	kHz	-3dB
11. Trigger threshold	1	$V_{57 min}$		30	50	mV_{rms}	$V_{43} = V_{43} (V_{57 mean}=0)$, $f_{57}=200 kHz$
12. Trigger threshold	1	$V_{57 dyn}$	130	170	210	mV_{rms}	$V_{43} = V_{43} (V_{57 mean}=50mV_{rms})$, $f_{57}=200 kHz$
13. Maximum noise mean value *	1	$V_{57maxmean}$	65	80	115	mV_{rms}	$f_{57}=200 kHz$
14. Suppression pulse duration	1		34	40	46	μs	
15. Input offset current	Lab	$I_{44,45}$	-50	0	50	nA	
16. Attack current	Lab	I_{43att}		880		μA	$V_{43}=5.5V$
17. Recovery current	Lab	I_{43rec}		20		μA	$V_{43}=4V$

*) The trigger threshold is adapted to the input noise. IF max. noise mean value is exceeded, threshold is too high for any trigger of the noise blanker

4.AM Mode**AGC-Amplifier****Measuring condition:** **$f_{iF} = 450 \text{ kHz}$; $f_{mod} = 1 \text{ kHz}$; $V_{10} = 10\text{mV}_{rms}$, **Deemphasis=100 μs****

1. AGC-range	1	ΔA	60	66		dB	$V_{58}=V_{58AM} \pm 3\text{dB}$
2. Input sensitivity	1	V_{10}		100		μV_{rms}	$V_{58}=V_{58AM} - 3\text{dB}$
3. AGC time seek mode on	1	V_{4L}	0		0.7	V	
4. AGC time seek mode off	1	V_{4H}	2.4		5	V	
5. Integrator Current	1	I_{14}^*	15	25	35	μA	$V_{10}=0$; $V_m=3\text{V}$
6. Integrator Current	1	I_{14}^*	- 13	- 25	-33	μA	$V_{10}=100\text{mV}_{rms}$; $V_m=3\text{V}$
7. Integrator Current	1	I_{14}^*	400	+500	650	μA	$V_{10}=0$ $V_m=3\text{V}$; $V_4=0.7 \text{ V}$
8. Integrator Current	1	I_{14}^*	-400	- 500	-650	μA	$V_{10}=100\text{mV}_{rms}$; $V_m=3\text{V}$; $V_4=0,7 \text{ V}$
9. Field strength output	1	V_{64}	0	0.3	0.8	V	$V_{10}=0 \text{ mV}$; seek mode off
10. Field strength output	1	V_{64}	1.4	1.75	2.1	V	$V_{10}=500 \mu\text{V}$; seek mode off
11. Field strength output	1	V_{64}	3	3.4	4	V	$V_{10}=5 \text{ mV}$; seek mode off
12. Field strength output	1	V_{64}	4	4.4	5.1	V	$V_{10}=30 \text{ mV}$; seek mode off

*) Integrator currents are measured between the output pin (- Pole of the measurement equipment) and a voltage source V_m (+ Pole)

Demodulator

13. AF output voltage	1	V_{58AM}	360	480	600	mV_{rms}	$m=0.8$
14. AF output voltage	Lab	V_{58AM}	283	406	550	mV_{rms}	$m=0.8$; Deemph=100 μs
15. Total harm. distortion	1	THD_{58}		0.7	2.5	%	
16. (S+N)/N	1		40	50		dB	$m=0.8$; $V_{10}=200\mu\text{V}$
17. (S+N)/N	1		60	70		dB	$m= 0.8$; $V_{10}=100\text{mV}_{rms}$
18. AF-linearity	1	ΔV_{58}			3	dB	

IF - Counter

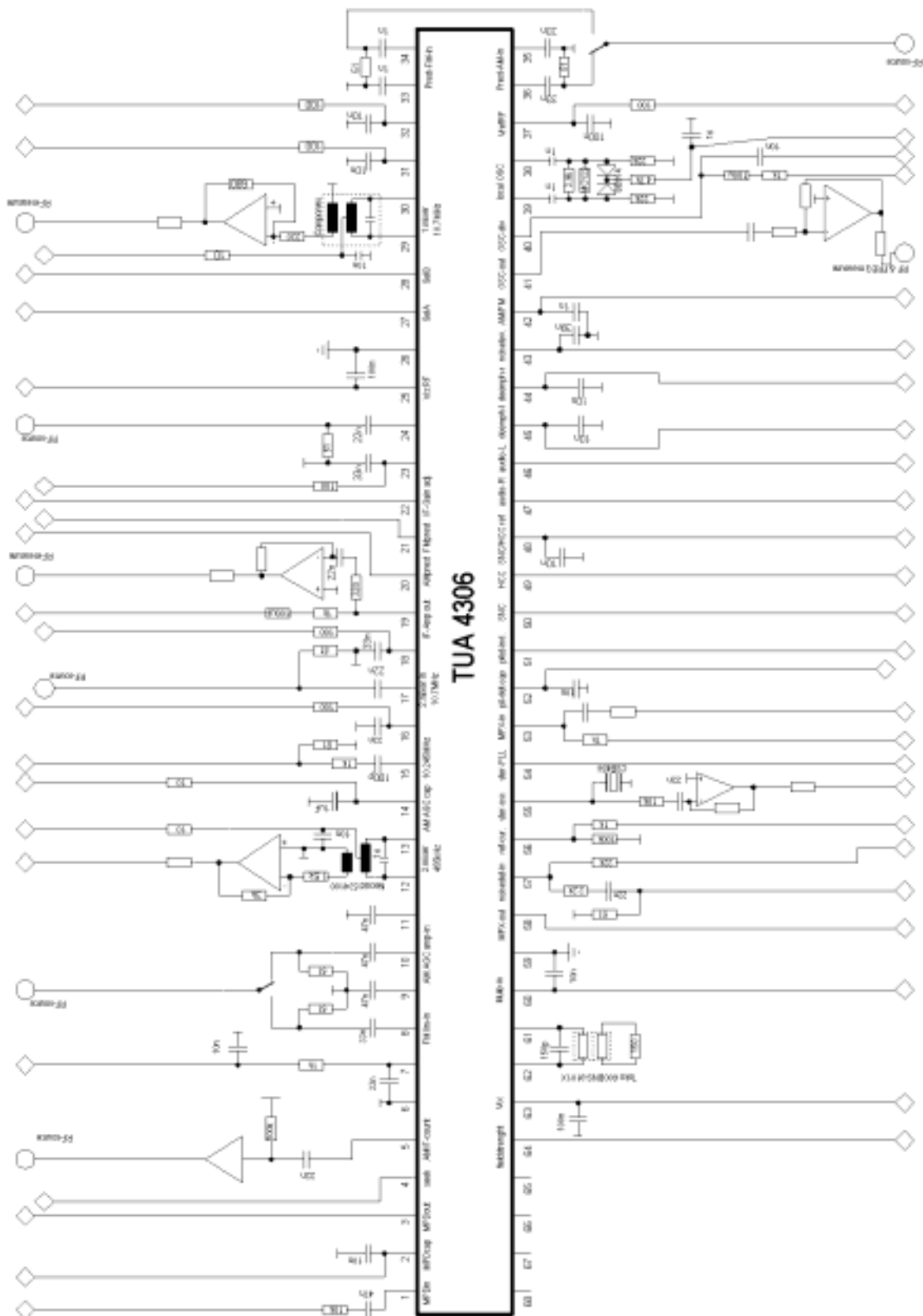
19. IF - counter Output voltage	1	V_5	220	270		mV_{rms}	$R_L=100k\Omega$ $V_4=0.7 V$; Ref. Appl. Board
20. IF-counter output voltage	1	V_5			0.5	V_{DC}	$V_4=2.4V$
21. IF-counter Output voltage	1	V_{5AC}			2	mV_{rms}	$V_4=2.4V$

14 Truthtables

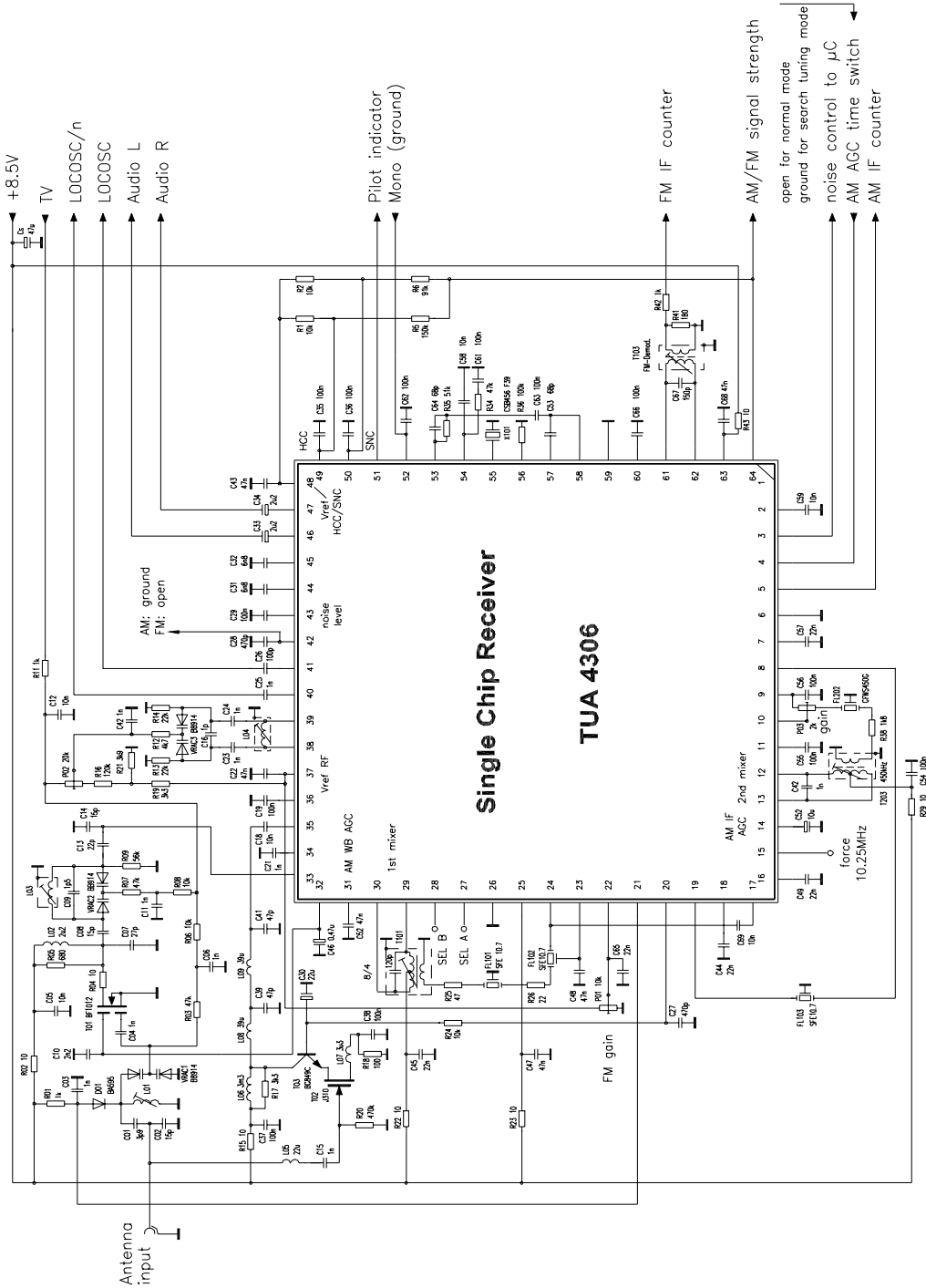
AM 1st LO ECL divider truthtable

	Sel A	Sel B					
divide by 4	0	0					
divide by 6	0	1					
divide by 8	1	0					
divide by 10	1	1					

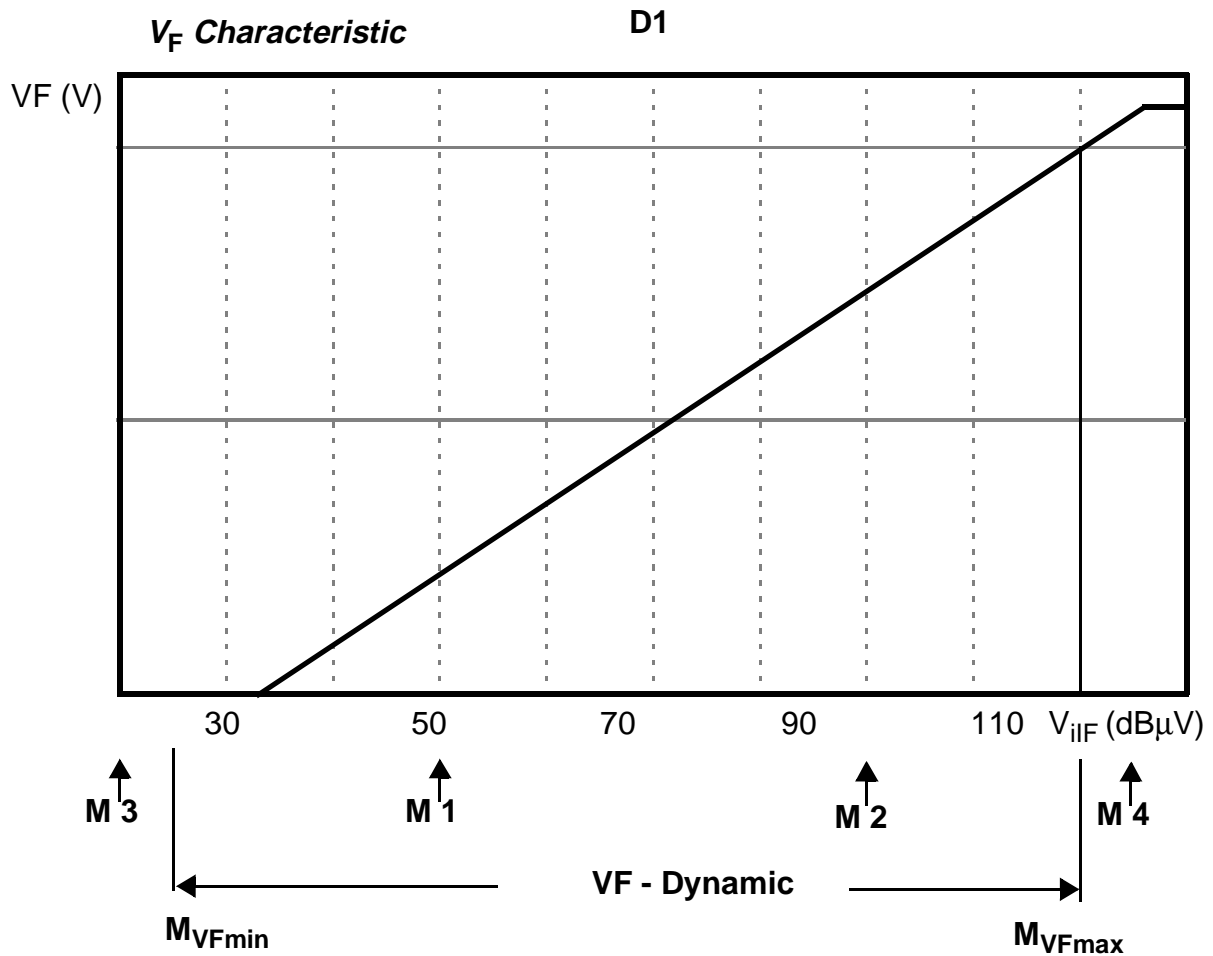
15 Test Circuit



16 Application Circuit



17 Diagram 1



V_F - Dynamic :The dynamic range of V_F voltage is determined by the test points M1 through M4 as follows:

- M1: test point (at V_{illF}= 50 dBμV) supplies V_F (M1)
- M2: test point (at V_{illF}= 90 dBμV) supplies V_F (M2)
- M3: test point (at V_{illF}= 20 dBμV) supplies V_F (M3)
- M4: test point (at V_{illF}=120 dBμV) supplies V_F (M4)

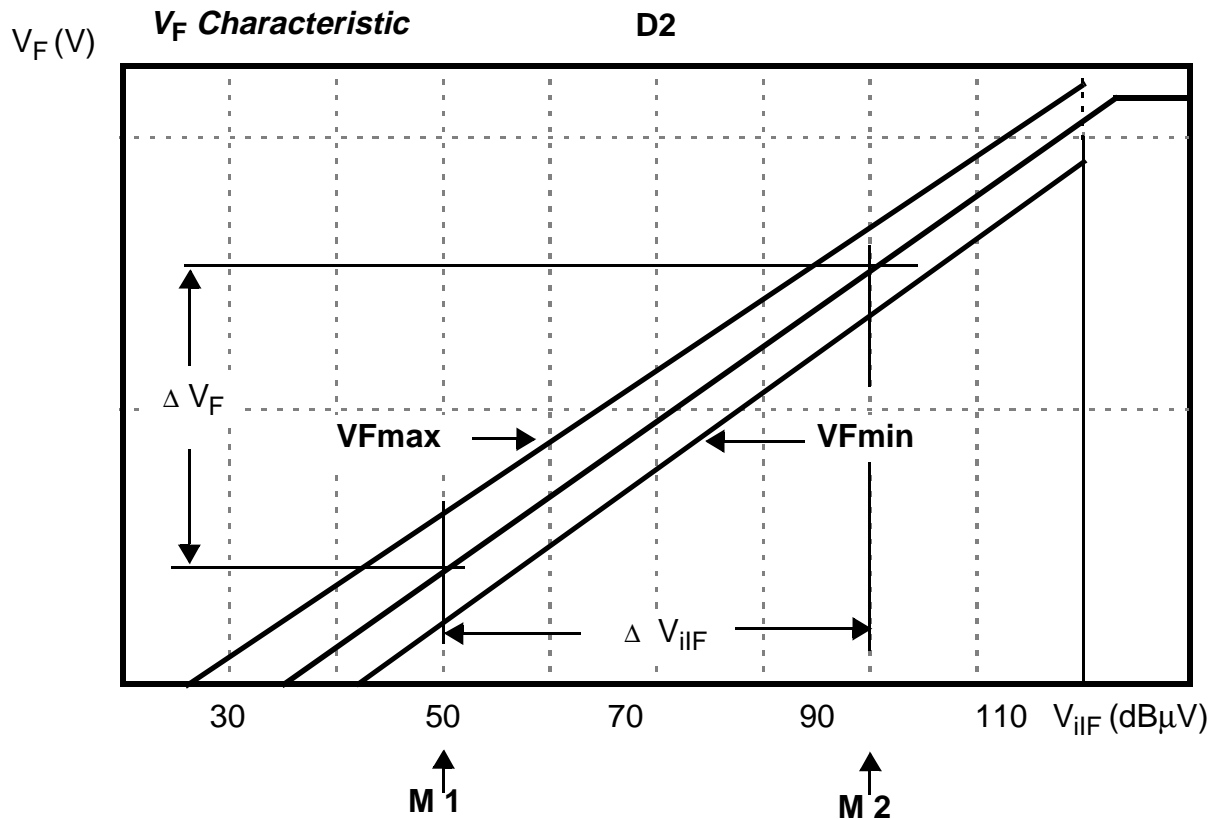
Hence follows :

$$M_{VFmax} := 90 \text{ dB}\mu\text{V} + \frac{V_F (M4) - V_F (M2)}{V_F (M2) - V_F (M1)} \times 40 \text{ dB}$$

$$M_{VFmin} := 50 \text{ dB}\mu\text{V} - \frac{V_F (M1) - V_F (M3)}{V_F (M2) - V_F (M1)} \times 40 \text{ dB}$$

V_F - Dynamic = M_{VFmax} - M_{VFmin}

18 Diagram 2



Test points to determine VF linearity

VF - Linearity: is determined at 25 °C

$$\text{Slope } : m = \frac{V_F (M2) - V_F (M1)}{40 \text{ dB}}$$

The tolerance range of the VF - linearity is determined by two parallel lines:

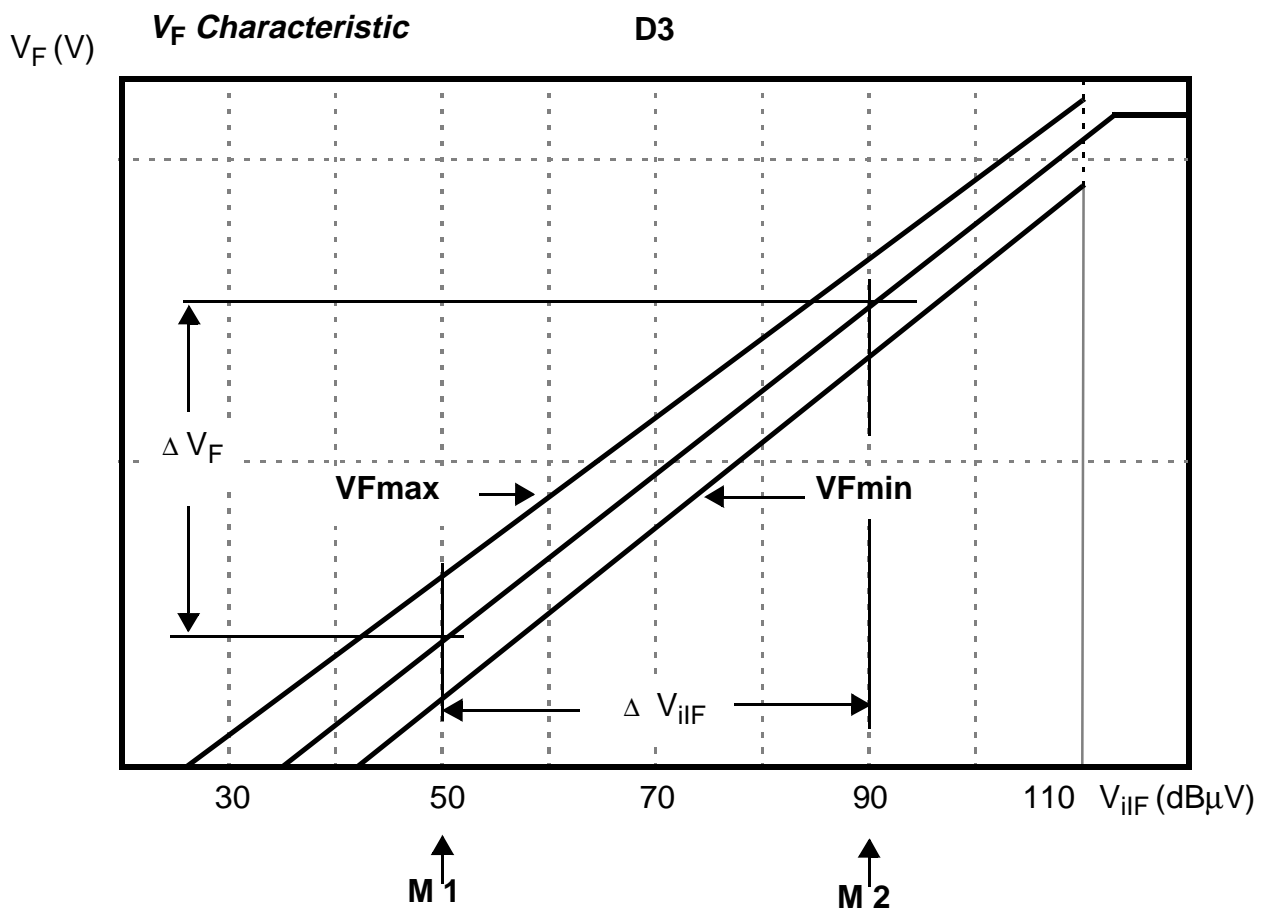
$$V_{Fmax} = V_F (M1) + m (M + 60 \text{ dB} + 1 \text{ dB})$$

$$V_{Fmin} = V_F (M1) + m (M + 60 \text{ dB} - 1 \text{ dB})$$

The VF values within the VF dynamic range (MVFmin ≤ M ≤ MVFmax) must be inside the predetermined tolerance range:

$$V_{Fmin} \leq V_F (M) \leq V_{Fmax}$$

19 Diagram 3



V_F -Temperatur - Drift : It is determined within -40 bis +85 °C

$$\text{Slope} : m = \frac{V_F(M2) - V_F(M1)}{40 \text{ dB}} \quad (\text{at } 25 \text{ }^\circ\text{C})$$

The tolerance range of the V_F temperature drift is determined by two parallel lines:

$$V_{Fmax} = V_F(M1) + m(M + 60 \text{ dB} + 3\text{dB})$$

$$V_{Fmin} = V_F(M1) + m(M + 60 \text{ dB} - 3\text{dB})$$

The V_F values for temperatures between -40 to +85 °C within the V_F dynamic range ($M_{V_{Fmin}} \leq V_F \leq M_{V_{Fmax}}$) must be inside the predetermined tolerance field:

$$V_{Fmin} \leq V_F(M) \leq V_{Fmax}$$